iEPS

PROCEEDINGS OF THE TECHNICAL CONFERENCE

VOLUME TWO

SEVENTH ANNUAL (1987)
INTERNATIONAL ELECTRONICS
PACKAGING CONFERENCE
BOSTON, MASS

PUBLISHED BY
INTERNATIONAL ELECTRONICS PACKAGING SOCIETY INC.
114 NORTH HALE STREET, SUITE 2B
WHEATON, IL 60187
PHONE: (312) 260-1044

Republication rights for any of the papers included in these Proceedings are retained by the individual authors and/or their employers. Permission to reprint must therefore be obtained from them. In the event of such republication, due credit must be given to the Seventh Annual International Electronics Packaging Conference and to these Proceedings as the source.

Additional copies of the Proceedings may be purchased, while the supply lasts, at $75.00 per copy, from the International Electronics Packaging Society, Inc., 114 N. Hale Street, Wheaton, IL 60187

SILVER-FILLED GLASS ADHESIVE CONTACT RESISTIVITIES

by T. Corbett* and G. Shirley
Intel Corporation
Component Assembly/Test
145 S. 79th St.
Chandler, AZ 85226

* Now at: Micron Technology, Boise, ID

pp733-749

Abstract

The transmission line method (TLM) was used to measure contact resistivities of silver-filled glass (SFG) to silver and gold cavity metallization, to wafer backs prepared in several ways, and to the "jumper" chips used as an intermediary in supplying substrate bias to the back of the die. Contact resistivity for SFG to jumper chip was 8 times larger than for Au-eutectic to jumper chip, but was still acceptable for device performance. Good ohmic contact to Cr/Au-coated wafer backs was obtained independently of whether the backs were prepared by "sand blasting" or by grinding, or whether or not the wafers had undergone an oxidation step (370°C, 2min) subsequent to Cr/Au coating. Uncoated wafers did not have ohmic contacts to SFG. Contact resistivity of SFG to gold cavity metallization was 4 times higher than SFG to silver cavity metallization. For Cr/Au-coated die backs, the bulk resistance of the silicon die dominates the resistance between the front of the die and the cavity metallization. Also, the bulk resistance of the jumper

chip dominates the resistance between the top of the jumper chip and the bulk of the SFG. Thus, for Cr/Au-coated die backs and jumper chips, use of SFG has no adverse device performance-related consequences.

1. Introduction

Silver-filled glass (SFG) has become an attractive option for attaching a die to the cavity of a ceramic package. It is less expensive and more suited to automation than the conventional gold-eutectic die attach process, and it opens the possibility of elimination of metallized cavities. In addition to the required mechanical performance, the silver-filled glass process should not degrade the electrical performance of the device. Two factors which might affect the electrical performance of a device are (i), the total resistance between the surface of the die and the cavity metallization and (ii), the resistance in the "jumper chip" circuit sometimes used to supply substrate bias to the back of the die. See Fig. 1. These resistances have contributions from the bulk resistivity of the silicon, the die-attach medium and cavity metallization, and the contact resistances at the several interfaces which the die-attach medium has to other conductors in the package. The three interfaces which the die-attach medium makes with the other conductors in the package are indicated in Fig. 1.

For real devices it is impossible to separate the various contributions to the resistance between the die surface and the cavity metallization. It is possible, however, to fabricate test structures which can be used to separate the various contact resistances from the bulk resistances. These test structures enable the application of the transmission line method (TLM) of contact resistance measurement. The TLM method used in this study is described in Section 2.

We studied several combinations of materials which form the three interfaces shown in Fig. 1. The materials and their processing are discussed in Section 3. Conclusions are presented in the final section.

2. Contact Resistance Measurement Theory

When a conducting film is deposited on another conducting film, the interface between the films has a contact resistivity, ρ_c (ohm cm^2), which is a characteristic of the interface. The problem of measuring this contact resistivity was first addressed by Shockley[1], and developed by subsequent workers[2-6]. The method is called the "transmission line method" (TLM). A pattern of parallel stripes of the top film is patterned onto the bottom film. Resistance measurements are made between many adjacent and non-adjacent pairs of stripes. This is illustrated in Fig. 2. The figure also shows the parameters of the theory: r_1 (ohms/square) is the sheet resistance of the bottom film, r_2 is the sheet resistance of the top film, d is the stripe width, and l is the spacing between stripes. The width of the stripes (into the plane of Fig. 2) is Z. The theory is simpler when the sheet resistance of the top film is much less than that of the bottom film ($r_2 << r_1$). This is the case for all structures studied in this paper. Sometimes it is necessary to account for the possibility that the sheet resistance of the bottom film is different under the top film than where it is bare. This was necessary for some of the structures studied in this paper. When this is the case, the sheet resistivity under a stripe is r_1 while the sheet resistivity between stripes is r_1'.

An important parameter is the current transfer length, L. This is the characteristic length over which, say, current in the bottom film is transferred into the top film at a contact. The TLM is valid if L is greater than the film thicknesses. The theory also reduces to a simple "short contact" limit (used by Shockley) if L>d. Sometimes, however, it is convenient not to restrict d in this way because it is easier to pattern the top film in a coarser geometry than the short contact limit would require.

The resistance measured by the 4-point technique illustrated in Fig. 2 is

$$R_{on} = Z^{-1}[2QC + (n-1)2QT + nlr_1'] \qquad (1)$$

where

$$Q = (\rho_c r_1)^{1/2} \qquad (2)$$

$$T = \tanh(d/2L), \text{ or } L = d/\ln[(1+T)/(1-T)] \qquad (3)$$

$$C = \coth(d/L) = (1+T^2)/2T \qquad (4)$$

$$L = (\rho_c/r_1)^{1/2} \qquad (5)$$

and where we have assumed $r_2 = 0$. Equation 1 is a result of the TLM[1-6]. The terms in the square brackets in Eq. 1 may be interpreted as follows: The first term accounts for the resistance of the stripe contacts on which the probes are placed. Each contact contributes QC. The second term accounts for the contribution of intermediate stripes under which the current must flow. Notice that this term vanishes for adjacent stripes ($n = 1$). The last term accounts for the sheet resistivity of the bottom film between the contacts.

Equation (1) may be rearranged to give

$$ZR_{on} = I + nS \tag{6}$$

If the experimental value of ZR_{on} is plotted against n, a slope S and an intercept I may be determined.

In Eq. 6,

$$I = Q(1-T^2)/T \tag{7a}$$

and

$$S = 2QT + lr_1'. \tag{7b}$$

If r_1' is not assumed to be the same as the sheet resistivity under the top film, but is assumed to be known from a separate measurement (say, a 4-point probe measurement), then Eqs. 7a and 7b are easily solved for T and Q.

On the other hand, if we assume that the bottom film sheet resistivity is the same everywhere ($r_1' = r_1$), then from Eqs. 2 and 5 we have $r_1 = Q/L$. Substitution from Eq. 3 into 7b then gives

$$S = Q\{2T + (\ell/d)\ln[(1+T)/(1-T)]\} \quad (r_1' = r_1) \qquad (7c)$$

The ratio of Eqs 7a and 7b yields an equation which may be solved iteratively for T. Q may then be calculated from Eq. 7a or 7c.

Once T and Q are determined by either method from the experimentally determined I and S, the current transfer length, the contact resistivity, and the sheet resistivity under the contact may be calculated from Eq. 3, and

$$\rho_c = QL \qquad (8a)$$

and

$$r_1 = Q/L. \qquad (8b)$$

In the short contact limit, $L > d$, the relationship between I and S and the desired resistivities reduces to the simple result first used by Shockley[1]:

$$\rho_c = Id/2 \qquad (9a)$$

$$r_1 = S/(l+d). \qquad (9b)$$

This result shows clearly that the slope of the ZR_{on} versus n plot is related the the sheet resistivity of the bottom film while the intercept is related to the contact resistivity.

ZR_{on} versus n plots were measured for each of the film combinations of interest, and values for r_1, ρ_c, and L were calculated using this theory.

3. Experimental

The technique described in section 2 was applied to three types of test vehicle, corresponding to the three kinds of interface described in the introduction.

SFG on Wafer Backs

SFG was patterned by silk screening onto the backs of wafers in an array of 17 3" long stripes. Each stripe is 0.050" wide and the pattern pitch is 0.100". The pattern is shown in Fig. 3. The wafers were then subjected to a standard firing cycle in air. This consisted of a slow 20 min drying ramp from 80°C to 180°C followed by a fast 3.5 minute ramp to 410°C. This final temperature was held for 9 minutes, and then the temperature was ramped to room temperature. The resulting SFG films were 0.036" thick. The manufacturer's data sheet specified a resistivity of 10.3×10^{-6} Ohm cm for films prepared in this way. SFG films were patterned on groups of differently prepared wafers. Two of the groups had the the wafer backs prepared by "sand blasting" (Swam) which produced a surface roughness of 5-10 microns, peak to peak, and two of the groups had their backs prepared by grinding (Disco), which produced a surface roughness of 0.1-0.3 microns, peak to peak. All groups had a very thin Cr film about 25 nm thick, followed by a 1.5 micron gold film deposited in a single pumpdown. One group from each backside preparation was subjected to 370°C for 2 minutes, called a "flash", in air before SFG patterning.

Before measurement, the wafers were cleaved into approximately 1" wide strips as shown in Fig. 3 to produce SFG stripes 1" long. We found that if measurements were done on whole wafers, the ZR_{on} vs n plots had a pronounced curvature. To facilitate the electrical measurements, a probe card was used in conjunction with a 40-pin Keithley parametric tester. The probe card had 15 pairs of probes configured so that 2 probes fell on each of 15 stripes of the pattern shown in Fig. 3. Resistances between every possible pair of stripes accessed by the probe card were measured. Thus, 14 adjacent pairs of stripes, 13 pairs with one stripe between, and so on, were measured. Means and standard deviations for each stripe separation were computed. Typical experimental data is plotted in Fig. 4. Measurements on bare wafers (Swam or Disco, but no chrome or gold) were attempted, but the contacts were not ohmic so contact resistivities could not be determined.

SFG on Cavity Metal

SFG was patterned and cured on 1"x2" metallized alumina blanks in exactly the same way as the wafers were patterned. See Fig. 3.

Two groups of metallized blanks were used: One group had cavity metallization of 220 microinches of gold, while the other had 740 microinches of silver.

We used the same data acquisition and analysis software as was used for the patterned wafers. Typical experimental plots are shown in Fig. 5.

Jumper Chips on SFG

This is different from the case of the wafers and the cavity metal because SFG is the substrate, not the top film. A wafer with a non-conducting surface was sawed on tape (100% saw-through), and without removing the tape, an array of C-shaped SFG patterns was silk-screened onto the dice. As the dice were removed from the tape, jumper chips were placed by tweezers into the wet SFG in the pattern shown in Fig. 6. The dice were then attached to a CERDIP cavity using the same SFG for die attach. The units were cured, wire-bonded, and sealed to produce the structures shown in Fig. 6. The SFG trace was 0.020" wide. The jumper chips are 0.02" square and 0.01" high, alloy 42, clad on top with aluminum, and on the bottom with an alloy of 3% silicon in gold. For comparison with a standard process, we also made similar measurements for jumper chips attached by a gold-eutectic alloy.

Electrical measurements were made by socketing the package. The same analysis was used as for the wafers and the cavity metal, but different physical dimensions were used. After the as-processed electrical measurements, the jumper chips were subjected to bakes at 175°C and 300°C, and electrical readouts were made after various times. Typical resistance data is shown in Fig. 7.

4. Results and Discussion

For the wafers, the data could not be analyzed without assuming that the sheet resistivity of the film under the SFG was different from the resistivity of the bare film. We used separate 4-point probe measurements to determine the sheet resistivity of the bare gold films. For the measurements on cavity metal and jumper chips we could assume that r_1 and r_1' were the same. The results of analysis of data like Figs. 4, 5, and 7 are given in Table I.

When jumper chips were baked at 175°C and 300°C, the contact resistivity varied as shown in Fig. 8. The constant slopes in Fig. 7 show that the sheet resistivity of the underlying SFG does not change. Under the same conditions, the contact resistivity of a jumper chip-gold eutectic interface was constant at 2 micro-ohm cm^2.

It is interesting to note the values of L/d in the right hand column of Table I. Conditions for the simple short-contact analysis (Shockley-type, L >> d) clearly do not hold.

There are no adverse practical consequences of the results in Table I. A calculation of the total resistance between the front of the die and the cavity metal using these contact resistivities, as well as the bulk resistivities of the silicon and the SFG shows that the bulk resistivity still dominates. This is also true for the jumper chip. Although the jumper chip contact resistance to SFG is 6 to 14 times the contact resistance to gold eutectic, it is still a negligible fraction of the total resistance from the top of the jumper chip to the bulk of the SFG.

Acknowledgments

Thanks are due to Jeanie Vierra, Helen Simmons, and Mike Kish for their help with processing and electrical measurements.

References

1. W. Shockley, Appendices B and C in Technical Report No. AL TDR 64-207, "Research and Investigation of Inverse Epitaxial UHF Power Transistors," Air Force Avionics Laboratory, Research and Technology Division, Air Force Systems Command, Wright-Patterson AFB, September, 1964.

2. H. H. Berger, Solid-State Electron., Vol. 15, pp145-158 (1972).

3. H. Murrmann and D. Widman, Solid-State Electron., Vol 12, pp879-886 (1969).

4. H. Murrmann and D. Widman, IEEE Transactions on Electron Devices, Vol. ED-16, pp1022-1024 (1969).

5. I. F. Chang, J. Electrochem. Soc., Vol. 117, pp368-372 (1970)

6. G. K. Reeves and H. B. Harrison, IEEE Electron Device Letters, Vol. EDL-3, pp111-113 (1982).

TABLE I

Interface(1)	Sheet Res. Under Contact (Ohms/sq)	Sheet Res. Bare (Ohms/sq)	Contact Res. (Ohm cm^2)	L/d
SFG-DG (2)	5.2±0.4	7.3 x10^{-2}	2.2±0.2 x10^{-2}	0.54
SFG-DGF (2)	2.8±1.6 x10^{-1}	1.77 x10^{-1}	1.2±0.1 x10^{-3}	0.55
SFG-SG (2)	1.9±0.1	1.64 x10^{-1}	3.0±0.3 x10^{-3}	0.32
SFG-SGF (2)	9.9±5.9 x10^{-1}	2.73 x10^{-1}	1.2±0.9 x10^{-2}	0.91
SFG-CG (3)	5.1±0.9 x10^{-3}	5.1±0.9 x10^{-3}	1.2±0.2 x10^{-4}	1.22
SFG-CS (3)	1.4±0.3 x10^{-3}	1.4±0.3 x10^{-3}	2.9±0.8 x10^{-5}	1.15
JC-SFG (3)	1.6±0.2 x10^{-3}	1.6±0.2 x10^{-3}	1.2±0.2 x10^{-5}	1.83
JC-AUEU (3)	2.3±0.2 x10^{-4}	2.3±0.2 x10^{-4}	1.9±0.1 x10^{-6}	1.78

Notes:

1. Code: TOP-BOTTOM, SFG = silver-filled glass, DG = Disco gold, DGF = Disco gold flashed, SG = Swam gold, SGF = Swam gold flashed, JC = jumper chip, AUEU = gold eutectic, CG = gold cavity, CS = silver cavity.

2. Bare film sheet resistivity was determined from separate 4-point probe measurement.

3. Bare film, and film under contacts are assumed to have the same sheet resistivity.

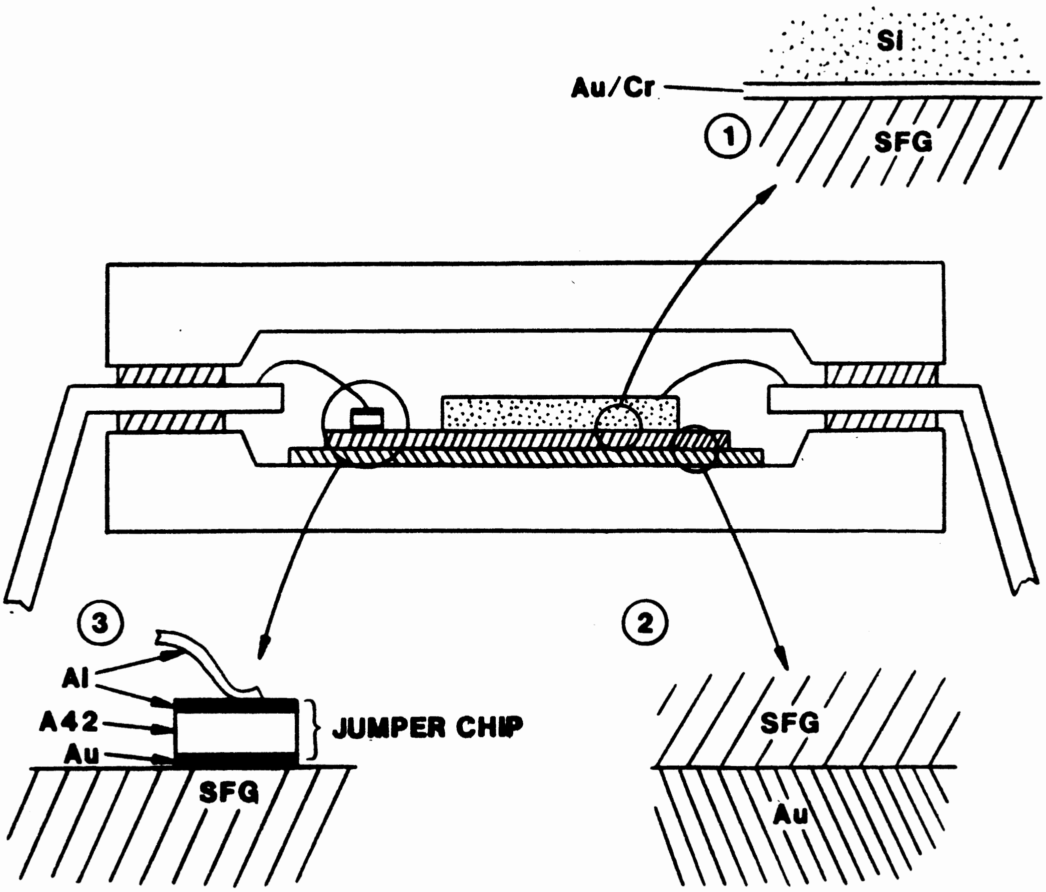

Fig. 1. Cross section of CERDIP package showing the three interfaces between SFG and other conductors.

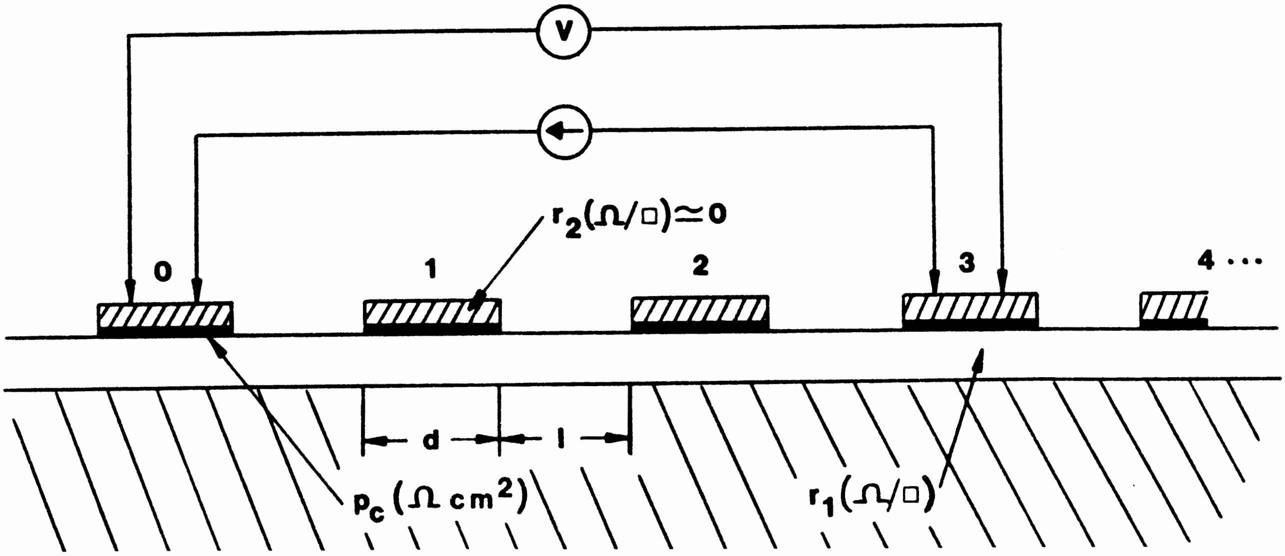

Fig. 2. Cross section of contact resistivity measurement test structure. Width of stripes (into page) is Z. For the case shown, the measured 4-point resistance is R_{03}.

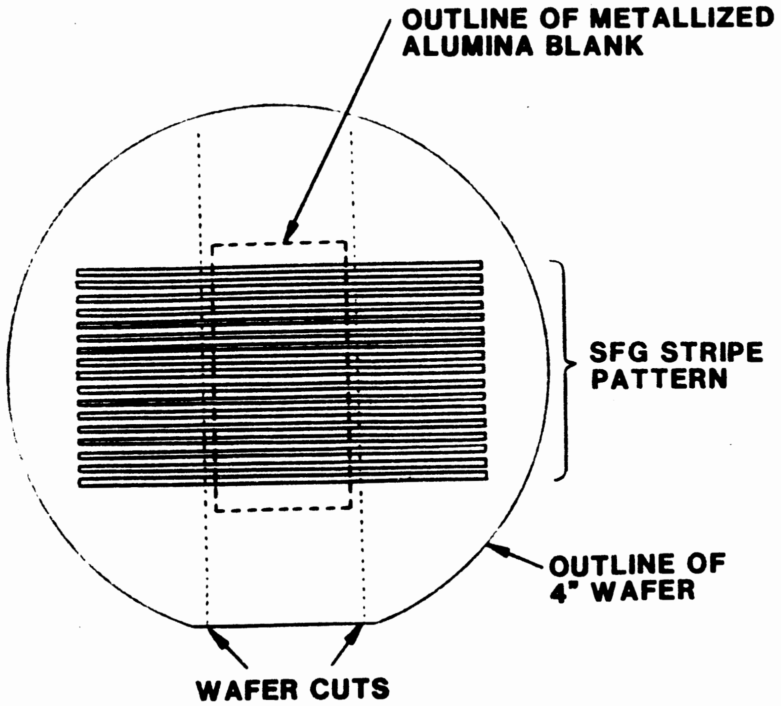

Fig. 3. SFG stripe pattern printed either on wafer backs or on metallized ceramic substrates. Stripes are 0.050" wide, and the pitch of the pattern is 0.100".

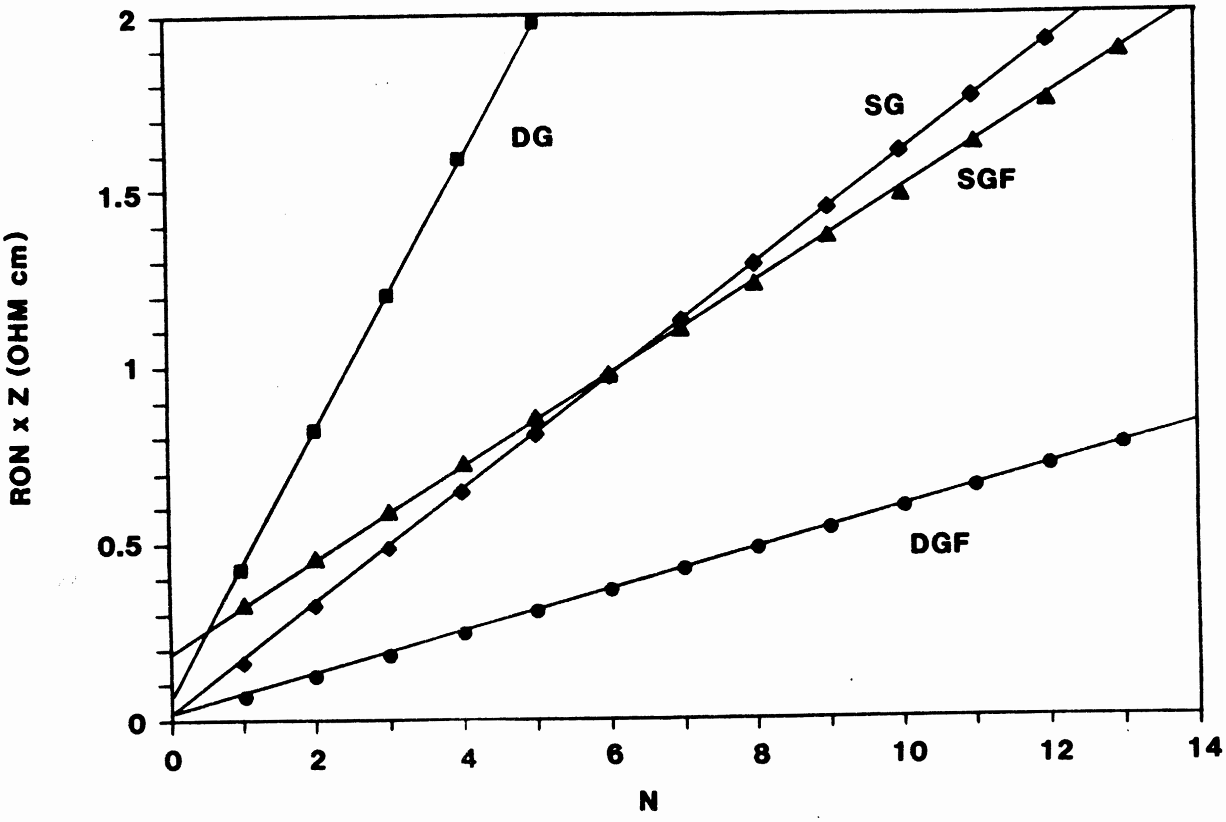

Fig. 4. Typical resistance data for SFG contacts to gold-coated wafer backs. DG is Disco-gold, SG is Swam-gold. DGF and SGF are the corresponding cases with an additional heat treatment ("flash") before application of SFG. The test pattern in Fig. 3. was used.

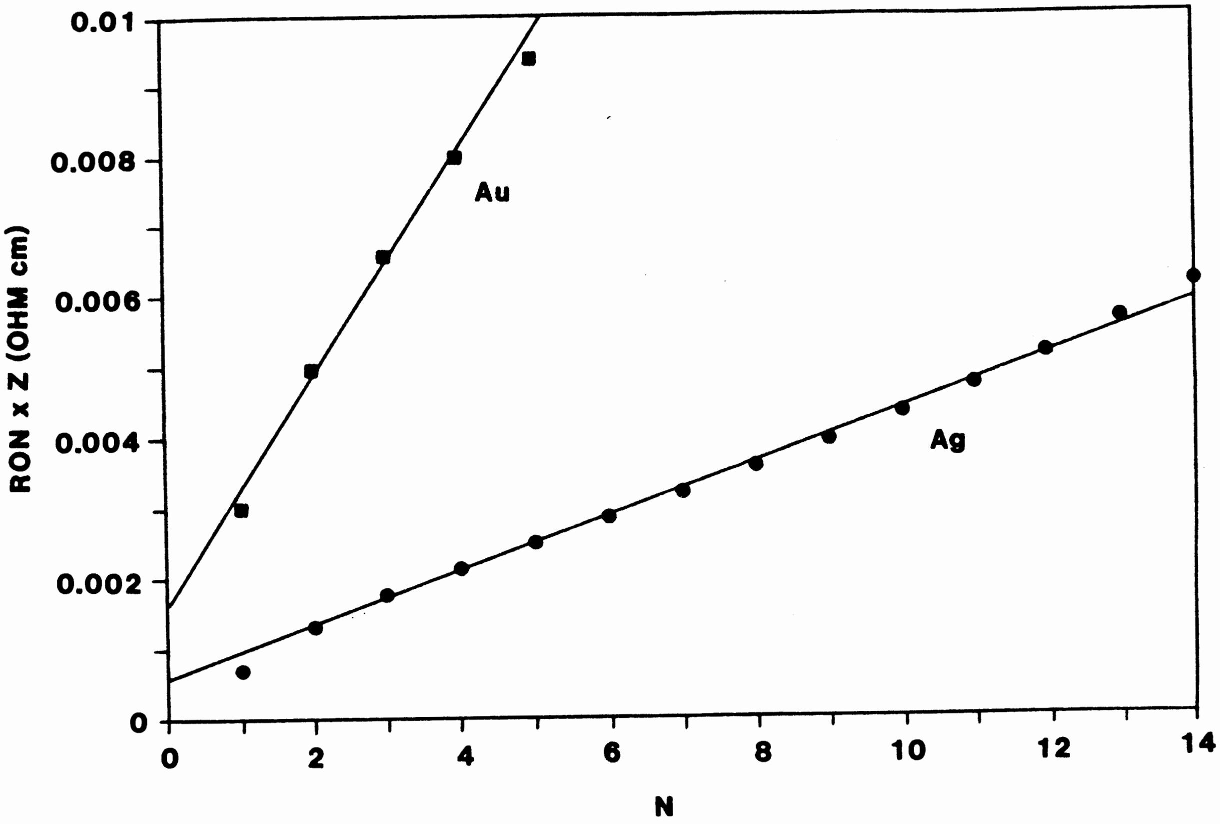

Fig. 5. Typical resistance data for SFG contacts to gold or silver cavity metallization on alumina substrates. The test pattern in Fig. 3. was used.

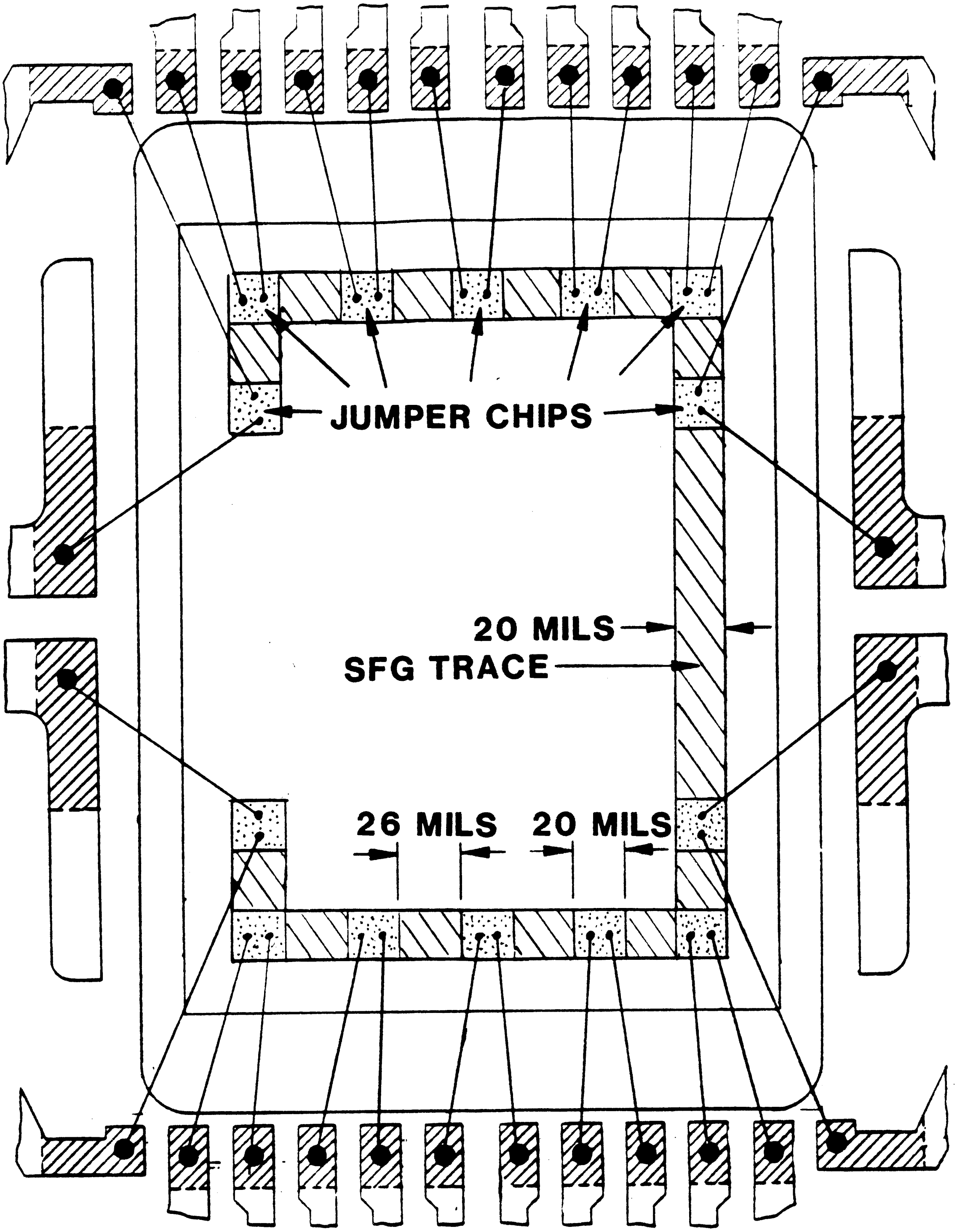

Fig. 6. Regularly-spaced jumper chips attached to a C-shaped SFG pattern on non-conductive silicon chip. The chip was mounted by SFG in a CERDIP package. Each jumper chip has two aluminum wires attached to enable 4-point resistance measurements.

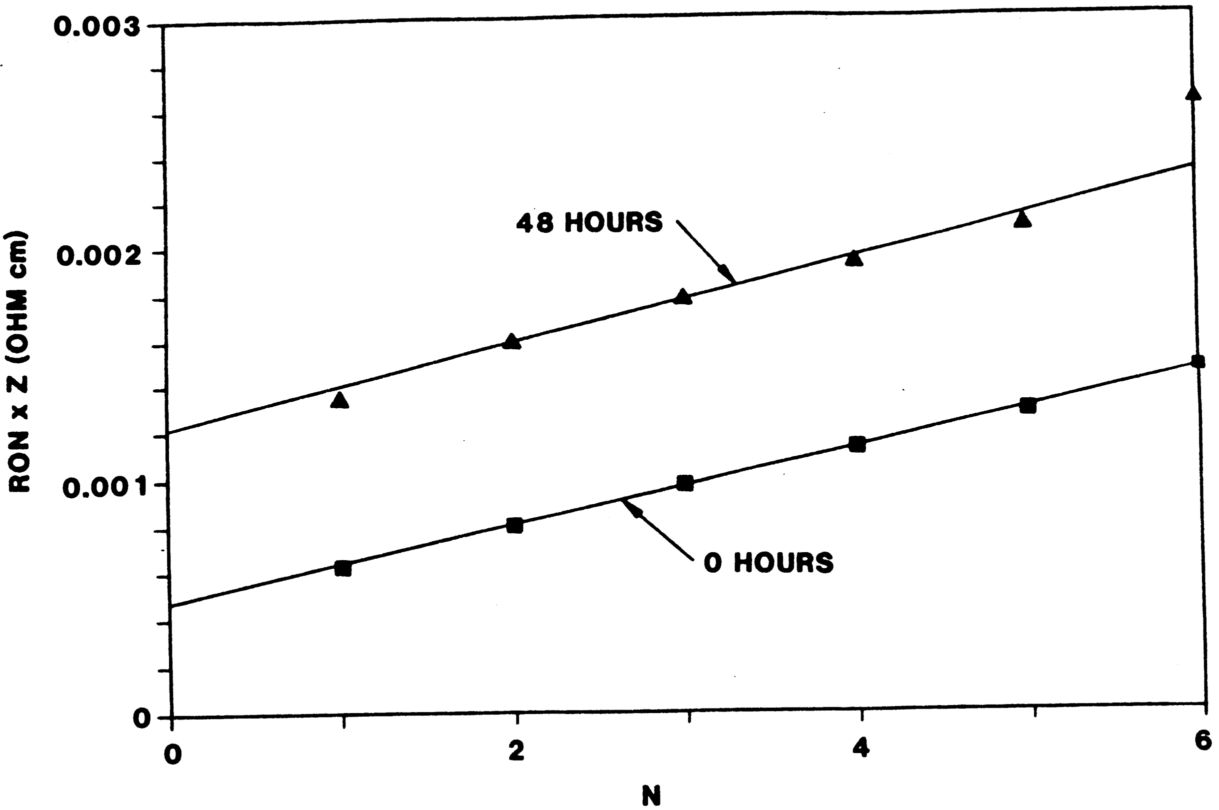

Fig. 7. Typical resistance data for jumper chips on SFG, using the test pattern in Fig. 4. Comparison of data before and after 48 hours of air bake at 300°C shows an increase of contact resistivity, but not sheet resistivity.

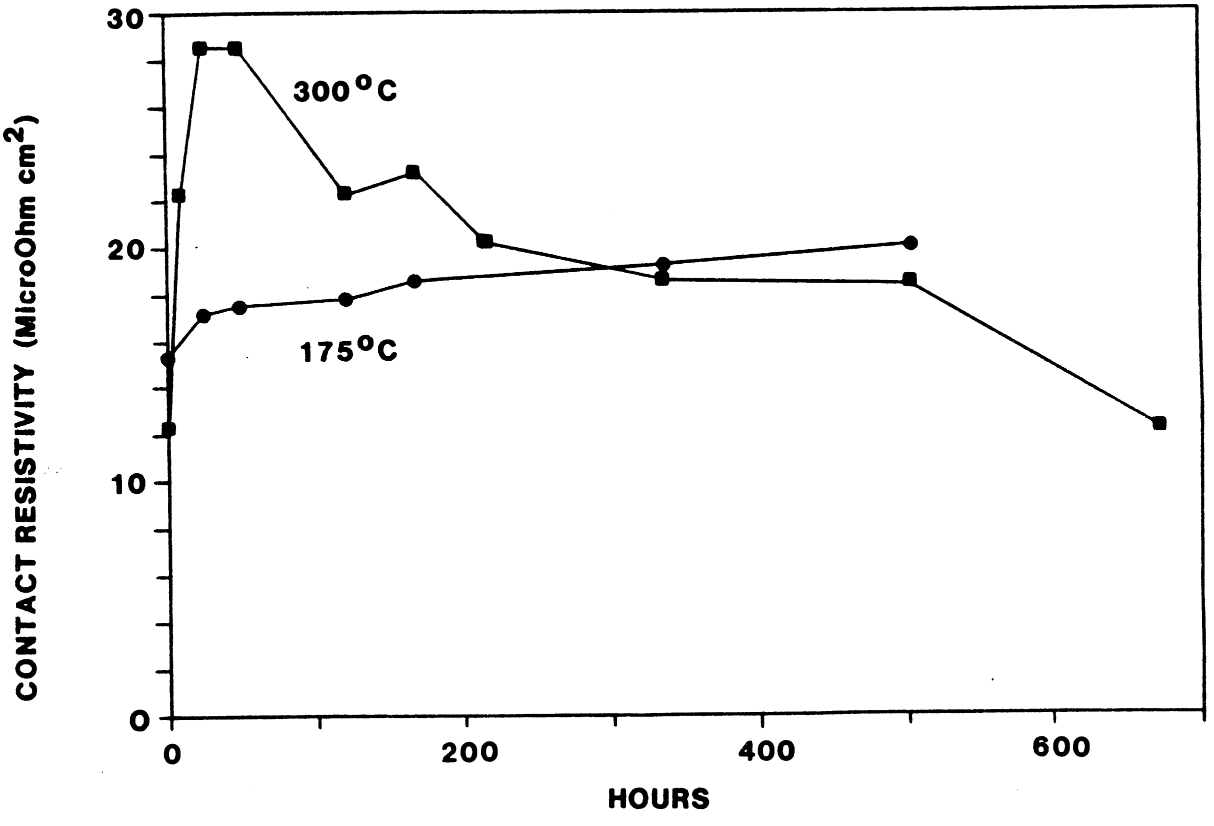

Fig. 8. Contact resistivity of jumper chip to SFG as a function of time and temperature in air.