# THIN-FILM CRACKING AND WIRE BALL SHEAR IN PLASTIC DIPS DUE TO TEMPERATURE CYCLE AND THERMAL SHOCK

C. G. Shirley and R. C. Blish II

Intel Corporation

## ABSTRACT

A test chip was used to compare thin film cracking of various circuit layouts at various positions on the chip, and to study wire ball shear. Slotted aluminum busses reduced thin film cracking in die corners. Thin film cracking and wire ball shear failure rates have remarkably different dependence on shock versus cycle and on lead frame material.

## 1. INTRODUCTION

Plastic-encapsulated silicon chips are susceptible to mechanical stress-induced failures due to plastic cracking, die cracking, thin film cracking, and/or wire problems. These failure modes result from thermal coefficient of expansion (TCE) mismatch among the materials of the package: copper or Alloy 42 lead frame, silicon chip, and silica-filled epoxy molding compound. Stress-related problems become more severe as die sizes increase. Failure can occur during any of the thermal excursions to which the package is subjected during its manufacture (eg. thermal shock during solder dipping), subsequent assembly operations (eg. wave solder immersion during board assembly), and final application. The major accelerated stress tests used to gauge the susceptibility of a packaged chip to these thermomechanical mechanisms are thermal shock (T/S, liquid-to-liquid) and temperature cycle (T/C, air-to-air).

Passivation cracking is known to occur near corners of plastic-encapsulated dice which have been subjected to T/C and T/S. The cracking is caused by shear stresses which tend to displace raised areas of passivation. The displacements are in the direction of the center of the die. This mechanism has been studied by measuring deformation of metallization on unpassivated dice.[1,3] It is interesting that passivation covering narrow aluminum lines is more resistant to cracking than passivation covering wide busses. Okikawa et al.[2] provided an explanation for this.

Passivation cracking by itself does not cause functional failure of the die. However, functional failure can be caused by cracking of polysilicon structures in association with cracking of overlying passivation. Specifically:

- o Cracking of polysilicon occurs where it emerges from under an aluminum sheet, if the point of emergence is near the corner of the die.
- o The polysilicon, and the overlying passivation, is more likely to crack if the aluminum sheet is greater than 50 microns wide.
- o Polysilicon cracking is a secondary effect of passivation cracking in which a passivation crack propagates into the underlying polysilicon layer.

At Intel, a test chip was designed which incorporates polysilicon resistors in proximity to metal lines and contacts with systematic variations of spacing and pitch. The polysilicon resistors are placed so that they are likely to crack when the passivation cracks. The polysilicon resistors can be thought of as electrically-measurable thin-film cracking detectors. A count of open "cracking-sensitive" polysilicon resistors indicates the extent of thin-film cracking.

Ball bonds in the corners of a plastic-encapsulated die tend to shear in T/S and T/C. We noticed that the occurrence of shearing is correlated with a resistance increase of the bond. The test chip incorporates two bond pads connected by an aluminum bus. A circuit was made by bonding wires to each end of this bus. The weakest links in this circuit were the two ball bonds. Thus a count of high-resistance "wire-bus-wire" resistors indicates the extent of wire ball bond shear.

This paper describes an experiment in which electrical signals from the test chip were used as indications of thin-film cracking and wire-ball shear. These indications, in turn, were used to study factors influencing thin film cracking and wire ball shear occurring in T/S and T/C in plastic-encapsulated devices. Section 2 describes the pertinent features of the test chip. Section 3 covers the experimental design. The results are presented in Section 4, and are discussed in the final section.

## 2. THE TEST CHIP

The test chip is manufactured using an all projection mask n-well CMOS process. The wafer is covered by an array of 36 mil square modules as shown in Fig. 1 (aluminum level only). The repeat unit stepped across the wafer is shown in Fig. 2. This repeat unit is a 3x3 array of "cells". The experiment utilizes only the cells labelled 1 through 8. Cell number 9 was not utilized in this experiment. The cracking-sensitive polysilicon line used in this experiment meanders back and forth under the edge of the aluminum bus as shown in Fig. 3. The aluminum bus resistors used to create the ball-shear sensitive wire-bus-wire resistors are also shown in Fig 3. Cells 1 through 8 all have the same equivalent circuits, but

CH2388-7/87/0000-0238$01.00 © 1987 IEEE/IRPS

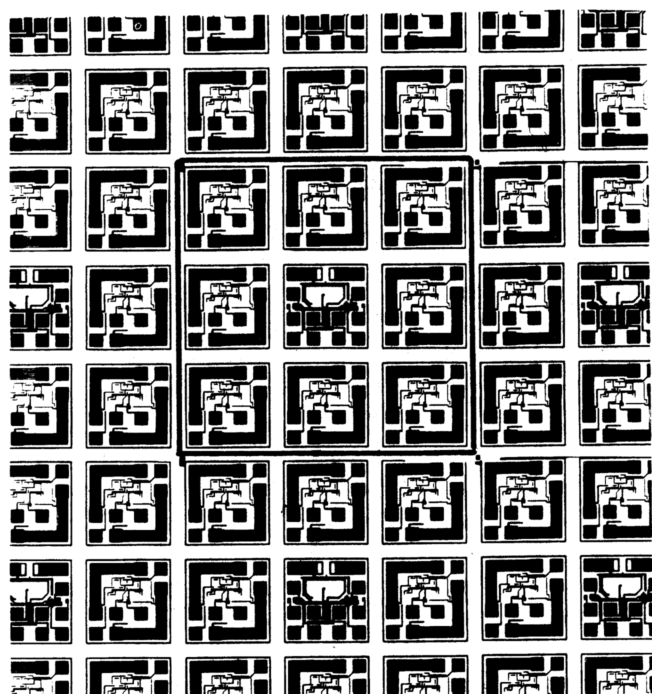

Fig. 1. Array of 36 mil square test chip cells. The 3x3 repeat unit is outlined.

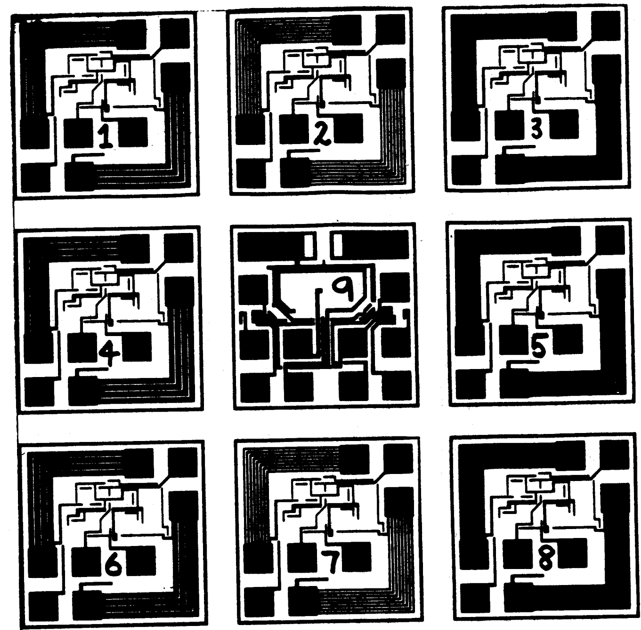


Fig. 2. Aluminum level of repeat unit of test chip. Numbers label cells.

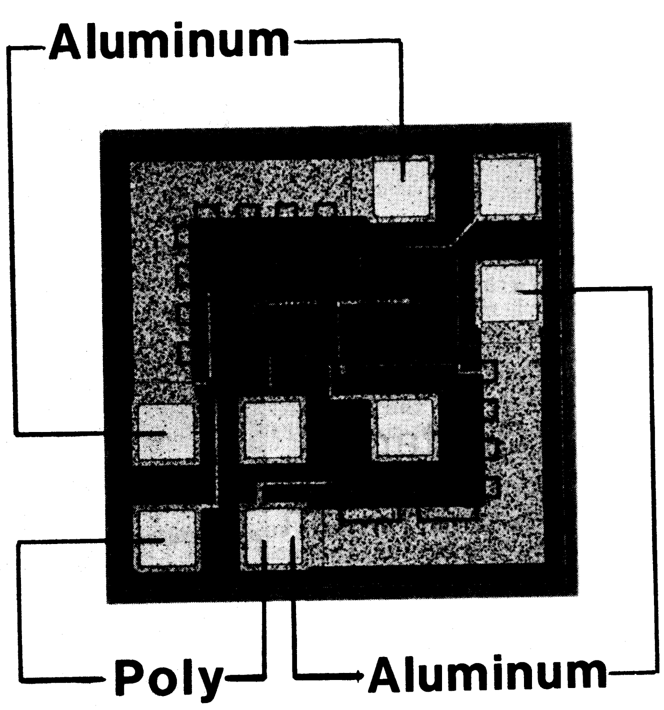


Fig. 3. Detail of cell number 3 showing the polysilicon resistor and the aluminum bus resistors used in the experiment. Pads used to access resistors are indicated.

differ in the layout of the aluminum bus, and the presence or size and pitch of arrays of contacts of aluminum to substrate. These differences are detailed in Fig. 4. The dimensions and pitches of the aluminum busses and contact arrays are given in Table I.

TABLE I. DIMENSIONS OF TEST CHIP STRUCTURES (MICRONS)
Subdie unit pitch = 914 microns (36 mils)

| | Aluminum Bus | | Contacts | |
|---|---|---|---|---|
| Cell No. | Pitch | Width | Pitch | Size |
| 1 | 28 | 21 | None | None |
| 2 | 14 | 7 | None | None |
| 3 | Sheet | 105 | None | None |
| 4 | 28 | 21 | 28 | 17 |
| 5 | Sheet | 105 | 28 | 17 |
| 6 | 28 | 21 | 14 | 3 |
| 7 | 14 | 7 | 14 | 3 |
| 8 | Sheet | 105 | 14 | 3 |

## 3. EXPERIMENTAL DESIGN

The objective of this experiment is to study thin film cracking and wire ball shear as a function of the following variables:

1. Aluminum layout and contact arrangement. Eight arrangements, specified by cell number, were studied. These are shown in Fig. 4.

2. Copper versus Alloy 42 lead frames.

3. Location on the die.

4. Thermal shock (T/S) versus temperature cycle (T/C), condition C.

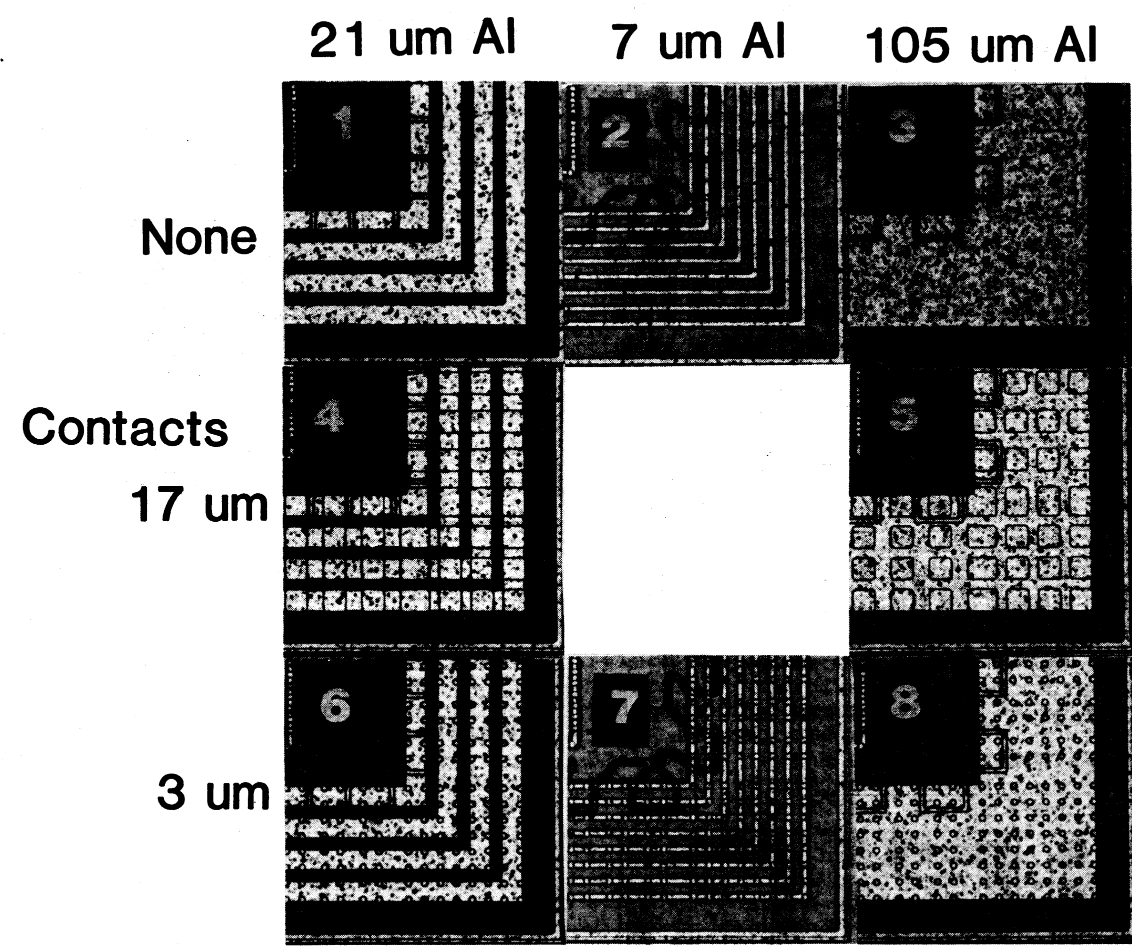


Fig. 4. Corner detail of cells used in the experiment. Aluminum bus width varies by column, contact size and pitch varies by row. Dimensions are given in Table I.

5. Condition B ($-55^{o}C$ to $125^{o}C$) versus condition C ($-65^{o}C$ to $150^{o}C$) for T/C only.

6. Number of cycles of shock or cycle.

The experiment can be discussed in three parts: The assembly matrix, the environmental matrix, and electrical test.

<u>Assembly Matrix</u>

When the 3x3 repeat unit is stepped across the entire wafer, a pattern such as shown in Fig. 5 is generated. The numbers in Fig. 5 correspond to the cell numbers in Fig. 2. The wafers were cut into 252 mil square dice as shown in Fig. 5. Since the 7x7 (units of 36 mil modules) dice so produced are incommensurate with the 3x3 repeat unit, 9 distinct die variants are produced. Each die variant may be recognized by the cell number of the cells which occur in all four corners (and centers of the edges) of the die. After sawing, the dice were visually sorted into 9 groups, each corresponding to a die variant. Half of each group were bonded to copper lead frames and half were bonded to Alloy 42 lead frames. A silver-filled polyimide adhesive was used for the die bonding. The copper and the Alloy 42 pieceparts are geometrically identical 40-lead 600 mil silver spot-plated lead frames.

| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |
| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |
| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |
| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |
| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |
| 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 | 3 | 1 | 2 |
| 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 | 5 | 4 | 9 |
| 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 | 8 | 6 | 7 |

Fig. 5. Schematic of wafer sawing pattern. Equal numbers of each possible die variant are produced.

Wire bonding for all dice was done according to the same bonding diagram, irrespective of die variant. The diagram is shown in Fig. 6 (for variant 8). The frames were molded in epoxy molding compound, dejunked, trimmed and formed, and solder-dipped. The die variant number and lead frame material were marked on the packages.

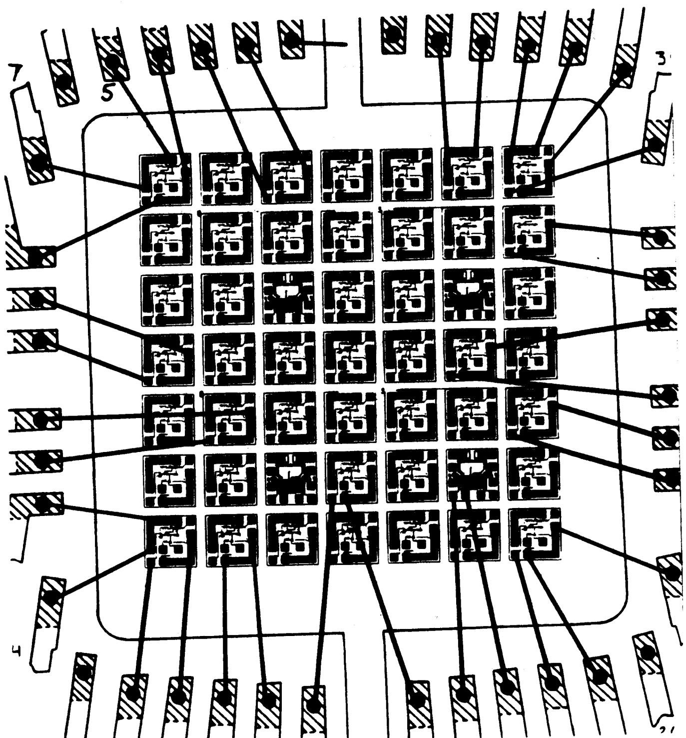


Fig. 6. Bonding diagram used in the experiment. Die variant 8 shown. All die variants used the same wire bond pattern.

There are 18 assembly splits for this experiment (9 variants x 2 lead frame materials). Inclusion of each of the nine possible die variants ensures that each cell number is sampled at each of the monitored locations on the die. For example, for die variant 2, layout number 2 occurs at (1,1), (7,1), (7,7), (1,7), (1,4), (4,1), (4,7), (7,4), and (4,4) while cell number 7 occurs at (1,2), (4,2), (7,2), (7,5), (4,5), and (1,5). However, on die variant 9, layout 2 occurs at sites (1,2), (4,2), etc.

Environmental Matrix

Each of the 18 assembly splits consisted of 28 electrically perfect units. Each of these assembly splits was divided into two groups. The first group (18 assembly splits of 14 units each) was subjected to temperature cycle only, half at condition B and half at condition C with readouts at 0, 100, 200, 500, and 1000 cycles. The second group was subjected to condition C only, half subjected to T/S and half subjected to T/C with readouts at 0, 5, 10, 15, 20, 30, 40, 50, 60, 80, 100, 150, 200, 250, 300, 400, 500, 700, and 1000 cycles. Pieces with failed resistors were not removed from the groups. This maintained the sample size for other unfailed resistors.

Electrical Test

Electrical test consisted of monitoring polysilicon resistors at the 12 locations on the die shown in Fig. 7, and the 6 wire-bus-wire resistors at locations shown in Fig. 8. Locations on the chip are specified by coordinates. For example, the cell in the lower left corner of the die is (1,1), the cell in the upper left corner is (1,7), and so on. Because cell number 9 has a different equivalent circuit from the other subdice, and is not used in this experiment, data from any monitored site which has a cell number 9 on it is ignored and is not included in the statistics. The nominal as-assembled value of the aluminum resistors ranges between 0.6 and 1.2 Ohms, depending on the layout number. A measured aluminum resistor was considered "open" if it rose above 10 Ohms. The nominal value of the polysilicon resistors is 22K Ohms. If it rises above 35K Ohm it is called "open".

4. RESULTS

The results of the experiment are most conveniently discussed in two sections: Wire Opens, and Poly Opens. Wire Opens refer to opens of the wire-bus-wire resistor monitored at 6 sites on the die. Poly Opens refer to opens of the polysilicon resistor, Fig. 3, monitored at 12 sites on the die.

Wire Opens

The bonding diagram shown in Fig. 6 has 6 two-terminal "devices" in which pins are connected to each other through gold wires and an aluminum bus only. For example, pins 5 and 7 in Fig. 6 are connected to pads which are directly connected to each other via an aluminum bus. Damage to the wire bonds shows up as an increased resistance between pins wired in this way, independent of other failure mechanisms such as thin film cracking.

Cumulative failure statistics for wire-bus-wire opens (> 10 ohms) are shown in Figs. 9 and 10. The particular variant had no effect, so the data from all variants was consolidated in these figures. In the figures, the monitored sites are differentiated by the fill patterns of the sub-bars.

Figure 9 gives data for T/C condition B (left graphs) and T/C condition C (right graphs), and it compares the effect of Alloy 42 (top graphs) with that of copper (bottom graphs). Figure 10 compares T/C condition C (left graphs) with T/S condition C (right graphs), and it compares the effect of Alloy 42 lead frames (top graphs) with the effect of copper lead frames (bottom graphs).

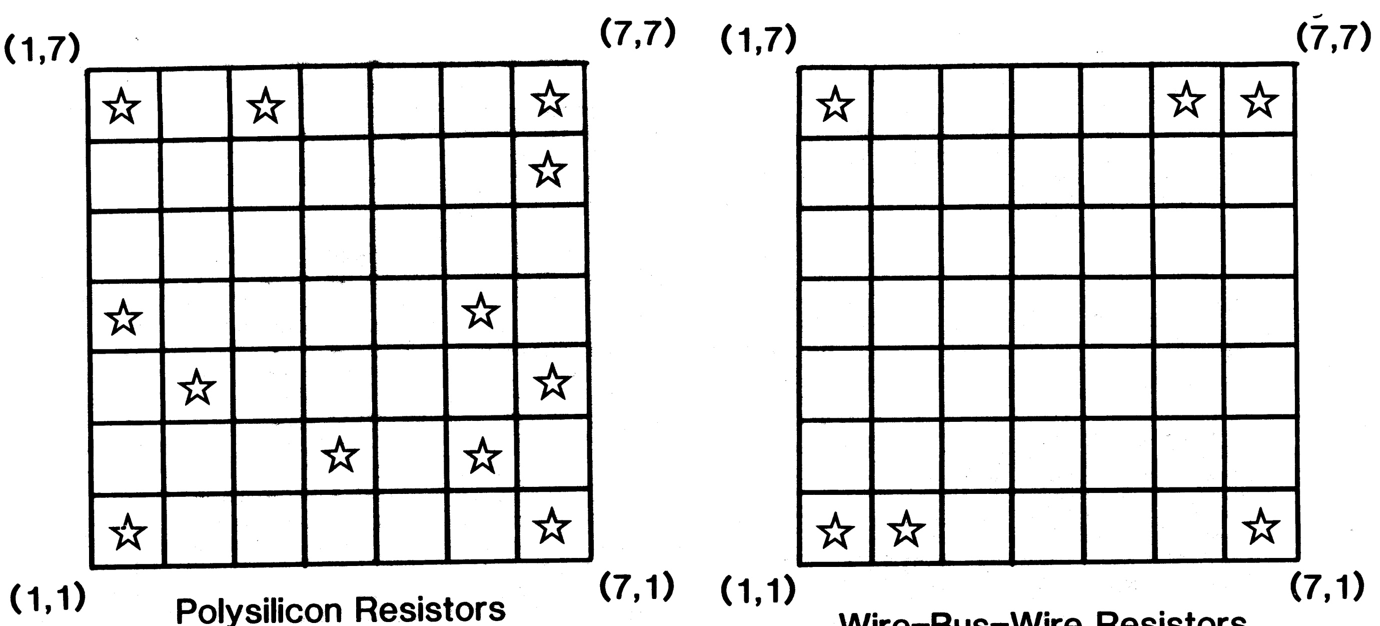


Fig. 7. Sites on die where polysilicon resistors are monitored. Orientation matches Fig. 6.

Fig. 8. Sites on die where wire-bus-wire resistors are monitored. Orientation matches Fig. 6.

Location key: 11 21 71 77 67 17

T/C Condition B
Alloy 42

T/C Condition C
Alloy 42

T/C Condition B
Copper

T/C Condition C
Copper

Cum % Fail
30
0
30
0

50 100 200 500 1K 50 100 200 500 1K
Cycles

Fig. 9. Wire-bus-wire opens in T/C condition B (left graphs) and T/C condition C (right graphs). Bar shadings indicate sites on die. Site (7,7) has the highest failure rate.

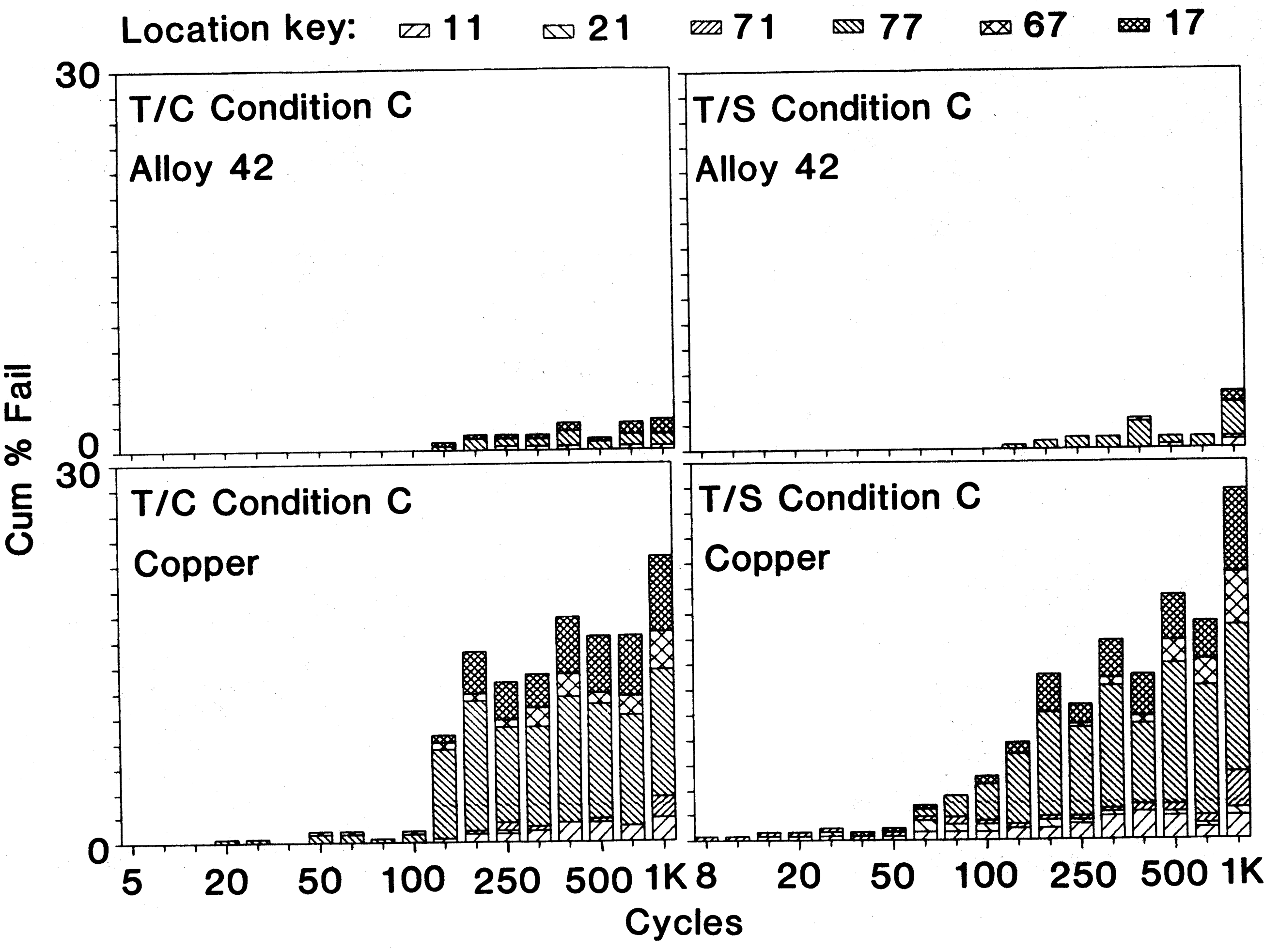


Fig. 10. Wire-bus-wire opens in T/C condition C (left graphs) and T/S condition C (right graphs). Bar shadings indicate sites on die.

---

Figure 11 is a general view of corner modules showing bonds which required zero pull force to remove the ball bond. These bonds all had resistances between 10 and 100 ohms. In each corner module shown, a typical failed bond is indicated by a circle and is shown in more detail in Fig. 12. The morphology of all fracture surfaces has a definite orientation relative to the location of the center of the die. This direction is shown by the large arrows in Fig. 12. Many of the failed bonds showed fracture in the silicon. This mechanism will be identified as Corner Ball Shear (CBS).

Observations about CBS, based on Figs. 9, 10, 11 and 12 may be summarized as follows:

- Copper lead frames have a much greater incidence of CBS than do Alloy 42 lead frames.
- For a given temperature amplitude, T/S and T/C do not cause significantly different failure rates.
- The acceleration from T/C condition B to T/C condition C is about 1.7 at 500 and 1000 cycles.
- CBS is confined to corner modules, with failure at one corner, (7,7), dominating the failures.
- Failure analysis confirms a correlation between an "open" (> 10 Ohms) and zero pull strength, with fracture often occurring in the silicon.

Detailed examination of the distribution of resistances of the wire-aluminum bus-wire devices shows that the initially narrow symmetrical distribution becomes more skewed towards higher resistances as the number of cycles increases. But no resistance ever exceeded 100 ohms. Typical "open" resistances due to ball shear were 20 to 50 Ohms.

Poly Opens

The device used to detect polysilicon opens is the resistance between the pads indicated in Fig. 3. This resistance includes the resistance of gold/aluminum bonds which are likely to be sheared based on the observations above. This polysilicon resistor has a nominal resistance of about 22K ohms and is considered open if the

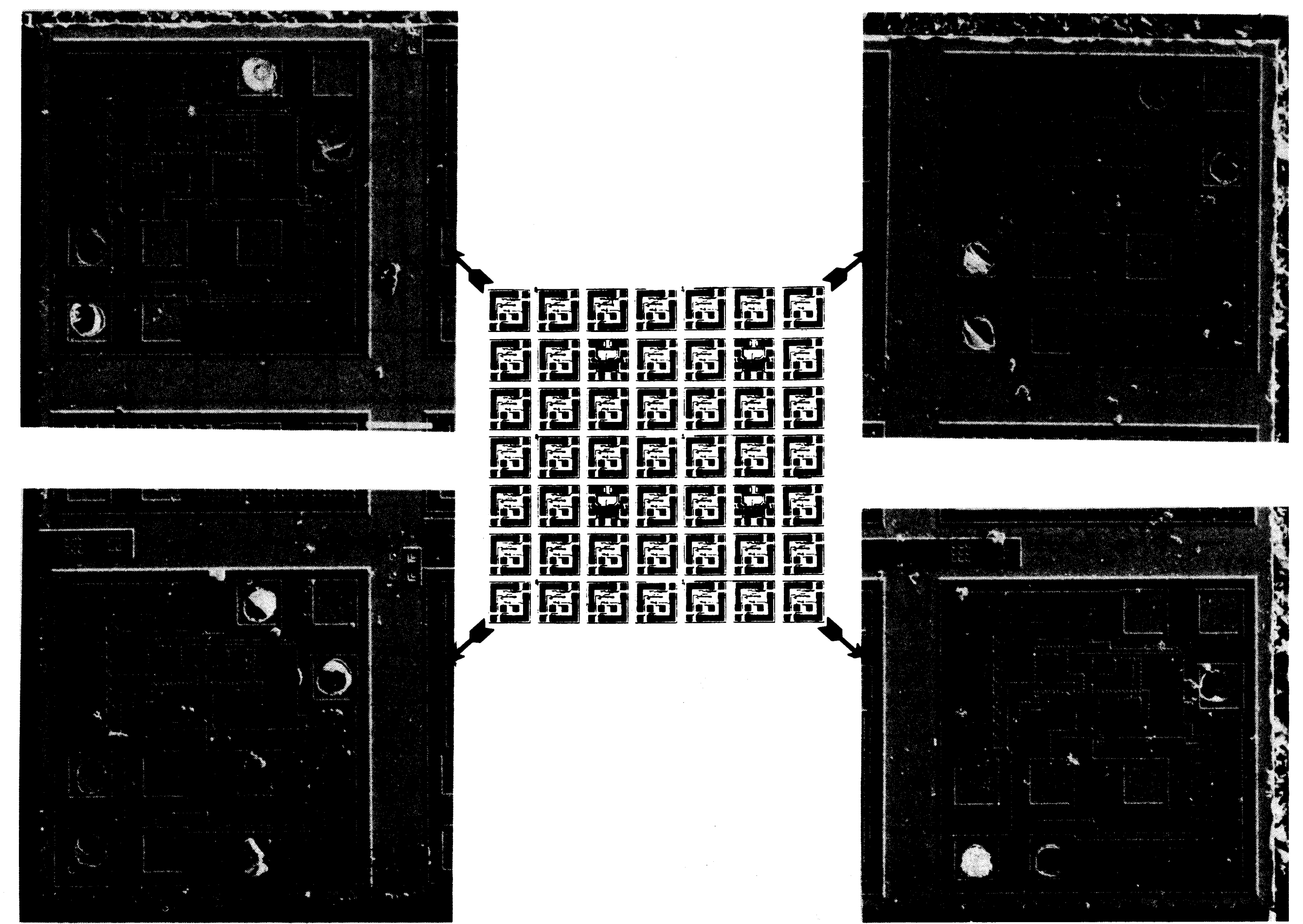

Fig. 11. Corner cells of a stressed die showing sheared bonds. Unit was variant 3 with copper lead frame, and has undergone 1000 cycles of T/C condition C.

resistance measured between package pins exceeds 35K ohms. It is important to recognize that since no wire-aluminum bus-wire device resistance ever exceeded 100 ohms, a wire "open" cannot hide a polysilicon interconnect "open". The electrical indication of thin film cracking is electrical continuity of polysilicon resistors monitored in 12 locations on each die and sampling 8 different circuit layouts in each location.

In T/C the dominant failure locations were sites (1,7) and (7,1). Examination of the corner modules in Fig. 6 shows that the orientation of the aluminum busses is such that the crack-sensitive polysilicon resistor will be closer to the corner of the die for sites (1,7) and (7,1) than for sites (1,1) and (7,7). Passivation cracking indicated by open polysilicon resistors and localized to the die corners, particularly (1,7) and (7,1) will be identified as Corner Passivation Cracking (CPC). Sites (1,7) and (7,1) of variant 3 devices usually had passivation cracks which intersected the polysilicon resistor as shown in Fig. 13. It was not possible to verify unambiguously that the crack was associated with the high value of the polysilicon resistance, but the correlation with variant 3 and sites (1,7) and (7,1) strongly suggests that this crack is at least part of the CPC mechanism. We shall use plots of the total number of failures at (1,7) and (7,1) in Figs 14 and 15 to draw conclusions about the effects of the independent variables (Cu vs Alloy 42, dependence on circuit layout, etc.), and to compare different mechanisms. The graphs in Fig. 14 compare the effect of T/C condition B (left graphs) with the effect of T/C condition C (right graphs) for Alloy 42 lead frames (top graphs) and copper lead frames (bottom graphs). The dominant failure mode in T/C is CPC, so study of Fig. 14 leads to the following observations about CPC:

- Copper lead frames have only a slightly higher failure rate than Alloy 42 lead frames.
- Most failures occur in extreme corners of the die at locations (1,7) and (7,1), but not at (1,1) and (7,7).
- Circuit layout number 3, Fig. 4, has the highest failure rate. Layouts 5 and 8 have the next highest failure rate. The other layouts, all with slotted aluminum busses have a much lower failure rate.
- T/C condition C is an acceleration of T/C condition B by a factor of 1.5 to 3, depending on the number of cycles.

Fig. 12. Detail of bond shear at pads indicated by circles in Fig. 11. Fracture surfaces are oriented relative to die center (direction indicated by large arrows).

---

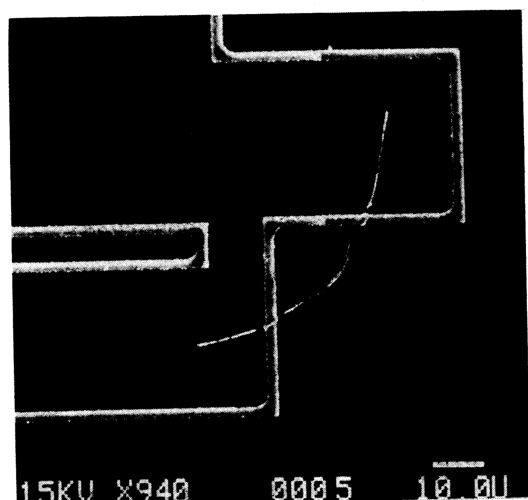


Fig. 13. Typical passivation crack intersecting the polysilicon resistor. Site (7,1) of variant 3 copper lead frame device after 1000 cycles of T/C condition C. Passivation, aluminum, and LTO have been removed.

- The first failures occur at 15 or 20 cycles. After 50 to 100 cycles most of the failures that are going to occur, have occurred.
- After 150 cycles some formerly open devices fall back into the pass window, indicating an apparent "healing" effect.

The effects of T/C and T/S are compared in Fig. 15. The left graphs are a confirmation of the data shown in Fig. 14 (right graphs), but at more closely spaced readouts. The right graphs in Fig. 15 shows that T/S is more complicated than T/C because an additional mechanism not observed in T/C starts to dominate the failures after 150 cycles. This additional mechanism is not confined to the corners of the die, and will be identified as Distributed Passivation Cracking (DPC). This is shown by the site maps, Fig. 16, of failures when CPC is the dominant poly-open mechanism (left graphs), and when DPC is dominant (right graphs). The data shown in Figs. 15 and 16 leads to the following additional observations:

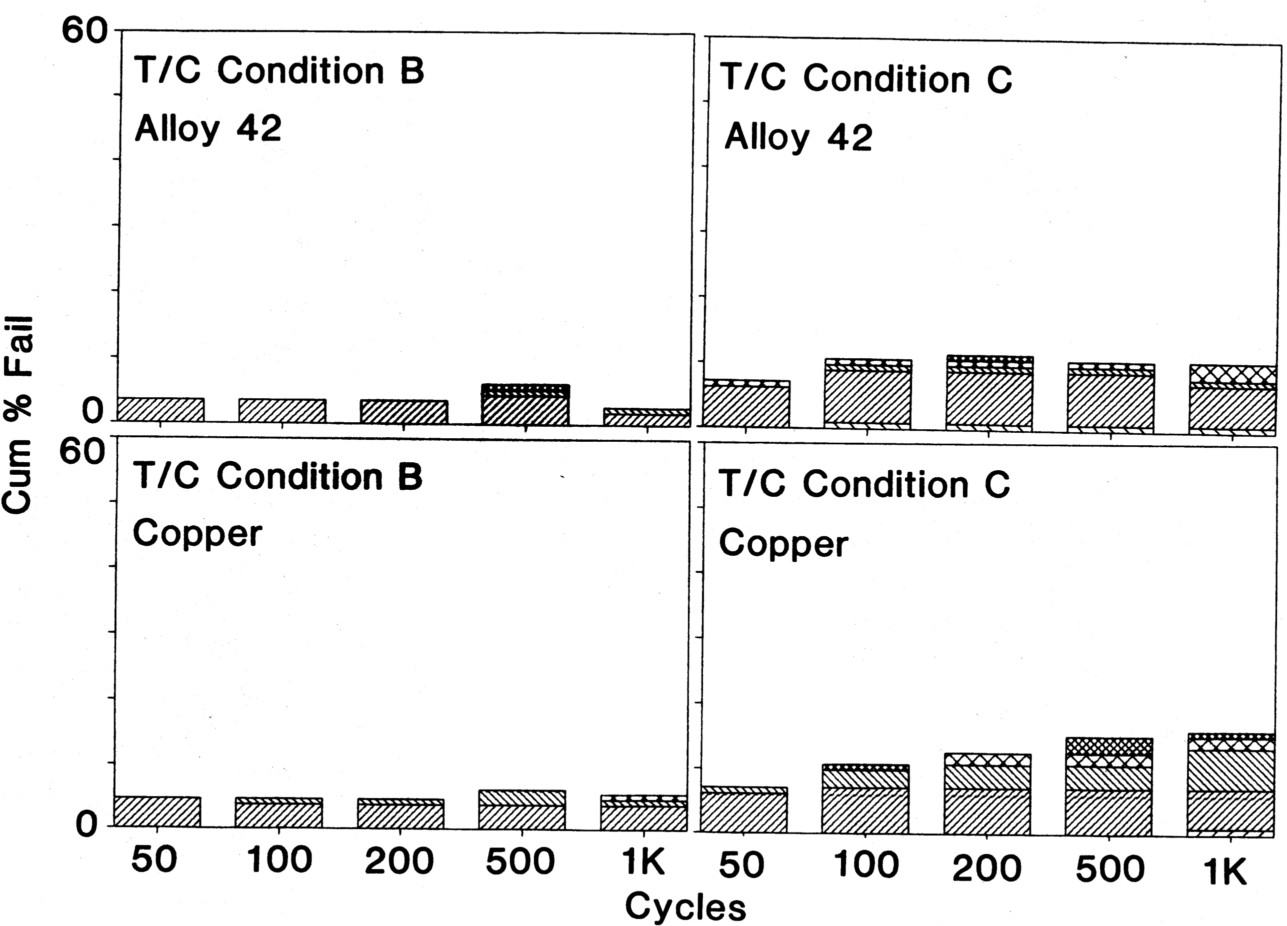


Fig. 14. Polysilicon resistor opens at sites (1,7) and (7,1) combined as a function of number of cycles of T/C condition B (left graphs) and T/C condition C (right graphs). Bar shadings indicate the contributions of the various circuit layouts. Note the preferential selection of layouts 3, 5, and 8.

---

- CPC is also observed in T/S, but only for copper lead frames. For Alloy 42 lead frames it is suppressed. It has the same tendency to occur at sites (1,7) and (7,1), and to select circuit layout 3 (Fig. 4).
- For greater than 150 cycles DPC is observed in T/S, but not T/C.
- Copper lead frames have a slightly higher failure rate for DPC than do Alloy 42 lead frames.
- DPC has no preference for any particular circuit layout or site, except that site (4,2) has an anomalously high failure rate.

## 5. DISCUSSION

The observations made in the previous section may be summarized as follows:

- Three mechanisms were observed:
  - Corner Ball Shear (CBS). Sheared ball bonds occurred only within 30-40 mils of the corner of the die.
  - Corner Passivation Cracking (CPC). Passivation cracking localized to the modules at (7,1) and (1,7).
  - Distributed Passivation Cracking (DPC). Passivation cracking occurring with equal probability anywhere on the die, except for site (4,2).

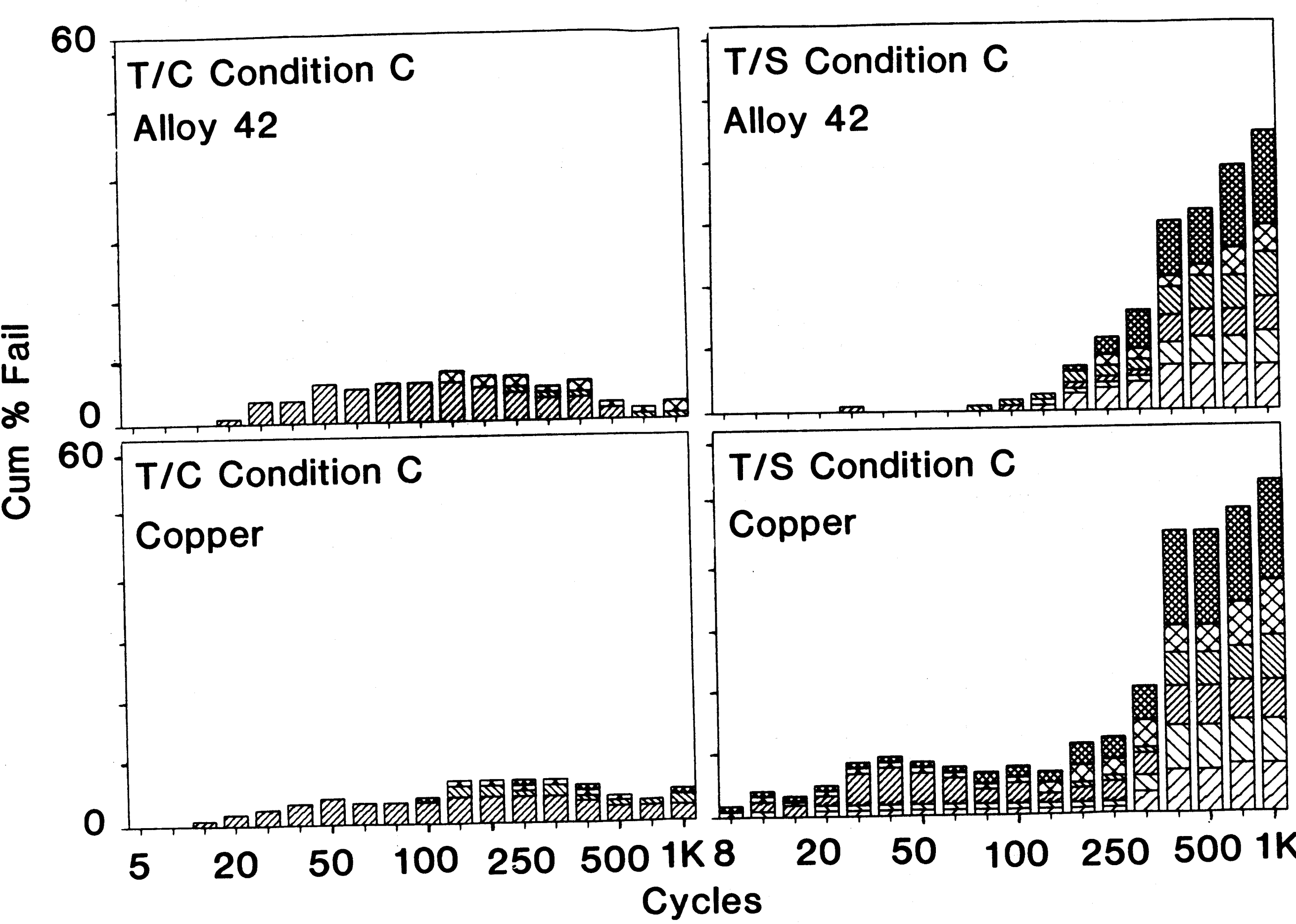


Fig. 15. Polysilicon resistor opens at sites (1,7) and (7,1) combined as a function of number of cycles of T/C condition C (left graphs) and T/S condition C (right graphs). Bar shadings indicate the contributions of the various circuit layouts.

---

- The three mechanisms have the following dependence on layout:

| | |
|---|---|
| CBS | All variants the same. |
| CPC | Variant 3 > Variants 5, 8 > Others |
| DPC | All variants the same. |

- The relative failure rates of the mechanisms:

| | Cu | | A42 | |
|---|---|---|---|---|
| | T/C | T/S | T/C | T/S |
| CBS | Hi | Hi | Med | Med |
| CPC | Med | Med | Med | 0 |
| DPC | 0 | Hi | 0 | Hi |

- Number of cycles (Cond C) to fail:

| | | |
|---|---|---|
| CBS | > | 150 |
| CPC | > | 20, "healing" after 150 cycles |
| DPC | > | 150 |

The most general observation is that T/S is far more complex, and damaging, than T/C. T/S introduces a failure mechanism not observed in T/C, DPC, and it does not depend in the same manner as CPC on the materials of the package. One of the most remarkable results is that CPC is suppressed in T/S relative to T/C for devices with Alloy 42 lead frames, but not for devices with copper lead frames. One concludes that T/S cannot be regarded simply as an acceleration of T/C, and that both are necessary to expose all failure mechanisms.

The results also have a bearing on the choice of the number of cycles of cycles of T/S or T/C needed to qualify a package. For CPC in T/C only 50 cycles are needed to produce the maximum number of failures, and "healing" sets in after about 150 cycles. Healing is probably an electrical artifact due to a

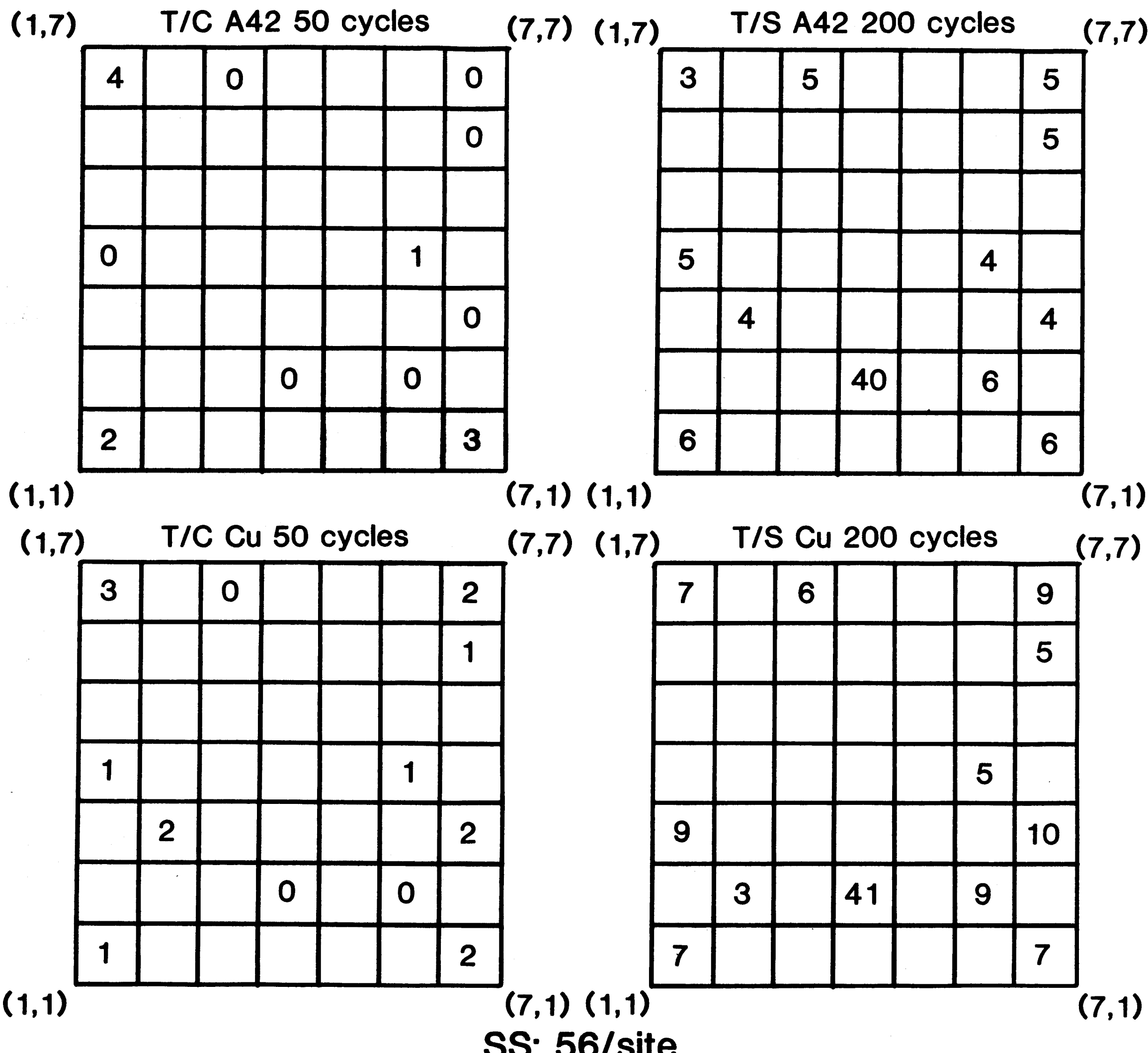


Fig. 16. Distribution of polysilicon resistor opens across die. Left maps show distribution when CPC dominates, while the right graphs show the distribution when DPC dominates.

relaxation which brings fractured surfaces back into contact. Still, it indicates that readouts at 500 or 1000 cycles of T/C may give an optimistic (low) indication of the incidence of CPC. On the other hand, wire opens due to WBS start at 150 cycles and the number stays roughly constant thereafter. Also, for T/S, WBS and DPC only start to produce failures after 150 cycles. On the basis of these observations, 200 cycles of both T/S and T/C is optimal for revealing all failure mechanisms.

It is interesting that ball shearing never resulted in a resistance increase of more than 100 ohms. A typical value was 20 ohms. If opens like this occurred on real devices, they would only cause functional failure if they happened to occur on a high current-drawing pin. A possibility which we have not explored is to see whether any of the opens become "dead opens" under hot or cold testing.

We found that introducing slots into aluminum busses, reducing the aluminum line width from 105 microns to 21 microns or less, was completely effective in eliminating thin-film cracking in the extreme die corners of overlying passivation. This confirms the results of Okikawa et. al.[2]. We also found that contacts of aluminum to substrate reduce the chance that the polysilicon crack-detection resistors will become open by cracking. The contact array can short to the polysilicon resistors which meander through the array of contacts. Slotting is therefore the preferred technique for minimizing thin-film cracking.

There are several areas open to further study. The is no obvious explanation for the high failure rate at site (7,7) by CBS, or at site (4,2) by DPC. Although dependence on circuit layout is understood[2], there is no model to explain, even qualitatively, the way in which the failure rates of the three

mechanisms depend on shock vs cycle or on leadframe material. These relationships probably depend more on the mechanics of the package than on the mechanics of the thin films on the die. It is hoped that these results will stimulate the development of better models for package mechanics. Such models should include the effect of thermal transients, and crack propagation and delamination of the molding compound.

ACKNOWLEDGMENTS

Thanks are due to Baby Kam for the assembly of the units, to Mike Kish for electrical test and failure analysis, and to Rajen Dias, Ron Oveido, and Suresh Golwalkar for failure analysis.

REFERENCES

1. M. Isagawa, Y. Iwasaki, T. Sutoh, "Deformation of Al Metallization in Plastic Encapsulated Semiconductor Devices Caused by Thermal Shock", in 18th Annual Proc. Reliability Physics, 1980, pp82-92.

2. S. Okikawa, M. Sakimoto, M. Tanaka, T. Sato, T. Toya, Y. Hara, "Stress Analysis of Passivation Film Crack for Plastic Molded LSI caused by Thermal Stress", presented at Int. Soc. for Testing and Failure Analysis Meeting, Los Angeles, CA, Oct. 1983

3. R. E. Thomas, "Stress-Induced Deformation of Aluminum Metallization in Plastic Molded Semiconductor Devices," IEEE Trans. on Components, Hybrids and Manufacturing Technology, Vol. CHMT-8, 1985, pp 427-434.