Shear Stress Evaluation of Plastic Packages

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Abstract—A study has been performed to determine the impact of package assembly on shear stress phenomena in plastic encapsulated integrated circuits (IC's). Test structures were used which allowed quantitative measurements of compressive stresses along with qualitative observation of shear stress effects. Results from experiments with various mold compounds, lead frame materials, and mount compounds will be presented. The experiments led to the development of a simplified stress model which can be applied to evaluating package and chip designs of future products.

INTRODUCTION

WITH THE advent of LSI and VLSI permitting the integration of complete system functions on a chip, die sizes have increased. This has pushed plastic packaging technology to develop new packaging solutions. Complicating the issue has been a drive towards smaller package outlines with an emphasis on surface-mount packages. These trends have led to increased mechanical stresses both on the plastic of the package and on the chip. New chip failure phenomena have been observed, including cracks from die mounting [1], deformed metal [2], [3], passivation cracking [4], and multilayer oxide cracks [5].

Of these, the latter three are largely functions of package-induced surface shear stresses. They are found mainly at the chip corners in passivations over wide aluminum busses, in narrow polysilicon interconnects passing under the wide busses, and in the multilevel oxides (MLO) along the edges of the busses. They lead to degraded leakage and corrosion performance, and in the case of multilayer oxide cracks, can cause catastrophic device failure. Understanding and control of these stresses are required for the design of a high-reliability package.

The shear stresses generated in a plastic package result from a complex interaction between the package materials, assembly process, and package geometry. Contributing factors include:

1) the package and chip geometric configuration;
2) thermal expansion mismatches between the materials (mold compound, silicon, lead frame metal, mount compound);
3) the thermal excursions of the package process (cures);
4) the adhesion properties of the materials.

Computer-aided finite-element method (FEM) models have been used to calculate average shear stresses at the chip surface. In separate FEM studies, Okikawa et al. [4] and Groothuis et al. [6] have shown exponential increases in the shear stress at the chip corners. Such FEM models allow input of various material properties, temperature conditions, and package geometries. Feedback from the design and test of the actual product is used to fine tune the accuracy of the model. However, modeling of shear stress effects in thin films is not yet as tractable. Problems that face such modeling include resolution limitations, difficulties with modeling localized variations in composite materials, difficulties in obtaining accurate physical characteristics of thin films, and the dynamic nature of the fracture mechanics involved.

A test structure approach to measuring shear stress effects was devised to provide a better understanding of the shear stress mechanisms for FEM refinement. The test structure scheme addressed three areas thought to have an effect on the shear stress problem: packaging, design, and wafer processing. Within packaging, test structures were used to evaluate new low-stress mold compounds, lead frame metals, the effects of different mount materials, the impact of post bond applied films, such as polyimide and silicon gels, and chip size variations. Process alternatives, such as chip metallization and passivation types versus thicknesses were also tested, along with a few design layout variations. The test structure approach allowed a ranking of the variations with respect to the amount of shear stress damage observed. This paper will report the results of the packaging investigation and will concentrate on methods for reducing the brittle passivation cracking mechanism.

TEST STRUCTURES

Test structures have long been used for fabrication process characterization. Recently, specialized test structures have been applied to the measurement of package-related phenomena such as stress and corrosion effects [1], [5], [7], [8]. The advantages of a test structure approach to assembly and package characterization include simplicity, direct measurement of internal package parameters such as stress and leakage, excellent correlation to actual device performance, and, usually, a lack of ambiguity in the readings. In addition, the test structures detect interactions between package components as a whole rather than in part.

The primary test chip used in this investigation was large, 12000 × 4500 μm on a side (Fig. 1). The test chip incorporated 1) strain gauges, 2) a wide metal electrical and visual structure to measure shear stress damage, and 3) a narrow metal structure that tested for delamination between the plastic molding compound and the chip surface. The test structures were positioned to obtain maximum sensitivity with
shear stress sensitive structures located in the corners of the chip and the strain gauges placed in an array to allow stress mapping. Correlation between results obtained with this test structure and studies with product devices has been good.

**Strain Gauge Description**

The strain gauge, detailed in Fig. 2, is formed by an implanted n-type resistor on (100) silicon. Since crystalline silicon is a piezoresistive material, the mobility of charge carriers, and hence the resistance of the diffusion, is modulated by the mechanical stress applied to the crystal lattice. The amplitude and sign of the resistance modulation are a function of the following factors: dopant type and concentration profile, the crystalline orientation of the silicon, and the nature of the stress, either compressive or tensile. For n-type diffusions or implants, positive resistance changes are indicative of compressive stress applied to the chip during the assembly operation. Negative resistance changes indicate tensile stress. The exact operation of these structures has been described elsewhere [9], [10].

Previous experiments with these strain gauges have shown characteristic patterns in their response [11]. Between wafer and mold, the chip within the package experiences about 75 percent of the maximum stress it will obtain. With post mold cure, as the plastic densifies, there is a continued increase in compressive stress which begins to level or decrease during temperature cycling due to stress relaxation. This relaxation can come from release of the molding material from the chip or lead frame or from the cracking of either the chip, mold compound, or mount material. The compressive stress is greatest at the center of the chip and least in the corners.

**Wide Metal Shear Structure**

The second test structure (Fig. 3) was designed to detect shorting between a wide metal line subject to shear stress damage and a narrow sense line. The wide line, designed to simulate a worst case power bus layout, was 102 μm across. The 10-μm sense line was separated from the wide bus by a 3-μm space.

**Fig. 4** is an example illustrating the types of cracking observed with this structure. In the low-magnification photo Fig. 4(a), large cracks in the passivation can be seen conforming to the direction of stress from the corner. Fig. 4(b) shows that the passivation over the wide metal bus has been shifted completely over the passivation of the narrow metal line. In the low-magnification photo of Fig. 4(a) these shifted layers show as dark lines at the edges of the metal. Note also that the passivation on the narrow line is uncracked and unshifted. In all observed cases the passivation over this narrower metal line remained intact after temperature cycling and acted as an insulating layer that prevented shorting between the two lines, negating the electrical intent of the structure.

**Fig. 5** is a cross-sectional view of the sampled picture in Fig. 4. Fig. 5(a) shows the typical crack morphology of the edge of the bus closest to the corner of the chip. Note that the passivation over the wide metal line has broken free and has shifted a good 3 μm across the surface of the chip. In the process, the metal under it has become deformed and smeared. Typical of outer edge cracks, the fracture in the passivation angles down towards the metal and the silicon along a 45° slope. Fig. 5(b) shows the crack morphology of the inward edge of the bus. In this picture the passivation that had been moored to the multilevel oxide has been completely shoved over the passivation of the adjacent narrow metal line. In contrast to Fig. 5(a), the crack runs parallel to the chip surface. The rationale for this typical crack behavior will be addressed by the model presented later in the paper.
Fig. 8 is an illustration of the package used in this investigation. It typifies the present plastic packaging trends which place larger and larger chips into smaller package outlines with less protective surrounding plastic. As such, it was considered to be a good vehicle to experiment with package effects on shear stresses. The results of the experiments can be easily generalized to other package types.

The test matrix used for package evaluation is diagrammed in Table I. Approximately 40 units were assembled in each leg of the matrix. Samples were decapsulated after durations on temperature cycling (−65°C to 150°C) up through 2500 cycles, totaling eight devices per matrix leg. It is interesting to note that within a given matrix leg, the same density and frequency of cracks was found on test structures decapsulated after 25 cycles as on those decapsulated after 2500 cycles.
cate greater compressive stress. The resistances plotted here represent the compressive stress directed along the length of the chip. Compound C exhibits slightly less compressive stress than the others, and, more importantly, shows a more uniform stress distribution from center to corner than either compounds A or B.

Fig. 10 shows typical crack characteristics observed for

implies that stress related cracking is an effect that occurs early on in temperature cycling.

**Mold Compound Study**

The molding compounds selected were all state-of-the-art low-stress epoxies. All compounds had been formulated for low shear stress characteristics, and there were no substantial differences in any of their physical properties. Indeed, the lack of "spec sheet" differentiation was one reason for the test structure approach.

Fig. 9 plots the average change in strain gauge resistance between wafer test and testing after 500 temperature cycles for the three molding compounds. Higher resistance shifts indicate greater compressive stress. The resistances plotted here represent the compressive stress directed along the length of the chip. Compound C exhibits slightly less compressive stress than the others, and, more importantly, shows a more uniform stress distribution from center to corner than either compounds A or B.

Fig. 10 shows typical crack characteristics observed for
Fig. 11. Strain gauge shifts measured for Alloy-42 versus Cu lead frames (500 temperature cycles: -65°C to 150°C).

Fig. 12. Cracking of Cu lead frame samples. Compare to Fig. 10(a).

Fig. 13. Strain gauge shifts measured for paste and film applied mount materials and 6-mil A-42 lead frame with film material (500 temperature cycles: -65°C to 150°C).

these compounds. The most sensitive crack location for this test structure is seen at the junction of the wide metal bus to its bond pad and is indicated by an arrow. This is an example of a design-related sensitivity to shear stresses. Comparing the crack densities to the strain gauge measurements shows that the compound with the most uniform stress distribution, compound C, also shows the smallest number of cracks.

**Lead Frame Study**

Lead frame materials tested were 8-mil (200-μm) copper and 8- and 6-mil (200- and 150-μm) Alloy-42. Changes in the resistances of strain gauges assembled on copper versus Alloy-42 lead frames are compared in Fig. 11. The higher stress level and nonuniformity across the chip in the copper case resulted from the mismatch in expansion coefficients between silicon and copper (3-17 ppm) as opposed to silicon and Alloy-42 (3-4.7 ppm). Not only are the stress values much greater on the copper lead frames, but the deviation within the group is much greater.

On an average of the samples assembled with copper lead frames, tensile stress was found in one corner after cure but in both corners and with increasing magnitude after temperature cycling, an indication that the silicon is approaching its breaking point in some of the samples. In fact, bending of the test chip was noted with copper lead frames following the die attach process. This bending occurs during cool down because the copper lead frame has expanded to a much greater length than silicon at the temperature where the adhesive gels and attaches the die to the lead frame.

Fig. 12 shows the typical passivation crack characteristics of a copper lead frame packaged unit (compare to Fig. 10(a)). In the majority of cases with Cu lead frames the cracks observed were more numerous than with A-42 lead frames.

**Mount Material Study**

Die attach materials tested were a silver-filled polyimide and a film version of silver-filled modified polyimide. Fig. 13 compares the effect of die attach on stress after 500 temperature cycles. The polyimide is applied as a paste and tends to produce voids beneath the chip and fillets of material around the chip perimeter. In contrast, the film mount is 0.8 mil thick, has no voids, and conforms to the chip outline with no excess to result in a fillet. At the post mold cure read point, there appeared to be little advantage to the film versus the paste on a 8-mil (200-μm) lead frame from a compressive stress standpoint, but after temperature cycling, as shown, the film results show considerably more uniformity across the chip than does the paste.

Nonuniformities in stress distribution with die attach materials have been attributed to voids [12]. In particular, voids near the edge of the chip may result in tensile stresses to the extent of die cracking in unmolded packages. Changes in stress distribution have been previously noted with both polyimide and epoxy die attach (more significant with undercured epoxy materials) on temperature cycle [13]. The void-free fully cured nature of the film mount appears to provide more stability under temperature cycling than can be achieved with a paste-applied mount.

A much greater degree of stress uniformity can be seen with a 6-mil (150-μm) lead frame coupled with the film mount. Stability to temperature cycling is most significant. The uniformity from the center of the chip to the corner is detailed in Table II.

The effect of lead frame thickness and mount on the stress uniformity may be related to previous observations in this lab and finite-element modeling data which have shown that the die attach material behaves like a compliant layer. If the thickness of the die attach material could be increased, it would absorb differences between the two rigid materials; i.e., silicon and lead frame. Thinning the lead frame reduces its ability to warp the silicon.

Fig. 14 shows typical crack features observed for the mount materials and lead frame thicknesses (compare to Fig. 10(a)). Note the significantly reduced number of cracks with the film.
TABLE II
STRESS DISTRIBUTION: 500 TEMPERATURE CYCLES

<table>
<thead>
<tr>
<th></th>
<th>Corner</th>
<th>Center</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-mil A-42, paste</td>
<td>0.1</td>
<td>1.1</td>
<td>1.0</td>
</tr>
<tr>
<td>8-mil A-42, film</td>
<td>0.4</td>
<td>1.1</td>
<td>0.7</td>
</tr>
<tr>
<td>6-mil A-42, film</td>
<td>0.6</td>
<td>0.9</td>
<td>0.3</td>
</tr>
</tbody>
</table>

mount material. Note also that the 8-mil lead frame produces featherlike cracks not found with the 6-mil lead frame.

Post Bond Applied Films

Stress relief overcoats of unfilled polymeric materials may be added to the surface of the chip to cushion compressive stresses from the mold compound; they cannot act to relieve stresses in the silicon from lead frame or die attach. Silicaes, because of lower elastic moduli, are particularly well suited as stress absorbers, but their expansion coefficients are high, and in a plastic package system, bond wire damage may result.

Finite-element modeling of stress relief overcoats shows that stress can be significantly relieved on the chip corners at the expense of increased stress in the bond wires and ball bonds. Fig. 15 is a contour of shear stress in a package without a potting overcoat. Note the shear stress values of about 11 k lbf/in² at the chip corner. With a Si-gel coating, the stresses on the corner of the chip are reduced to 1 k lbf/in², but potentially damaging stresses of 34–36 k lbf/in² are produced inside the ball bond and bond wire (Fig. 16). Fig. 17 shows the stress contours for the same system with a polyimide applied coating rather than a Si gel. Note that stresses have been reduced in the bond wire to 12 k lbf/in² but that the shear stress on the corner has only been reduced to 6–8 k lbf/in².

A polyimide and Si gel were drop applied as stress relief coatings after wire bonding of the test chips. The attempts made to achieve good corner coverage with the materials were only partially successful with the polyimide. The strain gauge results shown in Fig. 18 are consistent with the material properties. The polyimide applied as a 25-μm-thick layer provides a lowering of compressive stress in the center of the chip and distributes the stress more uniformly both before and after temperature cycling. The more compliant silicone ap-
plied at approximately 125-μm thickness buffers the high compressive stress in the center of the chip to an even greater extent.

Visual inspection revealed no passivation cracks on any chip coated with Si gel. One very small passivation crack was observed at the point closest to the chip corner on a device coated with polyimide. It is felt this crack is related to the difficulty encountered in achieving complete coating coverage in the extreme corners of the chip with the drop-applied polyimide.

No attempt was made in this test to optimize the assembly procedure to protect the bond wires from wicking-induced stress. Predictions that wire breakage would increase with overcoat process proved true. Continuity failures after 500 temperature cycles were as follows: nonpotted—1.0 percent, polyimide—2.3 percent, and silicone—6.6 percent.

**Electrical Delamination Measurements**

The resistance measurements of the electrical metal smear test structure provide a measure of mold compound delamination and slip along the chip surface. Though not capable of giving direct readings of the shear stress, such delamination will occur only when the shear stress is sufficient to break the interfacial adhesion. Delamination occurs faster and is greater on assemblies with higher shear stresses. Comparisons between assemblies can be made when the adhesion between the mold compound and chip surface is held constant. Since the studies with this structure were conducted with a single mold compound from a single lot, adhesion was a constant, and variations in electrical performance can be related to shear stresses.

Fig. 19 shows test results from three lead frames: A-42 (8 mil), A-42 (6 mil), and Cu (8 mil). Here Cu has shown the largest resistance increase, followed by A-42 (8 mil) and A-42 (6 mil). This correlates to the stress distributions plotted in Figs. 11 and 13. In addition, samples assembled with Cu lead frames showed the highest level of cracking among visual inspection structures.

Fig. 20 plots the resistance increase of the smear structures for the two post bond polymeric potting materials mentioned earlier. As expected, the Si-gel group showed no resistance variation because it was protected from the displacement-abrasion effects of the plastic. However, some resistance increase occurred on units coated with polyimide, probably as a result of poor corner coverage. Beading of potted polyimide as applied in these experiments resulted in insufficient coverage up to about 4 mils from the corner, just where shear stresses are highest and just where visual inspection showed metal abrasion to be maximum.

When delamination occurs, the effective "corner" of the chip is moved to the contact point between the plastic and the chip. If delamination is concurrent with the formation of a crack in the plastic along the chip edge, high shear stresses can develop at the effective "corner" that can lead to shear-stress damage far inboard from the actual corner. Visual inspection of metal smear structure cross sections has shown metal shifting (delamination) at up to 60 mils from the corner. Thus the movement of wide metal lines out of the immediate corner regions may not be enough to eliminate all shear-stress damage.

**Experiment Summary**

The results of the experiments just described are summarized in Table III. The column labeled "stress gradient" reports the percent difference in the measured stress between the chip corner and chip center after 500 temperature cycles. The column "crack rating" attempts to assign a qualitative value to the severity of the cracks observed. A rating of "O" indicates that no cracks were found in any units, while a rating of "3" represents severe passivation cracking and lateral passivation dislocation.

While only a weak correlation was found between the severity of cracking and the maximum compressive stress, a
strong correlation was found between cracking and the high and low stress differential. Those materials which had 60 percent or less difference in resistance change from center to corner strain gauge had significantly fewer cracks in the passivation than those with greater than 60 percent. This correlation suggests that nonuniformities in stresses as measured by strain gauge mapping indicates greater concentrations of shear stresses present on the chip. The correlation implies that the stress gradient after temperature cycling is an effect of plastic/chip delamination and, therefore, correlates to the electrical smear measurements.

THEORETICAL DISCUSSION

As has been shown experimentally, the shear stress experienced at the surface of the chip is a result of a complex interaction between the chip, mold compound, mount material, and lead frame. The shear stress is caused primarily by 1) volumetric shrinkage of the plastic material during cure, and 2) differences in the thermal expansion and elastic moduli properties of the materials as the devices cool down from the zero shear-stress state of cure to room temperature and below.

Fig. 21 shows how stresses are generated in a simplified two material system. Here, material "A," the plastic, has a higher Thermal Coefficient of Expansion (TCE) than does the silicon "B." Were it in free state, "A" would experience a greater thermal displacement than "B." Since the materials are in intimate contact, a compromise displacement results, with the creation of tensile stress in the plastic and compressive stress in the silicon. The stress gradient between the materials creates shear stress along the interface which, in the case of a plastic-encapsulated chip, is loaded onto the passivation and metallization. The conclusions from generalizing this simplified model to an encapsulated chip are the following.

1) The shear stress at the center of the chip, where there is no net thermal displacement, is zero.
2) The shear stress increases radially with distance from the chip center and is greatest in the corners.
3) The shear stress at the chip surface will be a function of

the five-layer system including (top down) the plastic, chip, mount material, lead frame, and plastic.

4) Geometric factors will lead to stress concentrations.

Fig. 22(a) shows a schematic of the chip surface under a uniform shear-stress field. The unit arrows indicate the direction of force applied by the plastic towards the chip center. There are two forces diagrammed here: a sidewall lateral force which is the same for both the wide and the narrow lines, and the surface forces. As can be seen, the passivation of line 1, being four times wider than line 2, experiences four times as much surface force. The underlying metallization, however, has both a low modulus of elasticity and a low threshold for plastic deformation. It offers little resistance to the tendency of the passivation to slide; load shedding to the underlying oxides and silicon is inefficient. Stresses are, therefore, concentrated at locations "A" and "B" and are greater in these locations on line 1. In region "C" the stresses propagate harmlessly into the underlying oxides and silicon.

If the stresses in locations "A" and "B" exceed the passivation strength, cracks will occur. Because these stresses are greater on the wide line, cracks are more likely to occur on passivation over wide metal traces. In addition, the stress concentrations in locations "A" and "B" can generate dangerous levels of tensile stress in the oxide/passivation interface. Oxide fractures have been observed in the region under "B" without any apparent passivation cracking.

Fig. 22(b) shows the surface conditions after delamination. Here only the sidewall forces remain and the stresses at points "A" and "B" on line 1 equal those on line 2. If cracking
occurred after delamination, an equal distribution of cracks would be expected on line 1 and 2. Since this is not the case, and since passivation cracking is observed as early as 25 cycles while delamination usually occurs at about 300 cycles, the conclusion is that cracking occurs before delamination.

To demonstrate the effect of stress loading on an actual design, Fig. 23 shows an outline of the wide metal shear test structure of Fig. 3 with three radial lines drawn along the direction of force applied by the plastic. The length of these lines represents the effective metal width along that cross section. In a uniform stress field the force applied to a test segment of the passivation along line A is greater than B which is greater than C. Because the stress is not uniform but is a function of distance from the chip center, the average stress along any segment must be calculated by integrating the stress magnitude along the segment. The force along the test segment can then be calculated by multiplying the area of the test segment by the average stress as in the following equations:

\[ F_{\text{seg}} = \sigma_{\text{ave}} \times (L \times W) = W \times \int \sigma(r, \theta) \cdot dr \]

(1)

where

- \( \sigma_{\text{ave}} \): average stress on segment,
- \( F_{\text{seg}} \): total force on segment,
- \( L \): length of segment,
- \( W \): width of test segment (nominally small).

Integration is along the test segment.

The exact values of the stresses at points A and B in Fig. 22 are not easily calculated. As has been shown, they depend on the applied stress and the width of the metal. In addition, they are influenced by the following:

1) the moduli of the plastic and metallization;
2) the hardness and thickness of the metallization;
3) the susceptibility of the metallization to plastic deformation;
4) the strength and thickness of the passivation;
5) the metallization and passivation film stresses built in during processing.

Yet another factor which must be considered is the effective weakening of the passivation due to its mechanical structure. After noting that the elastic moduli of both aluminum and typical plastics are an order of magnitude less than the elastic moduli of typical passivations, Okikawa et al. [4] suggested that the passivation could be considered as a long column under a buckling load. Assuming that the passivation cracking occurred only after a stress sufficient to cause buckling was reached, the strength of the passivation was approximated by the following equation which predicts the stress required to cause buckling:

\[ \sigma_p = \frac{n\pi^2EI}{L^2} \]

(3)

where

- \( \sigma_p \): strength of passivation,
- \( E \): Young’s modulus,
- \( I \): geometrical moment of inertia,
- \( L \): width of aluminum metallization,
- \( n \): constant.

This formula is based on Euler’s equation for the buckling load of an ideal slender column. \( N \) is a factor to be determined experimentally. A more precise formula would be as follows [14]:

\[ \sigma_p = \frac{K\pi^2E}{(L/r)^2} \]

(4)

where

- \( E \): modulus of elasticity for passivation,
- \( L \): passivation span length (metal width),
- \( r \): radius of gyration,
- \( K \): constant.

If the passivation segment of interest is a long slender rod of material with the width of the rod greater than the thickness, then the radius of gyration can be replaced with the following:

\[ r = t/(2\sqrt{3}) = t(0.2887) \]

(5)

where \( t \) is the passivation thickness.

This equation, then, relates the stress required to crack the passivation to its length and thickness. It predicts that as the passivation span becomes greater, a lower average stress along the linewidth will cause cracks. It also predicts that a thicker passivation will be more tolerant of stress than a thinner one. The parameter \( K \) in (4) is a measure of the constraining factors of the plastic and metallization which encase the passivation and represents a perturbation away from the ideal slender column case. By assuming this equation completely describes the stress required to crack the passivation and by forcing this stress to equal the shear as figured through computer modeling, \( K \) was found to be 10 in our studies. Okikawa et al. found good agreement to experimental values if \( K = 4 \).

One must question how an equation that is used to calculate the critical force required to buckle a long straight rod relates to the problem of cracked passivation. If the cracking was a direct result of buckling, cracks would be expected to occur down the center of the passivation spans, not at the edges of the metallization. Also, how does this model explain the occurrence of cracks at point A before cracking at point B?

Fig. 24 attempts to justify the observed experimental behavior. Fig. 24(a) shows a diagram of the unbuckled passivation. Here, the force applied by the plastic is repre-
sent by vector $P$, $P'$ is the opposing force from the passivation. In this instance, the shear torques at point $A = B$. If the conditions of (4) are met, the passivation buckles either up or down into the metallization (Fig. 24(b)). The downward buckle is expected due to vertical compression from the plastic, the tensile nature of the deposited aluminum, and the lower elastic modulus of the aluminum versus the plastic. If downward buckling occurs, some stress is relieved from point $B$ due to the bending curvature which is opposite the direction of the applied stress. However, extra stress is generated at point $A$. If the stress is sufficient, cracks will begin at point $A$.

When the passivation fractures at point $A$, additional stress is applied at point $B$. Also, if lateral fractures have occurred in the metallization, the passivation can act like a plate moored at $B$ in a shear-stress field. In this case, the plastic would tend to lift the passivation, applying tensile stress at $B$ along with shear stress. This is the mechanism felt to be responsible for the lifted and shifted passivation pictured in Fig. 5. It also explains the presence of a shear crack at point $A$ in Fig. 5(a) and the tensile crack at point $B$ in Fig. 5(b).

**Summary**

The experimental studies have shown that shear stresses can be reduced in plastic packages through proper selection of materials. The visual shear-stress test structure in conjunction with the diffused strain gauge proved to be valuable test structures for selecting between assembly options when there was no other selection criterion such as a difference in physical properties. Specifically, the studies showed the following.

1) Strain gauges are good structures for selecting between low shear-stress molding compounds when nominal physical properties are equal.

2) Assemblies with higher compressive stress gradients across the chip after temperature cycling are those with greater shear stress damage.

3) Mount materials producing a more uniform bonding layer between the chip and lead frame produce lower more uniformly distributed compressive stresses in assemblies and provide more stability during temperature cycling.

4) The choice of lead frame materials can have a dramatic impact on the observed brittle passivation cracking and compressive stress gradient. Matching the expansion coefficients of the lead frame metal towards the silicon reduces shear stresses. Matching towards the plastic increases the shear stress.

5) Thinner lead frames produce lower shear stresses.

6) Wide metal lines are more susceptible to shear stress effects than are narrow metal lines.

The conclusions which can be drawn from the theoretical discussion are as follows.

1) The effective width of any metal line is the edge-to-edge width measured along a radial path from the center of the chip.

2) The stress applied to the passivation over an effective width is the integrated average of the stress.

3) The stresses applied to the passivation over metal is inefficiently transferred to the silicon due to the ductility of the metal. Stress builds up at points where the passivation is anchored to the multilevel oxides.

4) Since more stress is loaded onto wide passivation spans, passivation cracking occurs first at the edges of wide metal lines.

5) Any design or process method which improves the transfer of stress to the multilayer oxides will reduce passivation damage. This includes slotting of wide metal lines and hardening of the metallizations. Thickening passivations will give them more strength.

**Acknowledgment**

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**References**


