Soft Errors
Causes and Mitigation

HINA MALIK

Errors

- Hard Errors
  - Cause a device to be permanently damaged
  - Affect chip yield
- Soft Errors
  - Non-destructive, cause transient damage
  - Affect lifetime reliability

Soft Errors

- Predominantly caused by radiations.
- Radiation event causes enough of a charge disturbance to flip the state of a memory cell.
- Single Bit Upset- SBU
- Multibit Upset- MBU

Types of Radiations

- Alpha particles
- Cosmic Rays
  - Low energy cosmic rays
  - High energy cosmic rays

Alpha Particles

- Cause: Radioactive impurities in packaging materials
  - Thorium and Uranium impurities
- Mitigation:
  - Employ high purity materials

Not a problem any more!

Cosmic Rays

- Of galactic Origin
- React with earth's atmosphere producing secondary and tertiary particles.
- Neutrons are the highest energy particles.

- Types of Cosmic Rays
  - Low energy Cosmic Rays
  - High energy Cosmic Rays

Low Energy Cosmic Rays

- Cause: Interaction of low energy cosmic ray neutrons (<< 1M eV) with Boron
  - Boron used in formation of Boron-doped Phospho Silicate Glass (BPSG)
- Mitigation:
  - BPSG has been removed from all advanced technologies

Not a problem any more!

High Energy Cosmic Rays

- Cause:
  - High energy neutrons interact with chip materials
  - Break Si nucleus into lighter fragments
- Mitigation:
  - Cosmic rays cannot be eliminated at the source

Effective shielding would require meters of concrete or rock!

Handling Soft Errors

Devices/Circuit Solution:

- Produce designs that resist cosmic ray effects e.g. Node Hardening

Architectural Solution:

- Invent mechanisms to detect and correct errors e.g. Error Correction Codes and Bit Interleaving

Node Hardening

- Device parameters that affect SERs
  - Q_{crit}
    - The smallest charge that results in a soft error
  - A_{diff}
    - Area of the circuit sensitive to particle strikes

$$SER \approx A_{diff} \times e^{-Q_{crit}}$$

$$Q_{crit} \approx V \times C$$

Layout modifications

- Minimize diffusion area
- Increase critical charge
  - Increase node capacitance by adding extra gate capacitance
    - Mitigates soft errors but
      - Results in area and power overheads

How can we minimize these overheads while improving soft error tolerance?

Selective Node Hardening

- Do we need to harden every node?

$$SER^{chip} = \sum_{cell} \sum_{nodes} (SER^{nominal} \times TVF \times AVF)$$

  - TVF - Timing Vulnerability Factor
    - Fraction of time a node is vulnerable
  - AVF - Architectural Vulnerability Factor
    - Fraction of faults that actually cause an error

Only harden nodes with high TVF and AVF

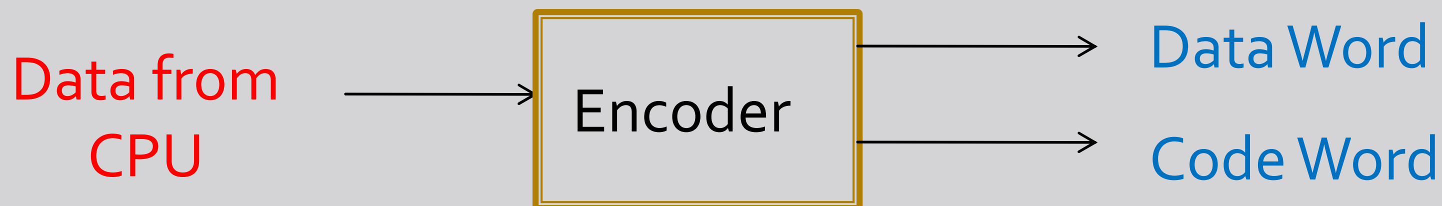
Increase SER tolerance without prohibitive overheads

Error Correction Codes (ECC)

- ECC tolerates errors by using information redundancy

- Divide memory into data words (e.g., 8-bit chunks)
- For each data word, store a corresponding code word

- Encode data upon writes:



Error Correction Codes (ECC)

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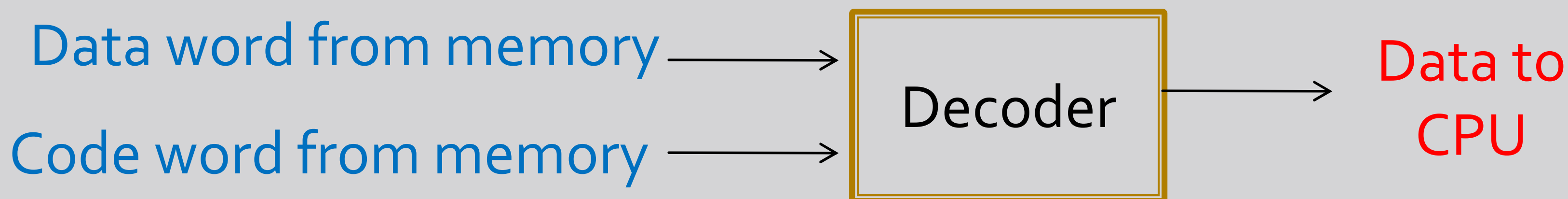
- Decode data upon reads:



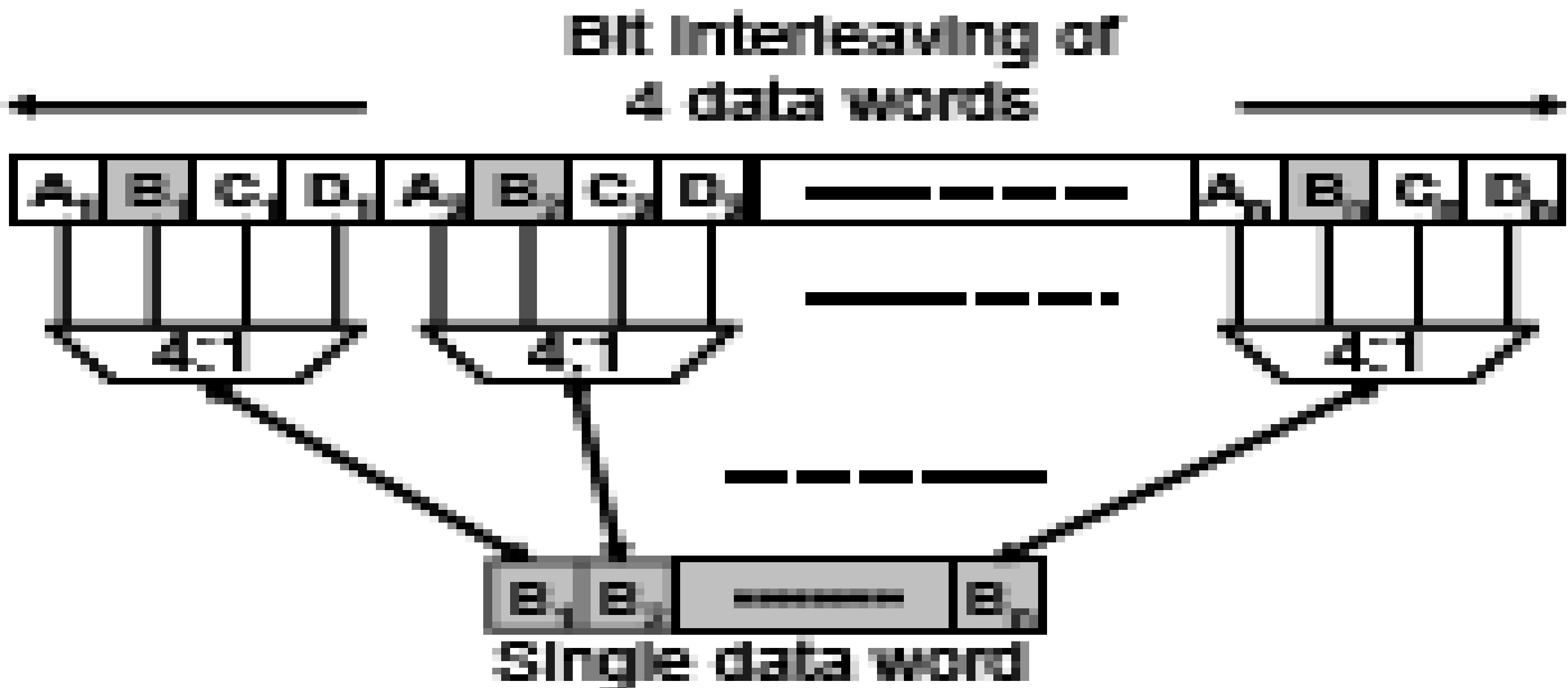
Single bit vs. Multi-bit Errors

- In current technologies, majority of soft errors cause SBU
- As technology continues to scale:
  - More memory cells fall under a single particle strike's footprint
  - MBU rate increases exponentially, as feature size decreases

- SECDED ECC can correct single-bit errors
- Correcting two errors would need a DECTED ECC
  - But DECTED doubles the ECC storage overhead

How can we correct 2-bit errors without incurring DECTED's storage overhead?

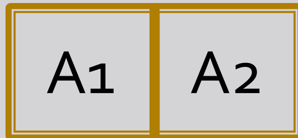
Bit-Interleaved ECC



Solution: Create data words by interleaving across data bits

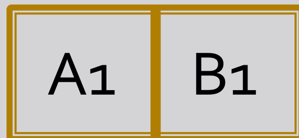
Bit-Interleaved ECC

- Without interleaving:



SER strike corrupts A1 and A2
SECDED ECC does not work

- With interleaving



SER strike corrupts A1 and B1
SECDED ECC works!!

Bit interleaving converts a multi-bit error into multiple single-bit errors

Conclusions

- Soft errors are of transient nature and are caused predominantly by radiations
- High energy neutron strikes are the most problematic source of soft errors
- Device/Circuit Solution: Selective Node Hardening
- Architectural Solution: Bit-interleaved ECC

Soft errors are an important reliability problem and need intelligent solutions