An Experimental Study Comparing the Relative Effectiveness of Functional, Scan, IDDq and Delay-fault Testing

SEMATECH^{SM} Test Methods PTAB

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ABSTRACT

This paper describes an experiment in which various semiconductor test methodologies (stuck-fault, functional, delay and IDDq) are applied to an ASIC device. The goal of this project is to provide the data that will enable manufacturers to optimize their application of the various tests. This project was supported through SEMATECH (Project S-121, "Semiconductor Test Method Evaluation").

1. Introduction

In order to achieve high quality of VLSI components it is accepted that a good test strategy must consist of a number of different types of tests. For any particular device, the tests used would typically be chosen from the set of functional, at-speed functional, scan-based stuck-at, scan-based delay and IDDq. Although much has been written regarding the usefulness of each of these tests, very little has been published regarding the relative effectiveness of each type of test on real devices. A major problem in carrying out such work is that it must be empirical: results on real chips are the only way to verify if the theoretical usefulness of a test is bourne out in practice. Since the gathering of such data is both difficult and expensive, it is not surprising that there is a deficit of information.

Recently, some experimental work has been reported. Several different test methods have been applied to a special test chip and their effectiveness have been evaluated [1-3]. A production chip has also been used to gather data [4]. Studies such as these support the concept that no one test method is sufficient to detect all defective devices. Because of resource limitations, however, both studies were limited in extent, leaving many more questions unanswered.

A better understanding of the key testing-related technological issues facing the IC industry is important to ensure that test does not become a manufacturing bottleneck from either cycle time, product quality or cost point of view. When one has the choice of a number of test methods, it is highly desirable to be able to trade off one type of test with another. Given X seconds of VLSI tester time, how should it be optimally allocated among the various test techniques currently employed by IC manufacturers? Extensive data is necessary to begin to be able to answer this question.

Because of the strategic advantage of having this data, the situation was seen as a unique opportunity to have technical cooperation among competitors. Such collaboration would have been possible only through a consortium such as SEMATECH. SEMATECH's mission is to "create shared competitive advantage by working together to achieve and strengthen manufacturing technology leadership," so the formation of a collaborative effort to undertake a test methods experiment fit well into this framework.

As a result, a "Test Methods" Project Technical Advisory Board (PTAB), was formed in April of 1994 to design an experiment to address the issues listed above..

Rather than produce a special design, it was decided to use an existing production ASIC, since this would be more representative of designs being manufactured by member companies. IBM volunteered to perform the experiment on a leading-edge (.45 µm Leff) design, using testing methods that are representative of common IC production test practices.

Whereas results from this experiment will not answer all questions, comparing them with others' results, such as those mentioned above, will provide more complete information. Since there will still be unanswered questions, it is hoped that the project will serve as a springboard to better industry cooperation (including university researchers) in jointly addressing key technical issues. The project is ongoing, and more data will be released in the future.

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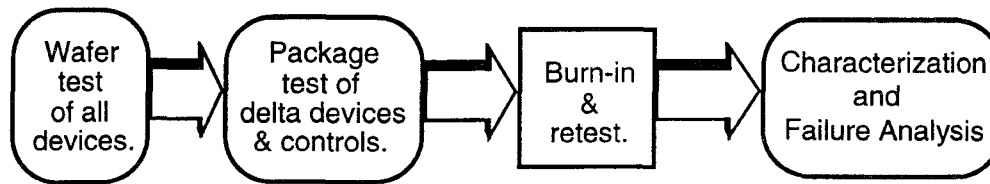
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Figure 1. Major project steps.

2. Project Background

The key objectives of this project were to compare the relative effectiveness of the test methods and to collect as much raw data as possible to enable additional analysis.

The four test methodologies analyzed were
- stuck-fault testing
- functional testing
- delay testing
- IDDq testing

There were three basic categories of devices that were evaluated. The first category include devices that passed all four of the tests listed above. The next was devices that failed all four tests. The third category was devices which passed some, but not all, of the applied tests--i.e., devices where we did not get perfect correlation among the four test methods. These will be referred to as *delta devices*. Most of the project steps (e.g., burn-in, failure analysis) concentrated on the delta devices plus a sample of control devices (ones that passed all tests). The key steps of this project are shown in Figure 1.

Each of these categories have unique characteristics which can skew any particular analysis. In particular, the failure analysis results are dependent on the sample submitted for analysis.

3. Device Description

The design that was chosen is a standard cell ASIC. Figure 2 shows the test-related chip architecture including the level-sensitive scan design (LSSD) chains. The chip has the following characteristics:
- Technology: IBM CMOS4LP, "Phoenix" ASIC family
- Chip function: bus interface controller
- 116K 2-input equivalent NAND logic gates
- 0.45 μm effective channel length (0.8 μm drawn)
- Three levels of metal
- 249 signal I/Os. C4 wafer contacts
- Package: 304-pin C4FP (C4 flat pack)

- Operating speed: some portions of the chip operate at 40MHz and other portions of the chip operate at 50MHz (both data & clock)
- 5280 LSSD shift register latches (full scan, double latch design)
- Eight scan chains
- Boundary scan
- VDD nominal voltage: 3.3V
- IDDq testable (i.e., design has zero static current)
- Die size: 9.4mm X 8.8mm
- Power bus is connected on-chip and connected to 20 off-chip pads.

4. Test Descriptions

In this section, the tester and each of the applied tests is described.

The tester used for this project was an Advantest 3381. It has the following characteristics: 512 pins, 100MHz maximum frequency (10ns cycle time), 300ps timing accuracy, and shared voltage & timing resources. The test fixture board was modified to add a relay between the low frequency capacitors and VDD to improve the IDDq measurement time and to ensure no added IDDq leakage was measured due to this capacitor.

The tests applied to each device are listed below. Notice that some additional "characterization" tests that were designed to add parametric test information were added to package-level testing. **Note that none of the original tests were removed or modified.** This was critical to ensure that equivalent test results could be compared from test step to test step.

Each of the voltage tests (stuck-fault, functional, delay and scan flush) were applied at three power supply corners: nominal and plus/minus 300mV (3.3V, 3.6V and 3.0V, respectively). The IDDq vectors were applied at a VDD voltage of 3.6V.
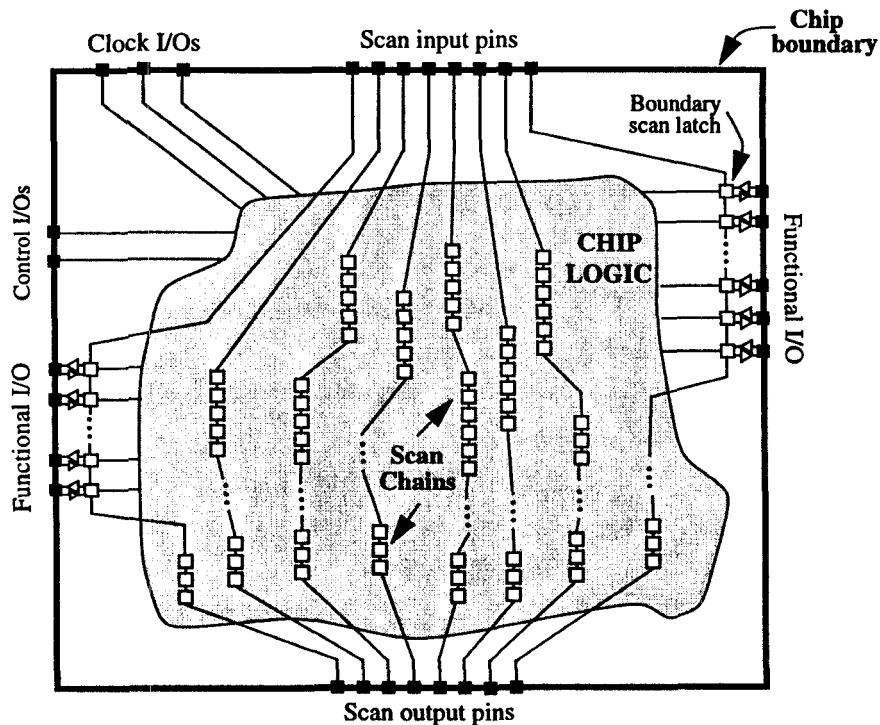
Figure 2. Chip architecture showing scan design architecture and boundary scan. (The scan input and output pins are also used as functional I/O. This is controlled by mux circuitry that is not shown.)

Power-up tests. Two types of power-up tests were applied -- a gross power supply short test and a signal input/output (I/O) opens and shorts test. If either of these tests failed, testing was aborted. If these tests passed, all other tests were completely applied--regardless of the testing results.

Stuck-at fault tests. The stuck-fault vectors were generated by IBM's test generator and applied using the LSSD scan chains. 8023 vectors were generated and had 99.79% stuck-fault coverage (375,142 total faults). The stuck-fault vectors were applied at a frequency of 2.5MHz (400ns cycle time).

Functional tests. A group of design-verification functional vectors were translated into test vectors and fault graded using the stuck-at fault model. The 532K functional cycles were graded to a fault coverage of 52%. These vectors were applied at a frequency of 29MHz. (The functional cycle time for these vectors was determined empirically at the tester.)

At package test, an additional test was added which applied the functional tests at relaxed timings (2.5MHz at VDD=3.0V). Also, another test was added in which the functional tests were repeated at a number of frequencies (29MHz, 26MHz, 20MHz, 2.5MHz) and the minimum output strobe times were measured. These were performed at VDD=3.0V.

Delay tests. The delay tests that were applied relies on using the LSSD scan chains as controllable and observable nodes which translates most timing requirements into simple launch/capture tests as shown in Figure 3 [5]. The delay test vectors were created by IBM's delay test generator [6]. Each vector was applied using the LSSD scan chains and the applied timings were calculated using a timing simulator. 5232 test vectors were generated that have a transition fault coverage of 91%. Thirteen unique timing sequences were applied--most of these timing sequences apply the launch/capture LSSD clocks at a critical timing close to the system functional cycle time (approximately 26ns).

At package test, an additional test was performed in which the delay test vectors were applied at relaxed timings (>1uS) at VDD=3.0V. Also, a test was added in which 15 minimum timing measurements were made for a subset of the delay test vectors. These were performed at VDD=3.0V.

IDDq tests. A total of 195 IDDq test vectors were applied to all devices at each test step. These vectors consisted of:
- 125 vectors created by IBM's IDDq test generator which targets pseudo-stuck-at faults (95.7% fault coverage)
- 10 vectors that applied simple, regular patterns into the scan chains (e.g., all zeros, all ones, alternating 0s/1s)
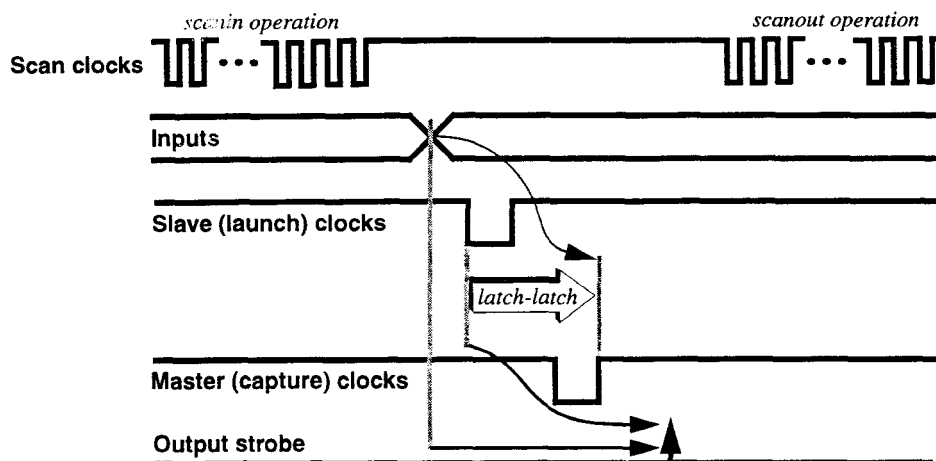- The first 60 vectors of the stuck-fault tests

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Figure 3. Timing diagram for latch-to-latch delay testing.
The LSSD latches consist of a master/slave pair controlled by separate clocks.

The final two sets of vectors were not fault graded. All IDDq test vectors were applied through the scan chains. For all 195 IDDq vectors, the absolute value of the IDDq current was measured and stored.

There were a total of 642 IDDq test vectors (graded to 99.5% fault coverage) created by the test generator. The additional 517 vectors which were not initially applied were used during characterization and diagnostic testing.

At package test, a test was added which measured the IDDq current for the first 20 IDDq vectors at VDD=2.0V.

Scan flush. A timing measurement was performed by sending a transition from the scan-in pin to the scan-out pin of the LSSD scan chains and measuring the propagation delay. This measurement was used to establish a relative performance for each device.

I/O Leakage. An I/O leakage test was added to the package-level tests. This test forced each I/O pin to VDD & GND voltages and ensured no more than 1µA of leakage current was measured. This test detected some failures that were in the I/O circuitry.

5. Test results data

The following information was collected for each device at each test step:

- Pass/fail results for each "pass/fail" test
- IDDq value for each IDDq measurement
- Scan flush delay measurements
- For failing chips, store first 10 failing vectors

A few characterization tests were added for the package-level tests. These included:

- Delay test timing measurements
- Functional strobe & rate measurements
- IDDq measurement on power-up
- IDDq measurement after waiting 1 second

All data is stored in ASCII format.

5.1 Characterization and diagnostic tests

A number of tests were selectively applied to a sample of packaged devices--e.g., the devices which exclusively failed the delay test or the devices targeted for physical failure analysis. These tests included:

- Additional timing measurements for the delay tests
- Delay vs. VDD voltage shmoo plots
- Collection of additional failures (failing vectors/pins)
- Application of additional IDDq patterns (up to 712 patterns)
- IDDq measurements for four vectors at a number of VDD voltages: 3.9V, 3.6V, 3.3V, 3.0V, 2.5V, 2.0V.

6. Burn-in description

The applied burn-in conditions were

- VDD voltage: 1.5X nominal VDD
- Temperature: 140°C
- Duration of initial burn-in: 6 hours
- Duration of extended burn-in: 144 hours with an added test after 72 hours
- Circuit states were exercised--i.e., dynamic burn-in

This 6-hour burn-in was calculated to be equivalent to over 200,000 power-on hours.
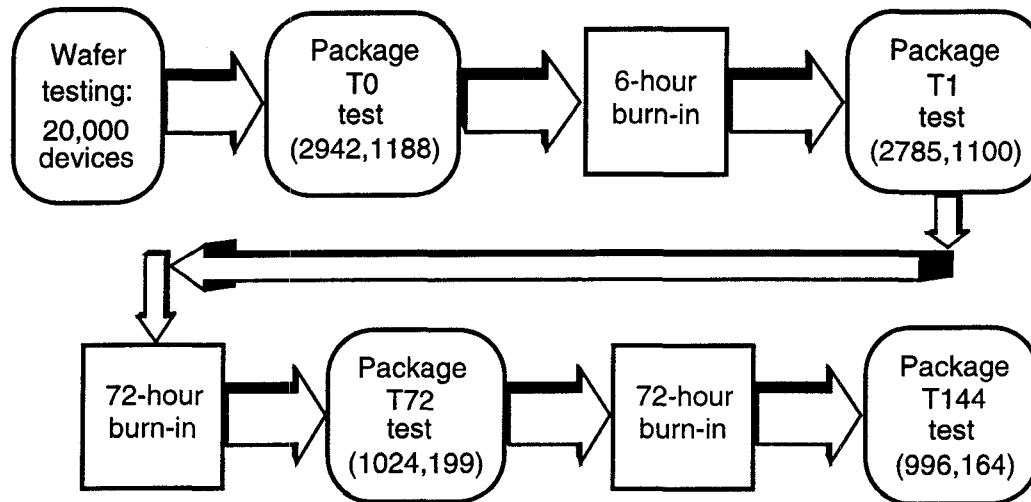
Figure 4. Experiment flow. The numbers in parenthesis represent the number of delta devices and control devices at each test step.

7. Test & burn-in flow

Figure 4shows the basic flow of the test and burn-in steps. The terms T0, T1, T72, T144 were used to represent the respective test steps. Note that the number of devices in each test step is shown in parenthesis (delta devices listed first, then control devices).

Note that only a sample of devices from T1 test went through the extended burn-in (T72 and T144) steps.

In addition to the test steps shown below, a number of devices went through further characterization testing. The applied tests were identical at each test step--e.g., pre-burn-in and post-burn-in. Although tests were added to package-level testing that were not performed at the wafer level, no wafer-level test was removed or changed. Wafer level testing was performed at 50°C while all package-level tests were applied at room temperature (25°C). (Two different temperatures were intentionally chosen to add additional information on temperature dependence of defects.)

8. Physical failure analysis

It is important to understand as much as possible about the physical mechanisms causing the faulty circuit behaviors. This is particularly true for defect mechanisms that passed some test methods and failed others. We are planning to perform physical failure analysis for at least 40 samples.

Although this is a relatively small sample compared with the total number of devices, the intent is to determine the root cause of the unique failures in each test category.

We plan to look at a variety of samples including:
- IDDq-only failures
- timing-related (only) failures
- functional test-only failures
- logical failures (not timing related) that passed the stuck-fault vectors
- post-burn-in failures

9. IDDq fault simulation & diagnosis

As part of the failure analysis portion of this project, IDDq fault simulation and diagnosis was developed and evaluated. This software has been used to help determine the physical location of defects based on testing results. Also, the fault simulation results can be used to compare various fault models with hardware measurements.

The IDDq diagnostic software implements techniques similar to ones described earlier [7-10]. The software supported both the pseudo-stuck-at fault model and the bridging fault model. The bridging fault list was created by extracting adjacent wires from the device layout (285,000 potential bridging faults were extracted).

We have successfully applied this technique for a number of devices targetted at failure analysis. The general results of this evaluation demonstrates that this is a promising area for further investigation.

10. Summary

This experiment has generated a large amount of valuable test data which is still being analyzed. It is anticipated that various forms of analysis and hypothesis testing will continue using the data over the next several years. Aspects of the experimental work are continuing at this time. As experimental work and data analysis is completed, more results will be publicized.

We are interested in feedback related to this project.
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