Outline

• Plastic Packages
• Stress and Test Flows
  • Thermal Mechanisms
• Moisture Mechanisms
• Thermo-mechanical Mechanisms
• Moisture-mechanical Mechanisms
• Technology Update
Focus Topic: Acceleration

• Acceleration between two stresses is the ratio of times (or cycles) to achieve the same effect.

• The “same effect” could be the same fraction failing.

  – eg. The ratio of median (not mean!) times to failure in different stresses is the Acceleration Factor (AF).

  • AF is proportional to $1/\text{MTTF}$

$$AF(2 \mid 1) = \frac{\text{MTTF}_1}{\text{MTTF}_2} = \exp\left\{ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right\} \quad \text{Thermal ("Arrhenius")}$$

$$AF(2 \mid 1) = \frac{\text{MTTF}_1}{\text{MTTF}_2} = \exp\left\{ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right\} \exp\{C (V_2 - V_1)\} \quad \text{Thermal and Voltage}$$

$$AF(2 \mid 1) = \frac{\text{MTTF}_1}{\text{MTTF}_2} = \left\{ \frac{a + bV_2}{a + bV_1} \right\} \left\{ \frac{RH_2}{RH_1} \right\}^m \exp\left\{ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right\} \quad \text{Moisture ("Peck")}$$

$$AF(2 \mid 1) = \frac{\text{MCTF}_1}{\text{MCTF}_2} = \left\{ \frac{\Delta T_2}{\Delta T_1} \right\}^m \quad \text{Thermal Cycle ("Coffin-Manson")}$$
Test chip failure data is at conditions different from external stress.

Product predictions require 1) AF model, 2) Transformation model.

Many “what-if” calculations involve only the Transformation model.
Thermal Mechanisms

ELFR
- Early life failure rate.
  - 168 hrs
  - JESD22-A108

HTOL
- High temperature operating life.
  - 168 - 1000 hrs
  - JESD22-A108

HTSL (Bake)
- 1000 hrs
  - JESD22-A103

TC
- 700 cycles
  - 3 cycles/hr
  - 233 hrs
  - JESD22-A104
- Condition B or G
  (C is too severe)

THB or HAST
- 1000 hrs (85/85)
  - JESD22-A101
- 96 hrs (130/85)
  - JESD22-A110

Preconditioning.
- JESD22-A113
Gold-Aluminum Bond Failure

• Gold and Aluminum interdiffuse.
  – Intermetallic phases such as AuAl$_2$ (“Purple Plague”) form.
  – Imbalance in atomic flux causes Kirkendall voiding.
  – Bromine flame retardant is a catalyst.

• Kirkendall voids lead to
  – Bond weakening - detected by wire pull test.
  – Resistance changes in bond - detected by Kelvin measurement of bond resistance.
Thermal (Ordinary) Purple Plague

Cross-section of gold ball bond on aluminum pad after 200 hours at 160°C
Arrhenius plot of time to 10% of wire pull failure. Activation energy (Q) = 1.17 eV.

Source: S. Ahmad, Intel

Linear in 1/T (°K), with ticks placed at T (°C).
Gold-Aluminum Bond Failure

- Kelvin resistance measurements.
- Resistance increase of Au bonds to Al pads vs bake time.
- Bake at 200 °C.
- Various levels of Br flame-retardant in molding compound.
- Br catalyzes Au-Al intermetallic growth.
- Br flame retardants are being phased out today.

Thermal Degradation of Lead Finish

- Only an issue for copper lead frames (not Alloy 42).
- $\text{Cu}_3\text{Sn}$ or $\text{Cu}_6\text{Sn}_5$ inter-metallic phases grow at the interface between solder or tin plating.
- Activation energy ($Q$) for inter-metallic phase growth is 0.74 eV.
- If inter-metallic phase grows to surface of solder or tin plate, solder wetting will not occur.
- Main effect is to limit the number of dry-out bakes of surface mount plastic components.
Thermal Degradation of Lead Finish

Post-plating solder plate

Post burn-in solder plate showing copper-tin intermetallic
Thermal Degradation of Lead Finish

X-section of solder-\textit{plated} lead

X-section of solder-\textit{coated} lead
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Example Stress Flow

Early life failure rate.
168 hrs
**JESD22-A108**

High temperature operating life.
168 -1000 hrs
**JESD22-A108**

**ELFR**

**HTOL**

**HTSL (Bake)**
1000 hrs
**JESD22-A103**

**TC**
700 cycles
3 cycles/hr
233 hrs
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Condition B or G
(C is too severe)

**THB or HAST**
1000 hrs (85/85)
**JESD22-A101**
96 hrs (130/85)
**JESD22-A110**

Preconditioning.
**JESD22-A113**
H$_2$O Diffusion/Absorption in MC

MODEL

Surface exposed to ambient.

Zero flux or "die" surface

ACTUAL

Surface exposed to ambient.

Plastic Molding Compound (MC)
H₂O Diffusion/Absorption in MC

**Diffusion Coefficient:**

\[ D = D_0 \exp\left( -\frac{Q_d}{kT} \right) \]

\[ D_0 = 4.7 \times 10^{-5} \text{ m}^2/\text{sec} \quad Q_d = 0.50 \text{ eV} \]

**Saturation Coefficient:**

\[ S = S_0 \exp\left( \frac{Q_s}{kT} \right) \]

\[ S_0 = 2.76 \times 10^4 \text{ mole/m}^3 \text{Pa} \quad Q_s = 0.40 \text{ eV} \]

**Henry’s Law:**

\[ M_{\text{sat}} = PS = HP_{\text{sat}}S \]

Source: *Kitano, et al IRPS 1988*

**Key Observation:** Saturated moisture content of molding compound is nearly independent of temperature, and is proportional to RH.

\[ M_{\text{sat}} = HP_0S_0 \exp\left[ \frac{(Q_s - Q_p)}{kT} \right] \]

\[ Q_s - Q_p = -0.02 \text{ eV} \]

Nearly zero!
H₂O Diffusion/Absorption in MC

\[ \frac{C - C_{\text{init}}}{C_{\text{eq}} - C_{\text{init}}} \quad \text{or} \quad \frac{M - M_{\text{init}}}{M_{\text{eq}} - M_{\text{init}}} \]

\[ \text{Fourier Number} = \frac{D t}{L^2} \]

Total Weight Gain (M)
Concentration at Die Surface (C)

0.8481
Response to Step-Function Stress

Typical Use Saturation Times

Package Moisture Time Constant (time to 90% saturation)

\[ t(\text{sat}) = \frac{L^2}{D_0} \exp\left(\frac{Q_d}{kT_{mc}}\right) \]

Typical 130/85 HAST Saturation Times

Normal Operating Range
Cyclical Stress
One-Dimensional Diffusion Equation Solutions
8 hours on, 16 hours off cycling for PDIP

T(ambient) = 100 °C, t(sat) = 28 hours
T(ambient) = 60 °C, t(sat) = 153 hours

Moisture concentration at the die is constant if Period << t(sat)
Peck’s Acceleration Model

• Fundamental environmental parameters are \( T, H \) and \( V \), \textit{at the site} of the failure mechanism.
  – If the die is the site, this is denoted by “\( j \)”.

• A frequently used acceleration model is due to Peck

\[
AF = (a + b \times V) \times H_j^m \times \exp(-Q / kT_j)
\]

• Find \( a, b, m, Q \) from experiments with steady-state stress and negligible power dissipation.

• Typically \( a \) is small or zero: Bias is required.

• Requires \( H > 0 \) for acceleration: Moisture is required.
Moisture and Temperature Fails

- Humidity gives a layer of water on most surfaces
  - Water also diffuses into the substrate
- Water + voltage $\rightarrow$ metal ions in water
- Metal can deposit in other locations or migrate

Water layer (in humid environment)
Metal ions dissolved in water
Metal deposited in a new location
Water and metal also diffuse through the substrate
Moisture: MM Tape Leakage
Moisture: MM Tape Leakage

Experimental Tape Data:

<table>
<thead>
<tr>
<th>Tape</th>
<th>m</th>
<th>Q  eV</th>
</tr>
</thead>
<tbody>
<tr>
<td>“A”</td>
<td>&gt;12</td>
<td>0.74</td>
</tr>
<tr>
<td>“B”</td>
<td>5</td>
<td>0.77</td>
</tr>
</tbody>
</table>

Source: C. Hong, Intel, 1991

Acceleration factor is proportional to bias.

\[ AF = \text{Constant} \times V \times H^m \exp\left(-\frac{Q}{kT}\right) \]
Moisture: Internal Metal Migration

• TAB Inter-lead Leakage/Shorts
  – Accelerated by voltage, temperature and humidity
  – Seen as early as 20 hrs 156/85 HAST
  – Highly dependent on materials & process

Copper dendrites after 40 hours of biased 156/85 HAST
Copper Migration (bulk)

Tin Migration (surface)

Copper Halo (bulk)

Dendrite growth (bulk)
Lead-Stabilizing Tape Leakage

- A vendor process excursion.
- Leakage observed after 336 hours of steam.
- Re-activated by 48 hours at 70C/100% RH
- No leakage seen between leads not crossed by tape
- Rapid decay for leads crossing end of tape
  - Tape dries from exterior inwards

Tape provides mechanical stability to long leads during wirebond.
Lead-Stabilizing Tape Leakage

![Graph showing recovery time and leakage current for pins crossed and not crossed by tape.](image)

Source: S. Maston, Intel
Aluminum Bond Pad Corrosion

\[ AF = \text{Constant} \times V \times H^m \exp(-Q / kT) \]

<table>
<thead>
<tr>
<th>Source</th>
<th>(m)</th>
<th>(Q) (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peck (a)</td>
<td>2.66</td>
<td>0.79</td>
</tr>
<tr>
<td>Hallberg &amp; Peck (b)</td>
<td>3.0</td>
<td>0.9</td>
</tr>
</tbody>
</table>

(a) IRPS, 1986; (b) IRPS, 1991.


Shortest path has highest failure rate.
Passivation in Plastic Packages

• Passivation is the final layer on the die.

• Passivation has two main functions:
  – Moisture Barrier
    • Molding compound is not a moisture barrier.
    • Silicon oxides are not good moisture barriers.
    • PECVD silicon nitride or silicon oxynitride film is a good barrier.
    • Film must be thick enough to avoid pinholes, coverage defects.
  – Mechanical Protection
    • Silicon nitride films are brittle.
    • Polyimide compliant film protects silicon nitride.
    • Polyimide can react with moisture (depending on formulation).
Polyimide/Au Bond Failure

- Bonds overlapping passivation don’t necessarily violate design rules.
- But can activate polyimide-related “purple plague” failure mechanisms in combination with moisture.
- Acceleration modeling showed no field jeopardy.
Wire Bond Pull Test
Moisture-Related Gold Bond Degrad’n

Effect of 80 hours of 156/85 HAST vs 156/0 Bake and Centered vs Off-Centered Bonds on Wire Pull Test Data

Source: G. Shirley and M. Shell, IRPS, 1993
Moisture-Related Gold Bond Degrad’n

Wire Pull Strength of Polyimide vs No Polyimide and Centered vs Off-Centered Bonds after 40 hours of 156/85 HAST

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993
Moisture-Related Purple Plague

Cross-section of gold ball bond on aluminum pad after 80 hours at 156C/85%RH
Moisture-Related Gold Bond Degrad’n

\[ b = 112.7 \text{ gm} \]
\[ a_0 = 1.13 \times 10^{10} \text{ (gm - hrs)}^{-1} \]
\[ m = 0.98; \quad Q = 1.15 \text{ eV} \]

\[ F_{50} = \frac{1}{\sqrt{(at)^2 + 1/b^2}} \]
\[ a = a_0 \times h^m \times \exp(-Q/kT) \]
\[ F_p = F_{50} \times \exp(-\sigma \times Z_p) \]
\[ \sigma = 0.17 \]

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993
Circuit Failure Due to Passiv’n Defects

Site of failing bit. SRAM after HAST stress.
Courtesy M. Shew, Intel
Circuit Failure Due to Passiv’n Defects

Etch-decorated cross-section of passivation. Note growth seams.
Circuit Failure Due to Passiv’n Defects

SRAM VOLTAGE THRESHOLD MAP FOR CELL PULLUP TRANSISTOR
(Baseline threshold is 0.89 V. Passivation is 0.6 μ nitride, no polyimide.)

After 120 h 156/85. 4 failed bits with Vt > 2.5 V
2 bits recover after further 2 hr bake at 150 C

Source: C. Hong, Intel
Acceleration Model Fit of HAST Data

SRAM HAST and 85/85 Bit Failures (No Polyimide)

\[ AF = \text{Constant} \times (a + bV) \times H^m \times \exp(-Q / kT) \]

\[ a = 0.24 \quad b = 0.14 \quad m = 4.64 \quad Q = 0.79 \text{ eV} \]

Notes:
- “Standby” = 5.5V bias, low power
- “Active” = 5.5V bias, high power
- 156/85: non-standard, limit of pressure vessel.
- Source: C. G. Shirley, C. Hong. Intel
# Peck Model Parameters

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>$Q$(eV)</th>
<th>$m$</th>
<th>$Q/m$</th>
<th>$Q/m &lt; 0.42eV?$</th>
<th>Hours of 130/85 $\equiv$ 1kh 85/85</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>MM Tape A</td>
<td>0.74</td>
<td>12</td>
<td>0.06</td>
<td>Yes</td>
<td>69</td>
<td>2</td>
</tr>
<tr>
<td>MM Tape B</td>
<td>0.77</td>
<td>5</td>
<td>0.15</td>
<td>Yes</td>
<td>62</td>
<td>2</td>
</tr>
<tr>
<td>Single Bit SRAM</td>
<td>0.79</td>
<td>4.6</td>
<td>0.17</td>
<td>Yes</td>
<td>57</td>
<td>3</td>
</tr>
<tr>
<td>Corrosion, THB (early Peck)</td>
<td>0.79</td>
<td>2.66</td>
<td>0.30</td>
<td>Yes</td>
<td>57</td>
<td>4</td>
</tr>
<tr>
<td>Corrosion, THB (later Peck)</td>
<td>0.90</td>
<td>3</td>
<td>0.30</td>
<td>Yes</td>
<td>39</td>
<td>5</td>
</tr>
<tr>
<td>Bond Shear</td>
<td>1.15</td>
<td>0.98</td>
<td>1.17</td>
<td>No</td>
<td>16</td>
<td>6</td>
</tr>
</tbody>
</table>

Yes/No: Increasing power dissipation at die, slows/accelerates the moisture mechanism.

Homework 11

1. Show that, for the 6 moisture mechanisms on slide 40, 100 h of 130/85 stress is equivalent to 1000 h or more of 85/85 stress.

2. A product operates in an ambient of 25 °C and 85% RH. When in standby mode, the product dissipates negligible power. When in “active” mode the product dissipates sufficient power that the die temperature is 5 °C hotter than ambient. For each mechanism on slide 40, calculate the acceleration of the active mode relative to the standby mode.

Suggestion: Make a new sheet in the “Rel Calculator” tool. Useful functions (Psat and Arrhenius) are available there. AltF11 will allow you to see the code if you want to see documentation of the functions.
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• Technology Update
Thermomechanical Mechanisms

ELFR

- Early life failure rate.
- 168 hrs

**JESD22-A108**

HTOL

- High temperature operating life.
- 168 -1000 hrs

**JESD22-A108**

HTSL (Bake)

- 1000 hrs

**JESD22-A103**

PC

TC

- 700 cycles
- 3 cycles/hr
- 233 hrs

**JESD22-A104**

THB or HAST

- 1000 hrs (85/85)

**JESD22-A101**

- 96 hrs (130/85)

**JESD22-A110**

Condition B or G

(C is too severe)
Key Material Properties

- Material properties which drive temperature cycling-induced failure mechanisms.

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Coeff’t of Expansion (ppm/°C) “TCE”</th>
<th>Young's Modulus (GPa)</th>
<th>Thermal Conductivity (W/m °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>17</td>
<td>119</td>
<td>398</td>
</tr>
<tr>
<td>Alloy 42</td>
<td>5 Match!</td>
<td>145</td>
<td>15 Low!</td>
</tr>
<tr>
<td>Silicon</td>
<td>3</td>
<td>131</td>
<td>157</td>
</tr>
<tr>
<td>Molding Compound</td>
<td>21</td>
<td>18</td>
<td>0.6</td>
</tr>
<tr>
<td>Alumina</td>
<td>6.5</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>PC Board</td>
<td>15-17</td>
<td>11</td>
<td>25</td>
</tr>
</tbody>
</table>
Cracking Due to Temperature Cycle

[Diagram showing stress distribution with and without cracks, indicating shear stress, normal stress, crack presence, and bond and TFC damage.]
Crack Propagation in Test Conditions

• Tensile Test of Notched Samples
  – Measure crack growth rate for sinusoidal load:

  
  
  
  
  – Sample geometry and load determine stress intensity factor, $K$.
  – Plot crack growth rate $da/dN$ versus $K$ on log-log plot to determine Coffin-Manson exponent, $m$:
Crack Propagation in Test Conditions

Slope of lines on log-log plot

\[ \frac{da}{dN} = Const \times (\Delta K)^m \]

\( m \approx 20 \)

Crack Propagation in Package

• The rate of crack propagation is also given by

\[
\frac{da}{dN} = Const \times (\Delta K)^m
\]

• But in plastic packages under temperature cycling, the stress concentration factor is

\[
\Delta K = Const \times (\alpha_{molding compound} - \alpha_{silicon}) \times (T_{min} - T_{neutral})
\]

• \(\alpha\) is the TCE of MC.

\(\Delta T\) in temperature cycling-driven models is the temperature difference between the neutral (usually cure) temperature, and the minimum temperature of the cycle. \(T_{max}\) is less important.
Package Cracking and Delamination...

..damages Wires, Bonds, and Passivation Films.

Silicon

Substrate Damage

Thin-Film Cracking

Normal (tensile)

Shear

Crack

Wire Shear

Au
Bond Damage: Wires and Ball Bonds

• Cracks can intersect wires, TAB leads.
• Bonds can be sheared at the bond/pad interface
• Shear and tensile normal stress can break wires at their necks.
• Substrate cracks induced during bonding can propagate and cause “cratering” or “chip-out”.

Wire Damage

Wires sheared by wire crack

(Open)
Ball bonds in plastic package after temperature cycle.
Bond Damage

Necking Damage
Bond Damage

Necking fracture
Bond Damage

Delamination induced down bond fail after temperature cycle
Bond Damage

Cratering damage on bond pads
Bond Damage

Bond shear at die corners after temperature cycle
Bond Damage and Delamination

Pulse-echo acoustic image of mold compound/die interface in four devices. Delamination is shown in black. White boxes added to show locations of low bond wire pull strength results.

Intermetallic fracture at bond due to shear displacement.

44 PLCC devices that failed after solder reflow and 1000 cycles (-40 to 125°C)

TAB cratering and diffusion barrier damage revealed by wet etch.
Bond Damage (TAB)

TAB bonds Au/Al intermetallic formed at cracks in Ti barrier
Bond Damage (TAB)

Crater under TAB bonds
Thin-Film Cracking (TFC)

- Au Substrate Damage
- Silicon
- Shear
- Normal (tensile)
- Crack
- Wire Shear

Thin-Film Cracking

Substrate Damage

100 microns

20 microns
TFC - Plastic Conforms to Die Surface

Die Surface

Replica in Plastic
TFC – Effect on Thin Films

Shear stress applied to passivation

Die center

Cracks

Passivation

Crack

Aluminum

PSG

Channel

Polysilicon

SiO2

Winter 2013

ECE 510  C. G. Shirley, S. C. Johnson
Passivation delamination crack propagates into substrate.
Test Chip

• Thin film cracking can be detected electrically by test structures in the corner of the die.
  – Sensitive to opens and to shorts.

• Buss width is varied to determine design rule.

![Diagram of test chip with labels for TFC, TFD, ATC, bond pads, and die edge.]

- Edge ring
- Die edge (saw cut)
- TFC sensor
- Metal 5
- Metal 4
- Via 4
- Minimum

X = 10, 20, 40, 100 microns
TFC – Effect of Buss Width

Factors Affecting TFC: Buss Width Effect

Polysilicon meanders under buss edge are vulnerable to crack-induced opens.

Narrow buss, or contacts, stabilizes buss, reduces incidence of TFC. Leads to buss width design rules, and buss slotting in die corners.
TFC – Effect of Temperature Cycle

- Drivers: T/C conditions, and number of cycles.
- **Minimum** T/C temperature, not amplitude, is key aspect of stress.
  - Stress depends on difference between cure temperature (neutral stress) and minimum stress temperature.

![Graph showing cumulative percentage of failure vs. cycles for different temperature ranges.]

• Fraction of PDIP-packaged SRAM failing.
• Post 1K cycle of T/C C.
• No Polyimide die coat.
• Thicker passivation is more robust.

Source: A. Cassens, Intel
TFC – Effect of Compliant Overcoat

- SRAM in PDIP
- Temperature Cycle Condition C
- Polyimide Overcoat

<table>
<thead>
<tr>
<th></th>
<th>200 cycles</th>
<th>500 cycles</th>
<th>1000 cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Polyimide</td>
<td>0/450</td>
<td>13/450</td>
<td>101/437</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0/450</td>
<td>0/450</td>
<td>0/450</td>
</tr>
</tbody>
</table>
Theory of TFC

• Shear stress applied to die surface by MC
  – Is maximum at die corners
  – Zero at die center.

\[ \sigma \text{(At die Surface)} \]
Theory of TFC, ct’d

- Buss width effect: Okikawa et. al.
- Passivation thickness effect: Edwards et al.
- TFC occurs when and where

\[ \sigma(\text{Passivation Surface}) > K \times E \times \left(\frac{t}{L}\right)^2 \]

- \( K \) = dimensionless constant
- \( E \) = Young’s modulus of passivation
- \( t \) = Passivation thickness
- \( L \) = Buss width

**Thicker passivation, and/or narrower busses implies less TFC.**

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Thin Film Delamination

- Saw cut exposes thin film edges to moisture..
- And shear stress tends to peel films.

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Other films

PECVD Oxynitride/Nitride

Polyimide

Metal Bond Pad

Silicon

Thin films

Substrate (Si)

Shear stress

Thin film delamination.

Moisture
Test Chip

• “Edge rings” are lateral moisture barrier.
• Effectiveness of edge rings can be tested electrically by a TFD sensor on a test chip.

Cross section of TFD sensor
Thin-Film Delamination

Delamination at die edge after 168 hours of steam.

Edge ring

TFD Sensor

Source: C. Hong
Intel
Delamination at die edge after 168 hours of steam.
Popcorn Mechanism

ELFR
- Early life failure rate.
  - 168 hrs
  - JESD22-A108

HTOL
- High temperature operating life.
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HTSL (Bake)
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- 700 cycles
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  - 233 hrs
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THB or HAST
- 1000 hrs (85/85)
  - JESD22-A101

Preconditioning.
- JESD22-A113

Condition B or G (C is too severe)
Popcorn Mechanism

Plastic package cracking due to “popcorn” effect during solder reflow
Popcorn Damage

Plastic package cracking due to “popcorn” effect during solder reflow
Pulse-echo acoustic image through back of 68PLCC that developed popcorn cracks during solder reflow

Popcorn Damage

Pulse-echo acoustic image through top (delamination in black)

Delamination

Crack

Acoustic time-of-flight image indicating package crack

Crack

Die

Real-time x-ray image showing deformation in wires where they intersect the crack

Deformed Bond Wires

132 lead PQFP which was damaged during solder reflow.

Factors Affecting Popcorning

- Peak temperature reached during soldering.
- Moisture content of molding compound.
- Dimensions of die paddle.
- Thickness of molding compound under paddle.
- Adhesion of molding compound to die and/or lead frame.
- Mold compound formulation.

Not on this list: Pre-existing voids in the plastic package.
Popcorn Model, Internal Pressure

Water Concentration Profile
Cavity = 0.05 mm, Precond = 25/85, Tsolder = 215 °C
Package Thickness = 0.60 mm

Cavity Water Vapor Concentration

Time (sec)

Moisture conc. in MC

Moisture conc. in cavity.
Popcorn Model, Internal Pressure

\[ P_{\text{cav}} \rightarrow 0; w \rightarrow \infty \text{ (or } t \rightarrow 0) \rightarrow H_0 \times P_{\text{sat}}(T_0) \times \frac{S(T_0)}{S(T_1)} \]

Delamination pressure exists even with no physical void.

Example:

- Unit preconditioned in 85/85 for a long time, then subjected to 215 C solder shock.
- Saturation coefficient has activation energy of 0.4 eV. (eg. Kitano et. al.)
- Steam table pressure at 85 C is 0.57 atm.

\[
P_{\text{cav}} = 0.85 \times 0.57 \times \exp\left\{ \frac{0.40 \text{ eV}}{8.62 \times 10^{-5} \text{ eV/°K}} \left( \frac{1}{273 + 85} - \frac{1}{273 + 215} \right) \right\}
\]

\[ = 15.3 \text{ Atmospheres} \quad \text{Wow!!} \]
Outline

• Plastic Packages
• Stress and Test Flows
• Thermal Mechanisms
• Moisture Mechanisms
• Thermo-mechanical Mechanisms
• Moisture-mechanical Mechanisms

Technology Update
This is an example of a packaged part as it might be used in a product.
This is a close-up of the package substrate showing the many layers of conductors and insulators.
Location: Silicon (vs. Package)

"Back end" = interconnects

"Front end" = transistors

Interlayer dielectric (ILD)
Metal interconnect
Via

Transistor

Source

Drain

Gate

Gate Oxide

Channel

Le

Slide: Scott C. Johnson