ECE 510, Lecture 11
Plastic Package Reliability, and Qualification Methodology

Glenn Shirley
Scott Johnson

Outline

- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- Technology Update

Focus Topic: Acceleration

- Acceleration between two stresses is the ratio of times (or cycles) to achieve the same effect.
- The "same effect" could be the same fraction failing.
  - eg. The ratio of median (not mean!) times to failure in different stresses is the Acceleration Factor (AF).
    - AF is proportional to 1/MTTF

"Activation energy"

$$AF(2|1) = \frac{MTTF_1}{MTTF_2} = \exp\left\{ \frac{Q}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right\}$$

Thermal ("Arrhenius")

$$AF(2|1) = \frac{MTTF_1}{MTTF_2} = \exp\left\{ \frac{Q}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right\} \exp\left\{ C\left(V_2 - V_1\right) \right\}$$

Thermal and Voltage

$$AF(2|1) = \frac{MTTF_1}{MTTF_2} = \left\{ \frac{a + bV_2}{a + bV_1} \right\} \left\{ \frac{RH_2}{RH_1} \right\}^m \exp\left\{ \frac{Q}{k_B}\left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right\}$$

Moisture ("Peck")

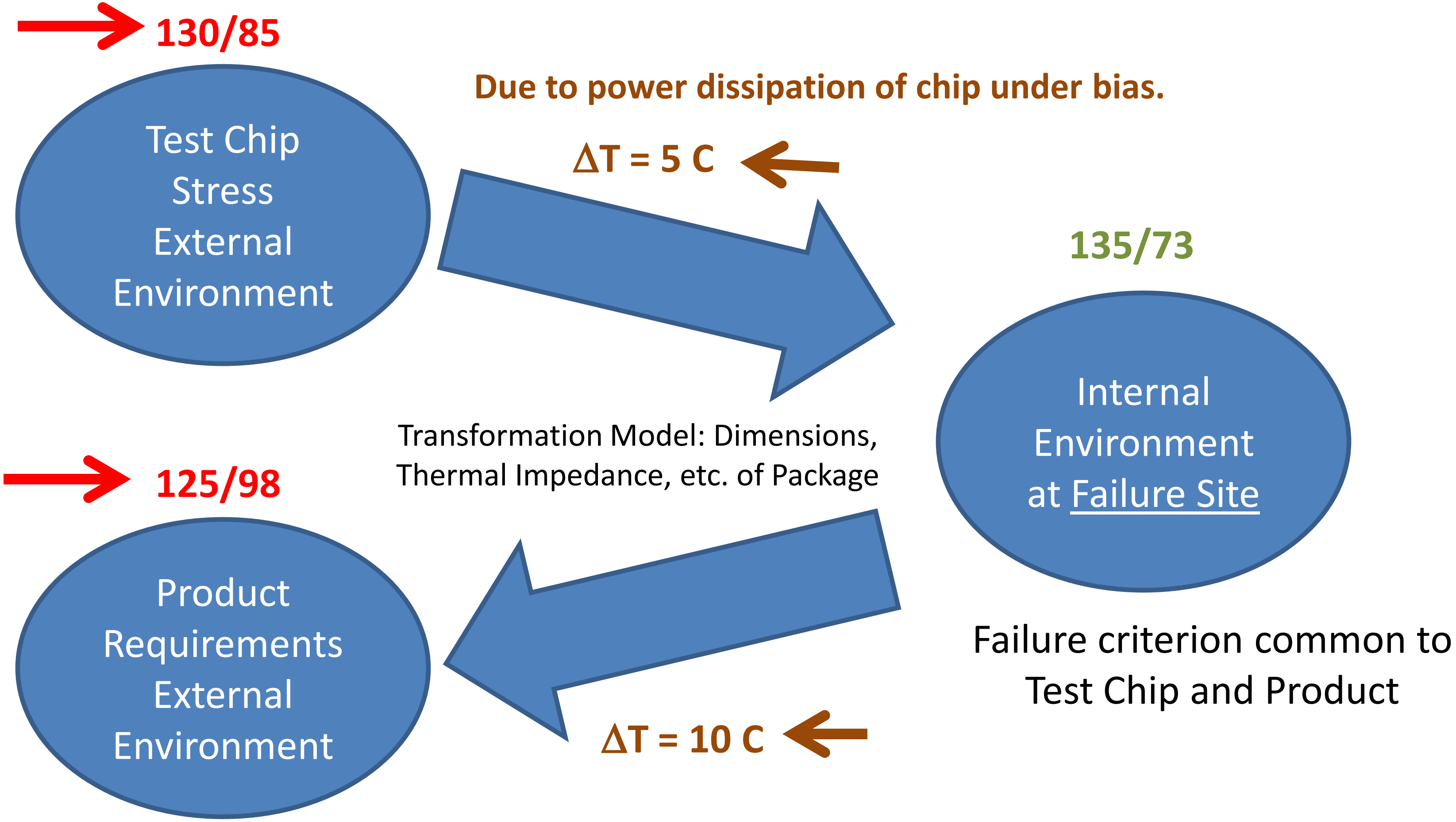
$$AF(2|1) = \frac{MCTF_1}{MCTF_2} = \left\{ \frac{\Delta T_2}{\Delta T_1} \right\}^m$$

Thermal Cycle ("Coffin-Manson")

"cycles"

External/Internal Transformation

Equivalent stress because stress at failure site is the same.



130/85

Test Chip Stress External Environment

Due to power dissipation of chip under bias.

ΔT = 5 C

135/73

Internal Environment at Failure Site

Transformation Model: Dimensions, Thermal Impedance, etc. of Package

125/98

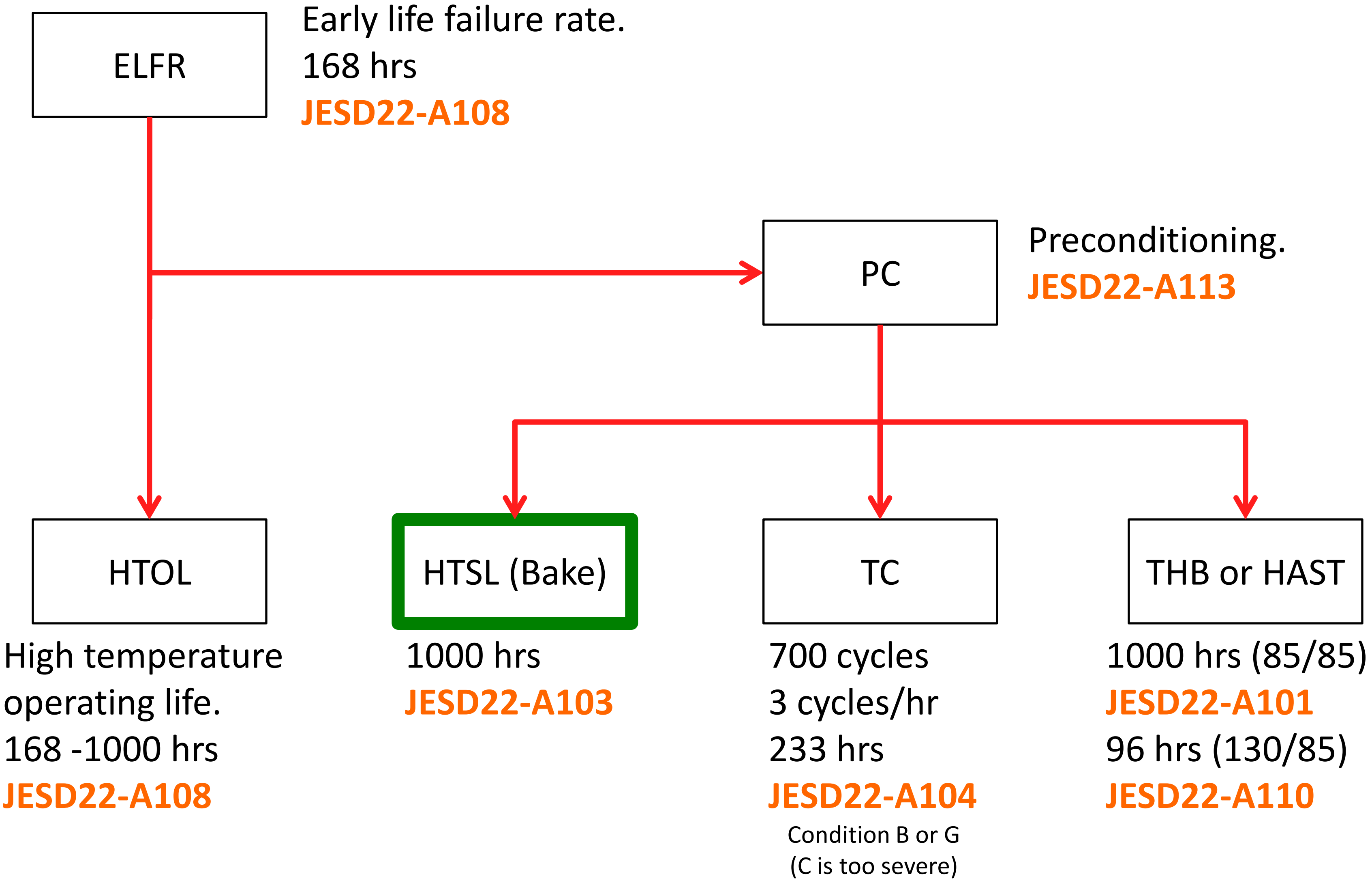
Product Requirements External Environment

Failure criterion common to Test Chip and Product

ΔT = 10 C

- Test chip failure data is at conditions different from external stress.
- Product predictions require 1) AF model, 2) Transformation model.
- Many “what-if” calculations involve only the Transformation model.

Thermal Mechanisms



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

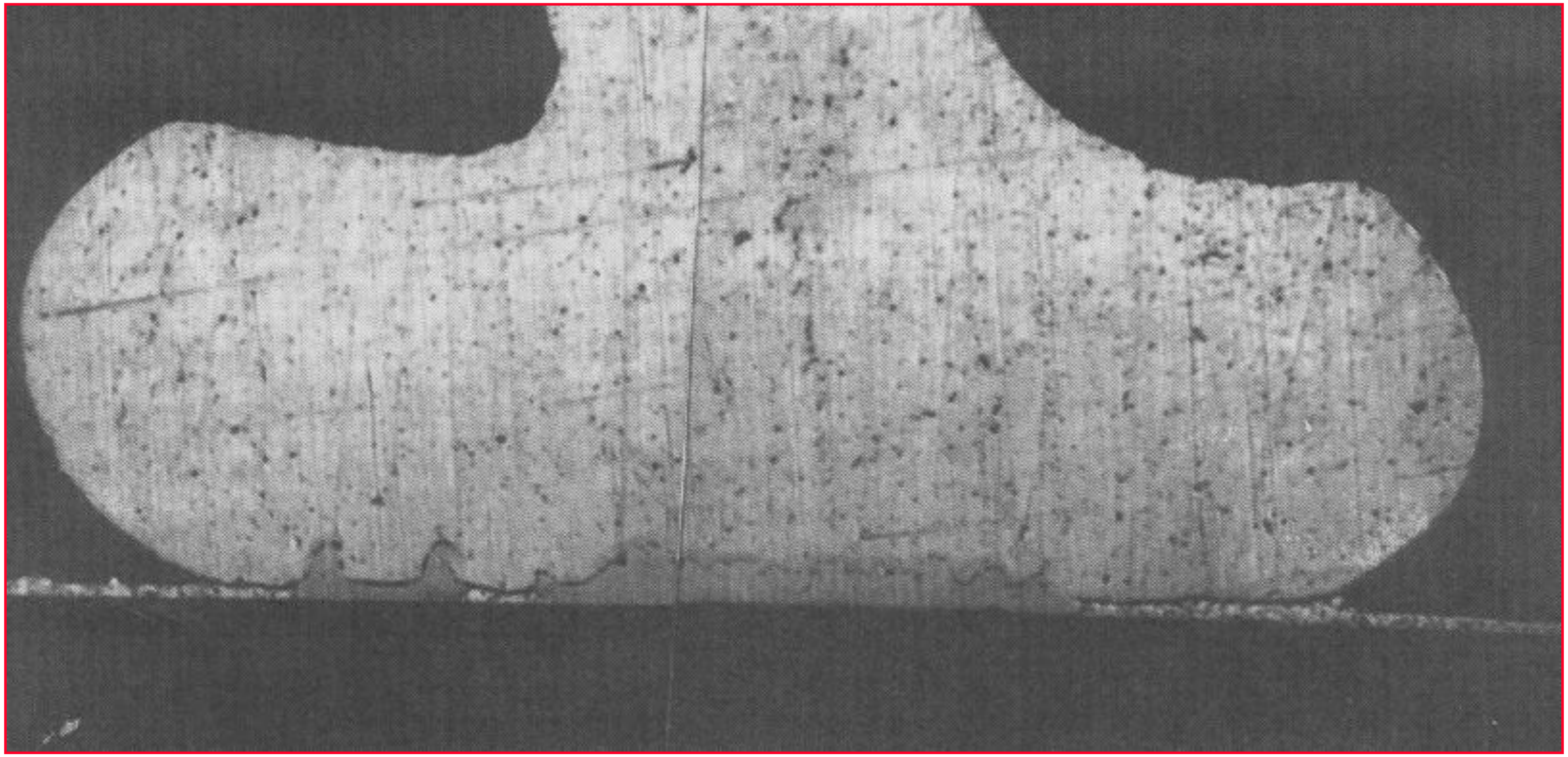
THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Gold-Aluminum Bond Failure

- Gold and Aluminum interdiffuse.
  - Intermetallic phases such as $AuAl_2$ ("Purple Plague") form.
  - Imbalance in atomic flux causes Kirkendall voiding.
  - Bromine flame retardant is a catalyst.
- Kirkendall voids lead to
  - Bond weakening - detected by wire pull test.
  - Resistance changes in bond - detected by Kelvin measurement of bond resistance.

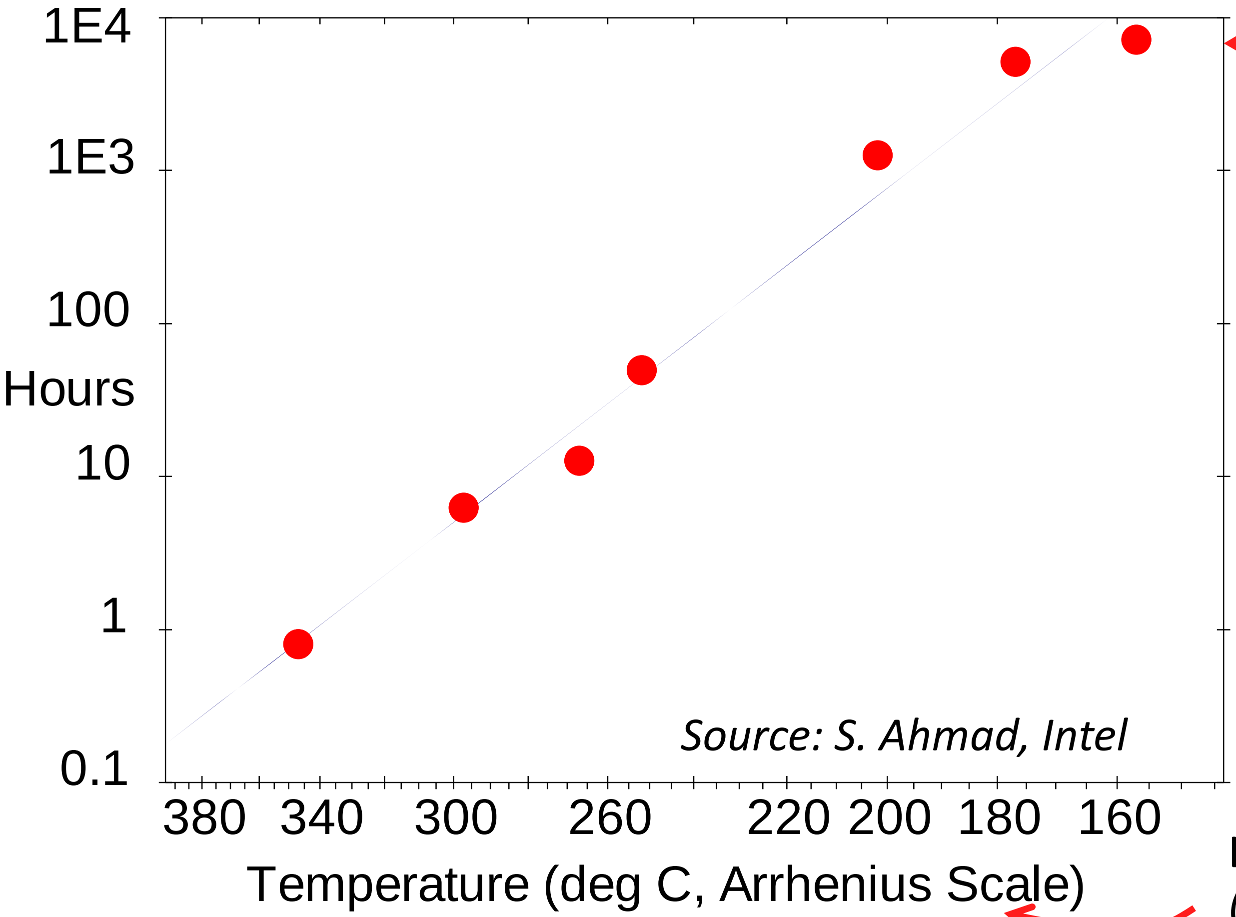
Thermal (Ordinary) Purple Plague



Cross-section of gold ball bond on aluminum pad
after 200 hours at 160°C

Gold-Aluminum Bond Failure

Log scale



Source: S. Ahmad, Intel

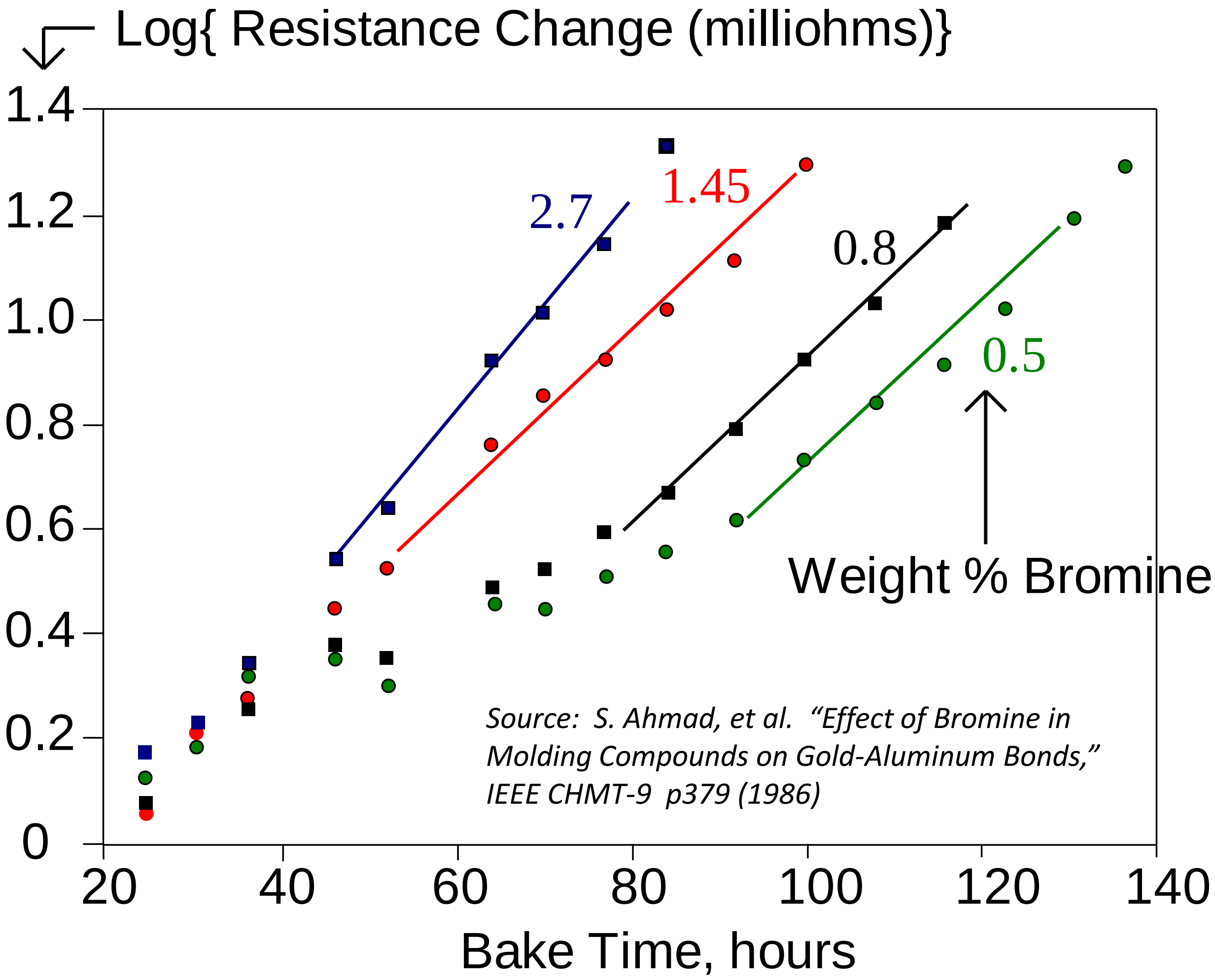
1 year (!)
(8760h)

Linear in 1/T (°K), with ticks placed at T (°C).

Arrhenius plot of time to 10% of wire pull failure.
Activation energy (Q) = 1.17 eV.

Gold-Aluminum Bond Failure

- Kelvin resistance measurements.
- Resistance increase of Au bonds to Al pads vs bake time.
- Bake at 200 °C.
- Various levels of Br flame-retardant in molding compound.
- Br catalyzes Au-Al intermetallic growth.
- Br flame retardants are being phased out today.

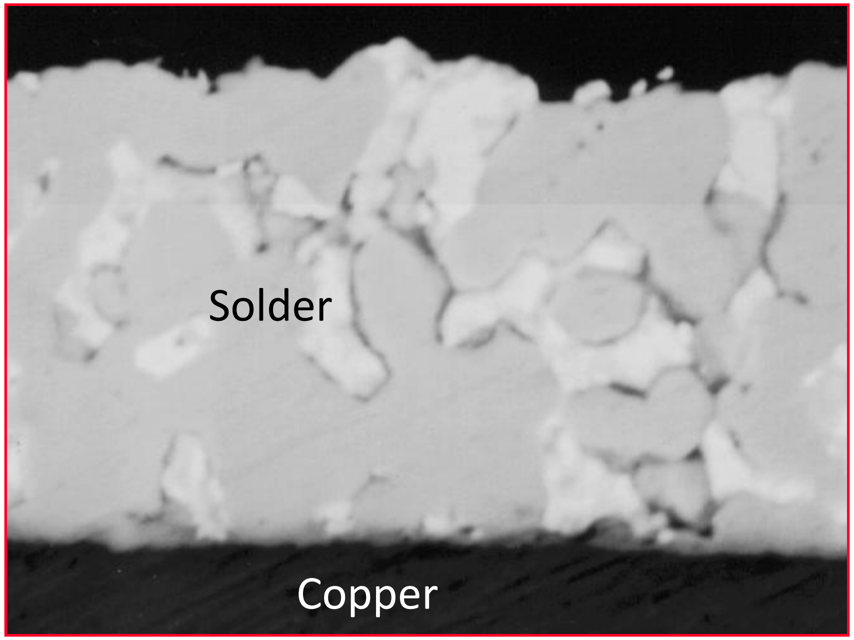


Source: S. Ahmad, et al. "Effect of Bromine in Molding Compounds on Gold-Aluminum Bonds," IEEE CHMT-9 p379 (1986)

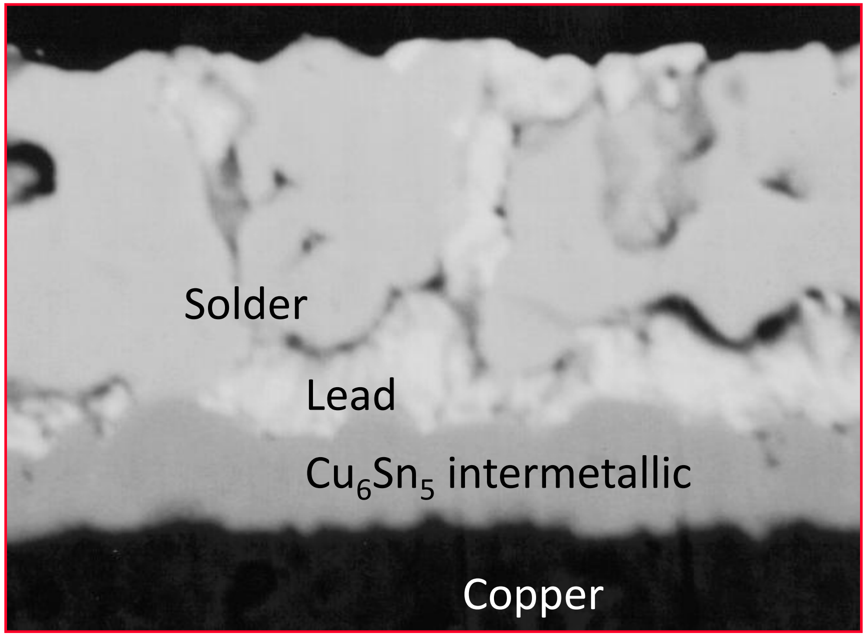
Thermal Degradation of Lead Finish

- Only an issue for copper lead frames (not Alloy 42).
- Cu_3Sn or Cu_6Sn_5 inter-metallic phases grow at the interface between solder or tin plating.
- Activation energy (Q) for inter-metallic phase growth is 0.74 eV.
- If inter-metallic phase grows to surface of solder or tin plate, solder wetting will not occur.
- Main effect is to limit the number of dry-out bakes of surface mount plastic components.

Thermal Degradation of Lead Finish

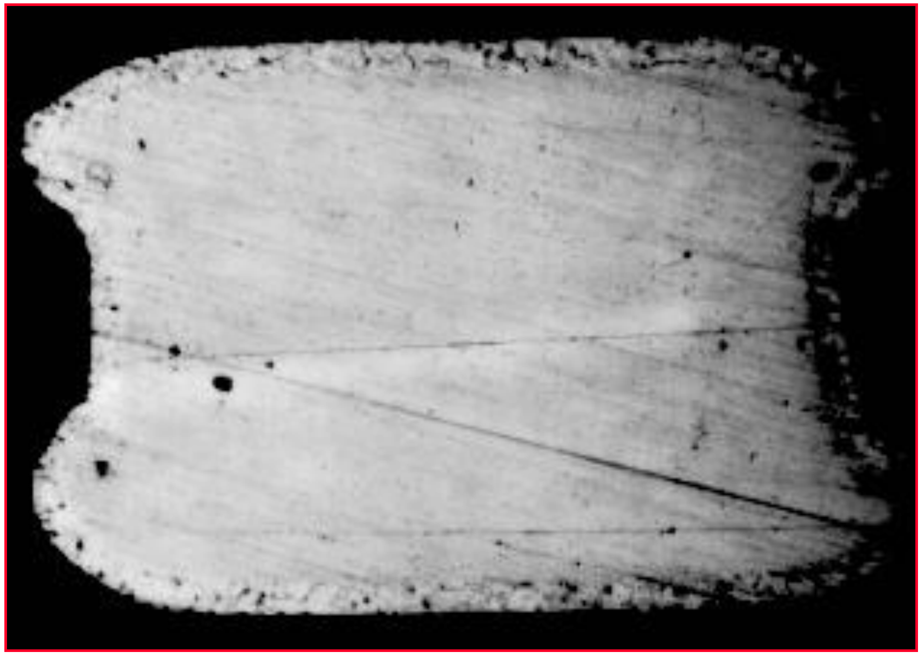


Post-plating solder plate

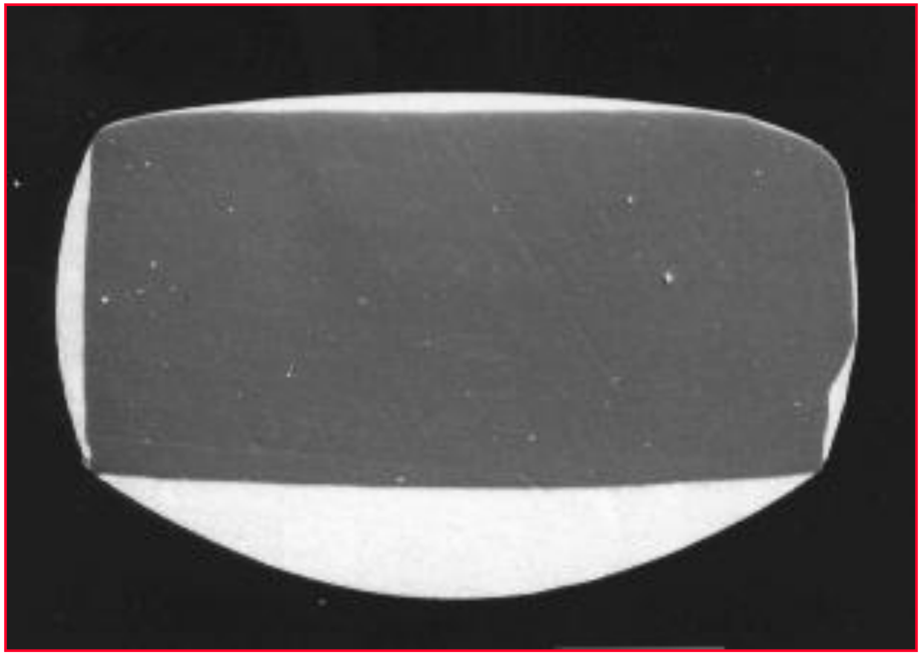


Post burn-in solder plate showing copper-tin intermetallic

Thermal Degradation of Lead Finish



X-section of solder-*plated* lead

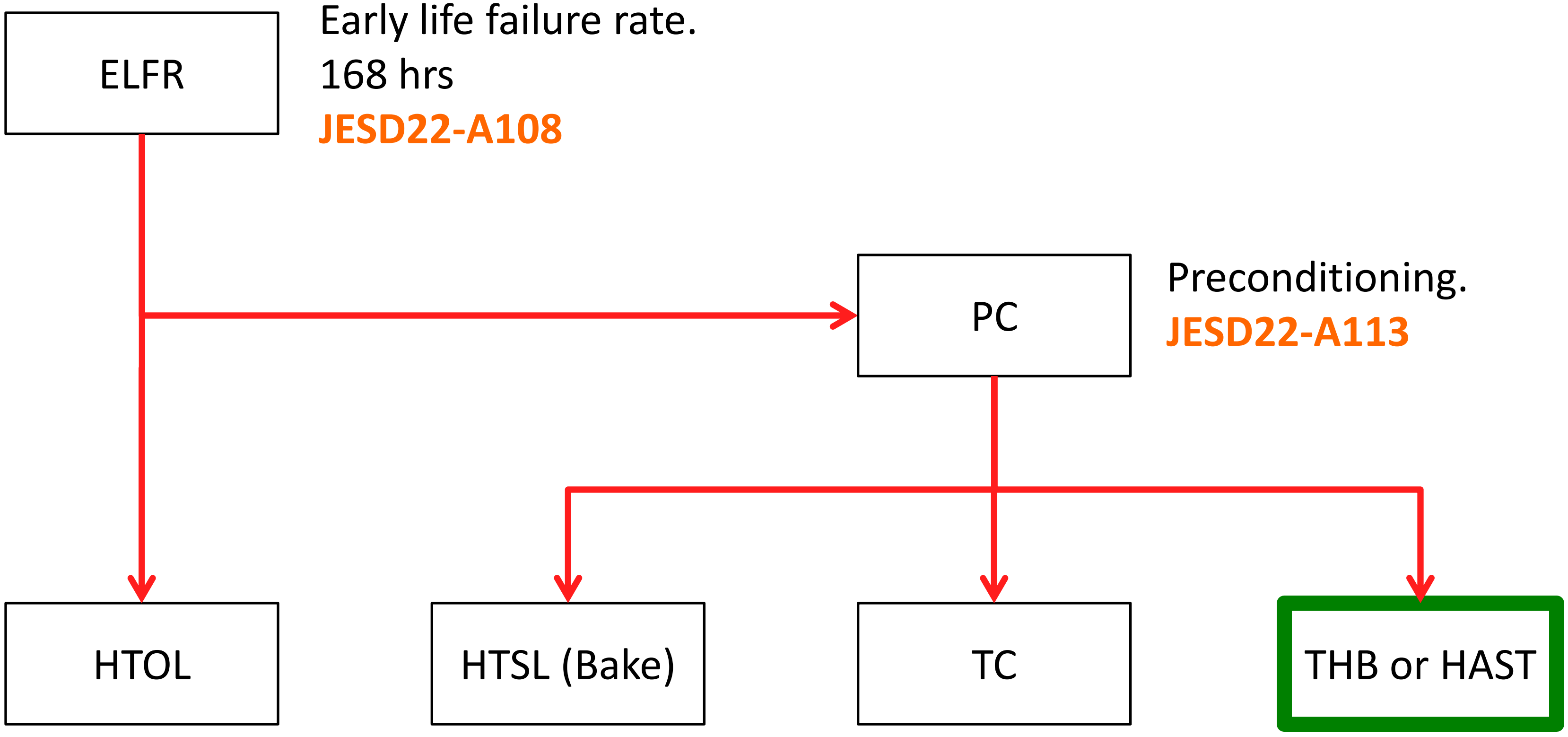


X-section of solder-*coated* lead

Outline

- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- Technology Update

Example Stress Flow



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

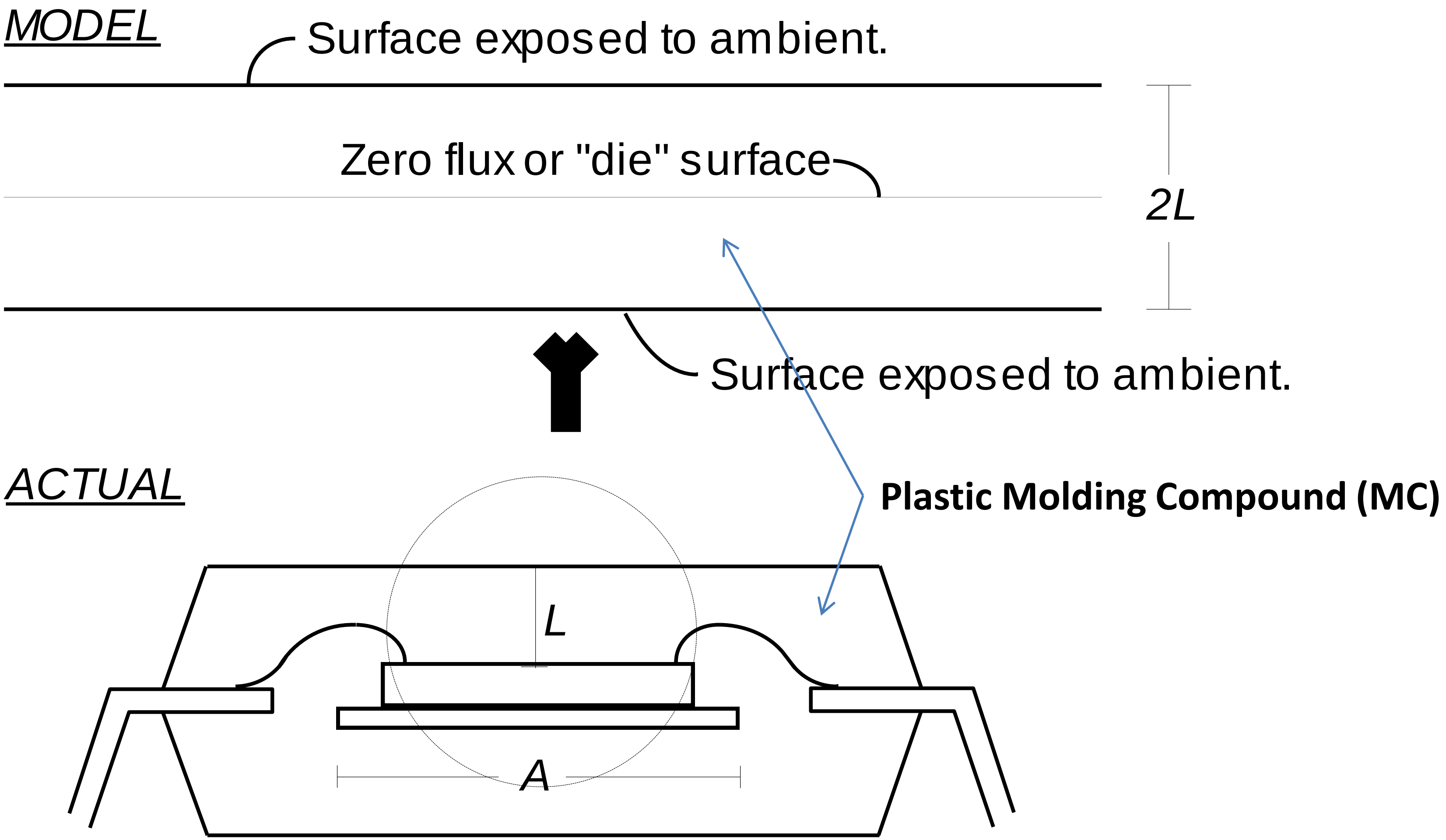
TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

H_2O Diffusion/Absorption in MC



H_2O Diffusion/Absorption in MC

Diffusion Coefficient:

$$D = D_0 \exp\left(-\frac{Q_d}{kT}\right)$$

See slide 13.

Saturation Coefficient:

$$S = S_0 \exp\left(\frac{Q_s}{kT}\right)$$

$$D_0 = 4.7 \times 10^{-5}\ \mathrm{m}^2/\mathrm{sec} \quad Q_d = 0.50\ \mathrm{eV}$$

$$S_0 = 2.76 \times 10^{4}\ \mathrm{mole/m^3Pa} \quad Q_s = 0.40\ \mathrm{eV}$$

Source: Kitano, et al IRPS 1988

Henry's Law:

$$M_{\mathrm{sat}} = PS = \underbrace{HP_{\mathrm{sat}}}S$$

H_2O vapor pressure.

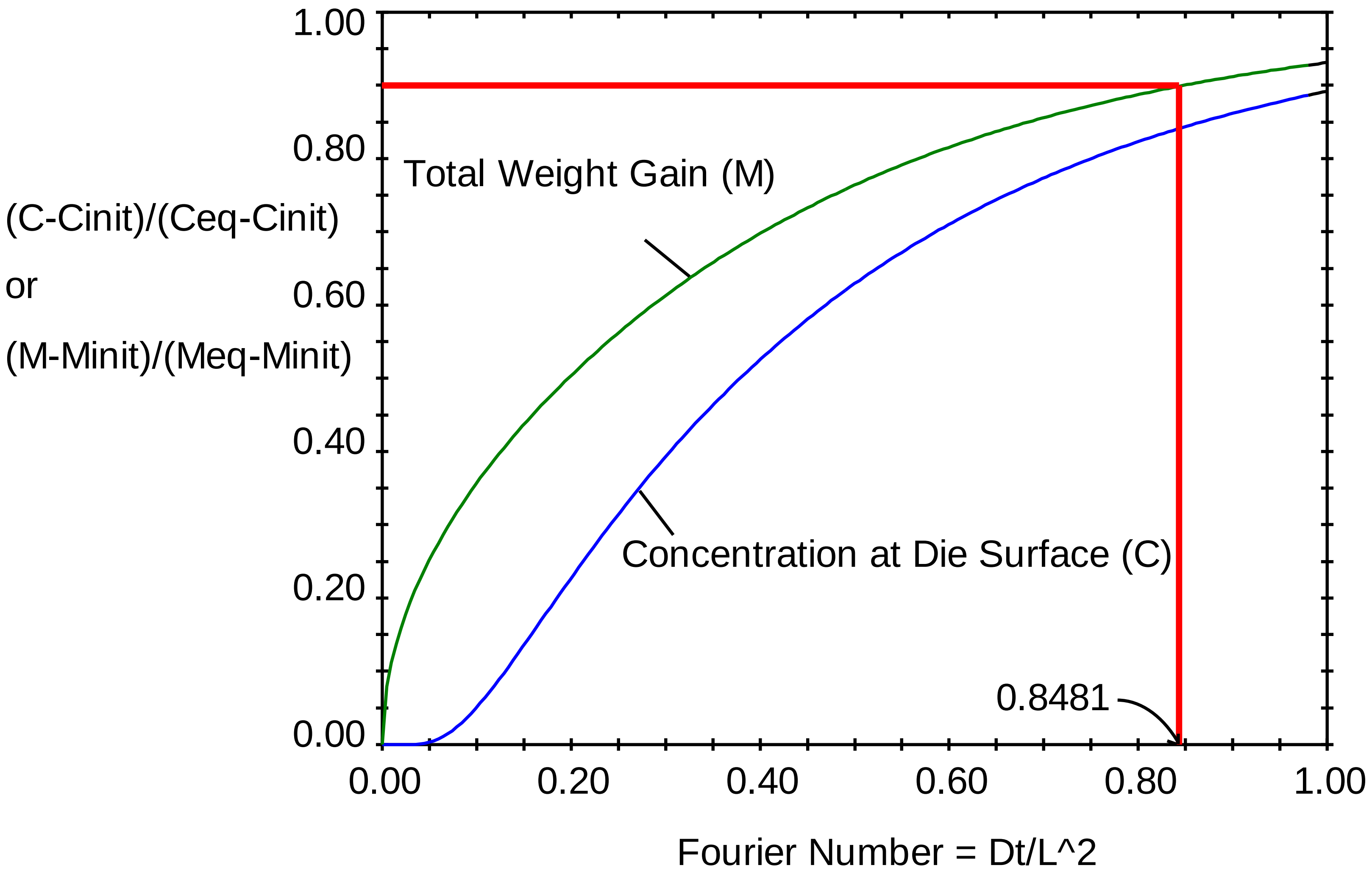
See slide 33.

Key Observation: Saturated moisture content of molding compound is nearly independent of temperature, and is proportional to RH.

$$M_{sat} = HP_0 S_0 \exp\left[\frac{(Q_s - Q_p)}{kT}\right] \qquad Q_s - Q_p = -0.02\ \mathrm{eV}$$

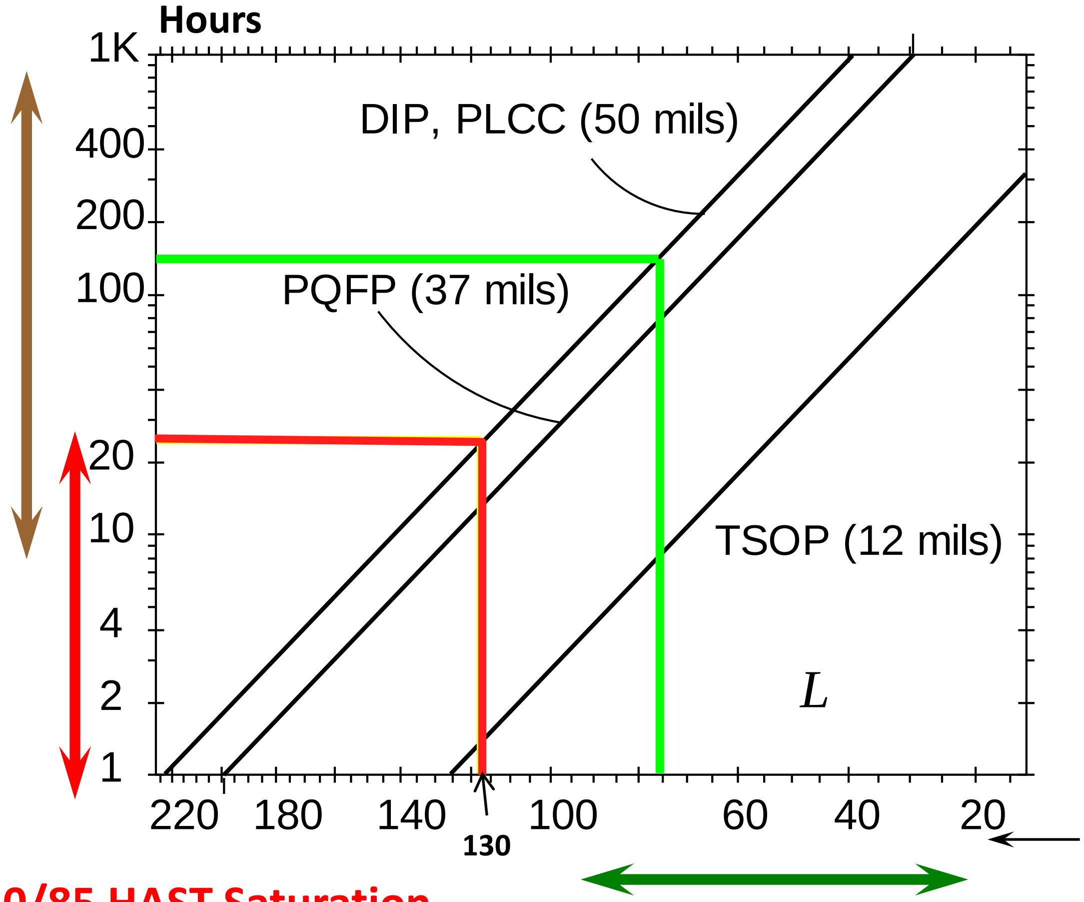
Nearly zero!

H_2O Diffusion/Absorption in MC



Response to Step-Function Stress

Typical Use Saturation Times



Typical 130/85 HAST Saturation Times

Normal Operating Range

Package Moisture Time Constant

(time to 90% saturation)

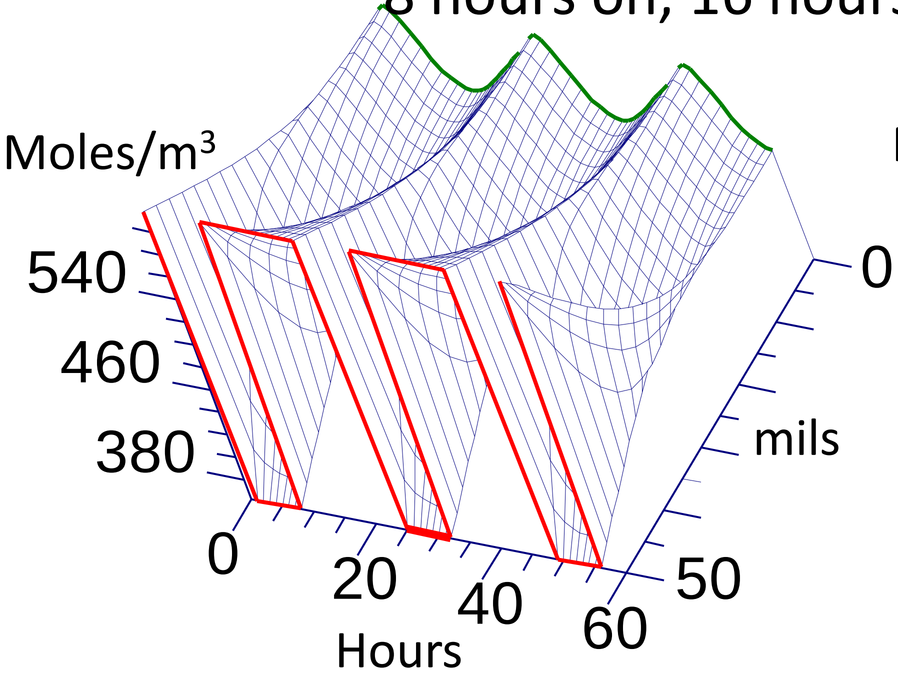
$$t(\mathrm{sat}) =$$

$$0.8481\frac{L^2}{D_0}\exp\left(\frac{Q_d}{kT_{mc}}\right)$$

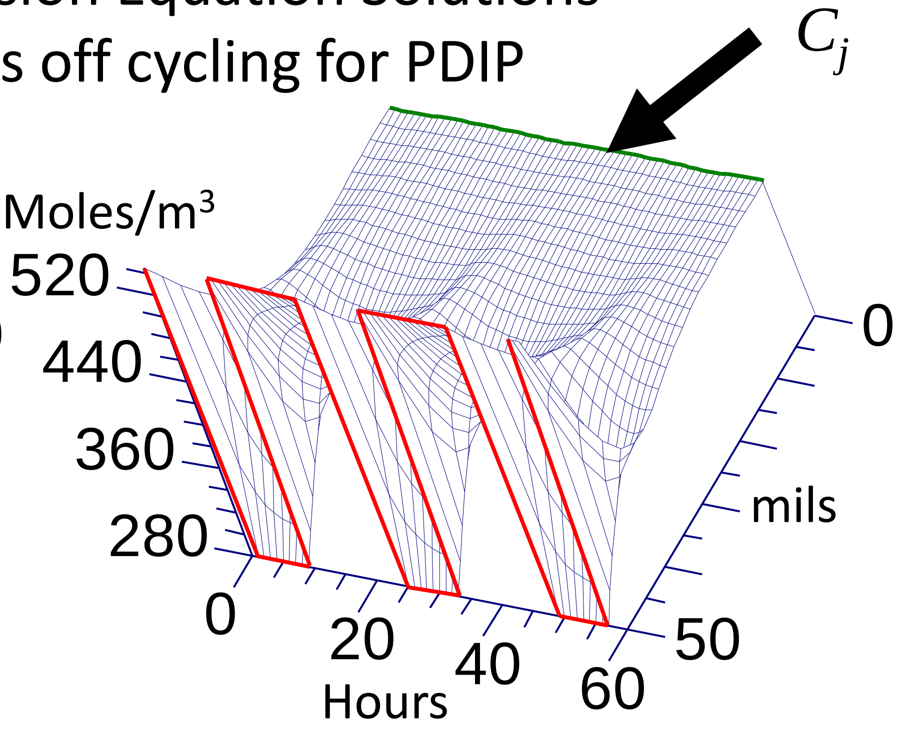
Cyclical Stress

One-Dimensional Diffusion Equation Solutions

8 hours on, 16 hours off cycling for PDIP



T(ambient) = 100 C
t(sat) = 28 hours



T(ambient) = 60 C
t(sat) = 153 hours

Moisture concentration at the die is constant if Period << t(sat)

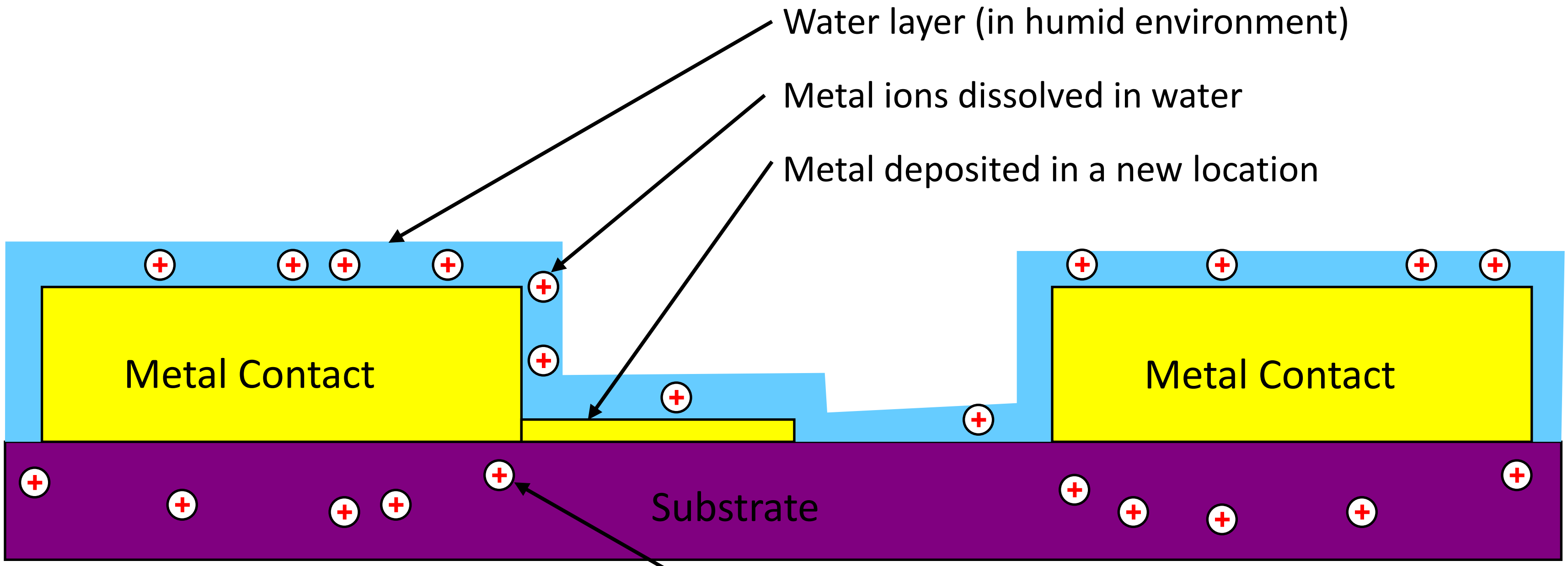
Peck’s Acceleration Model

- Fundamental environmental parameters are *T*, *H* and *V*, *at the site* of the failure mechanism.
  - If the die is the site, this is denoted by “*j*”.
- A frequently used acceleration model is due to Peck

$$AF = (a + b \times V) \times H_j^m \times \exp(-Q / kT_j)$$

- Find *a*, *b*, *m*, *Q* from experiments with steady-state stress and negligible power dissipation.
- Typically *a* is small or zero: Bias is required.
- Requires *H* > 0 for acceleration: Moisture is required.

Moisture and Temperature Fails



Water layer (in humid environment)

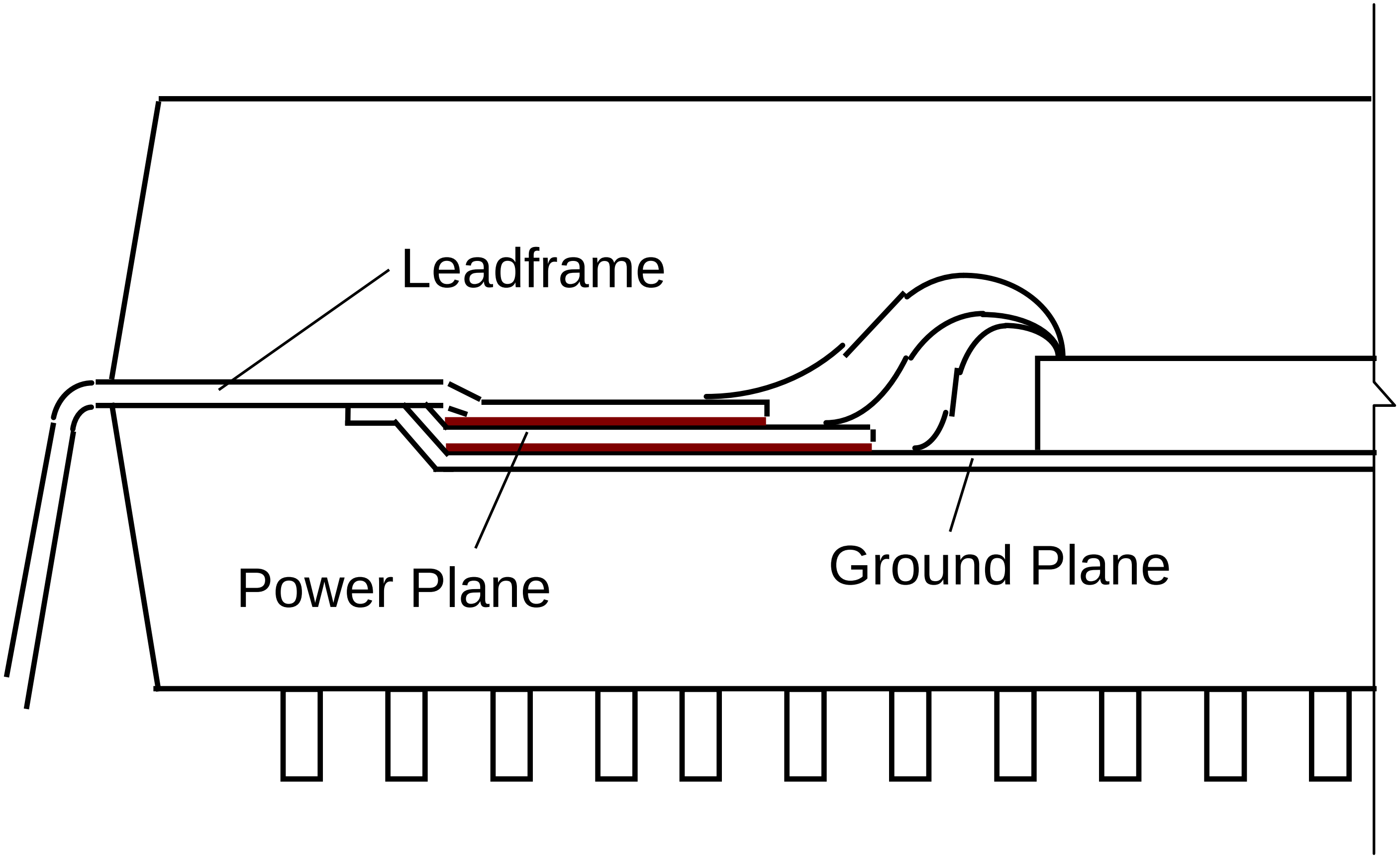
Metal ions dissolved in water

Metal deposited in a new location

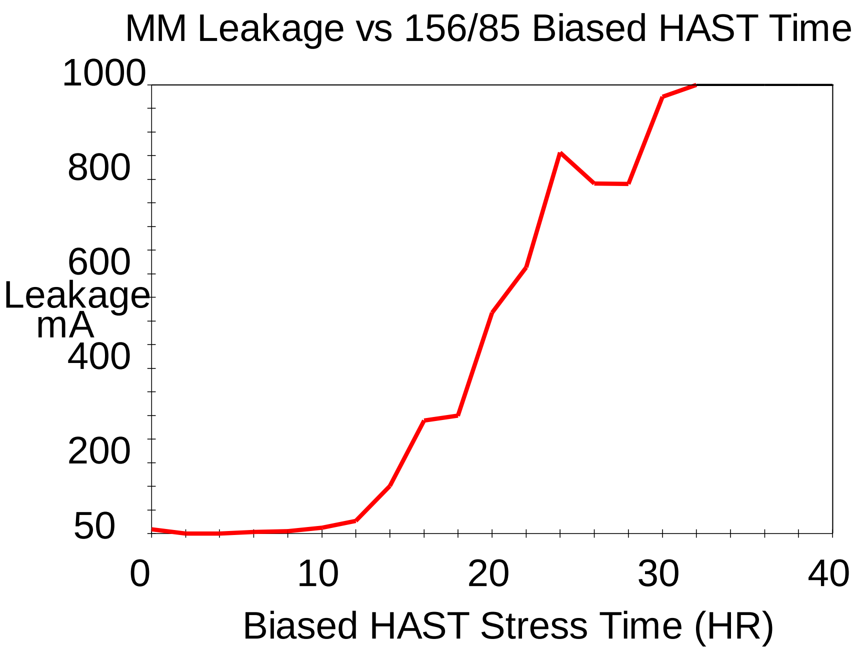
Water and metal also diffuse through the substrate

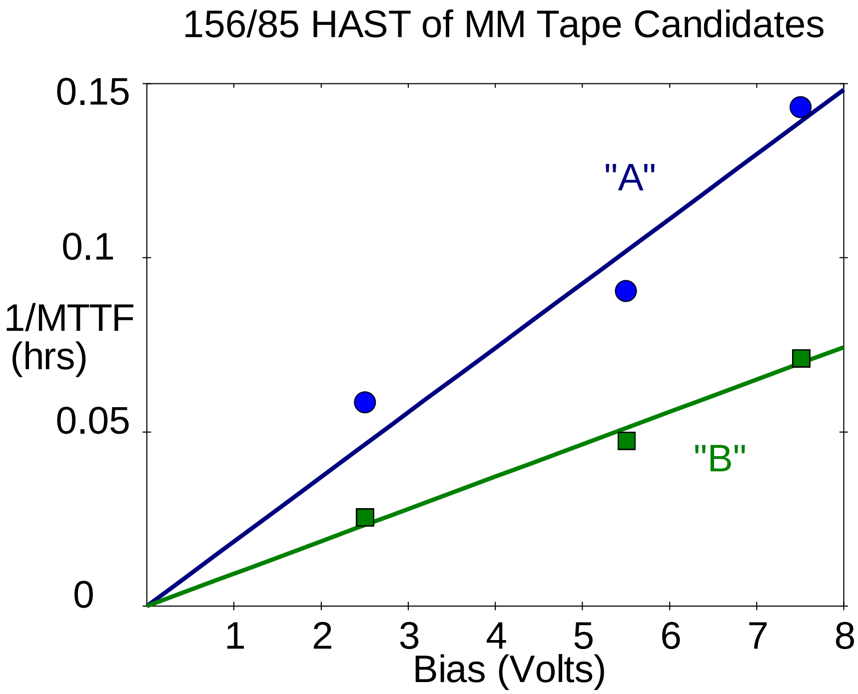
- Humidity gives a layer of water on most surfaces
  - Water also diffuses into the substrate
- Water + voltage → metal ions in water
- Metal can deposit in other locations or *migrate*

Moisture: MM Tape Leakage



Moisture: MM Tape Leakage





Experimental Tape Data:

Tape	m	Q eV
“A”	>12	0.74
“B”	5	0.77

Source: C. Hong, Intel, 1991

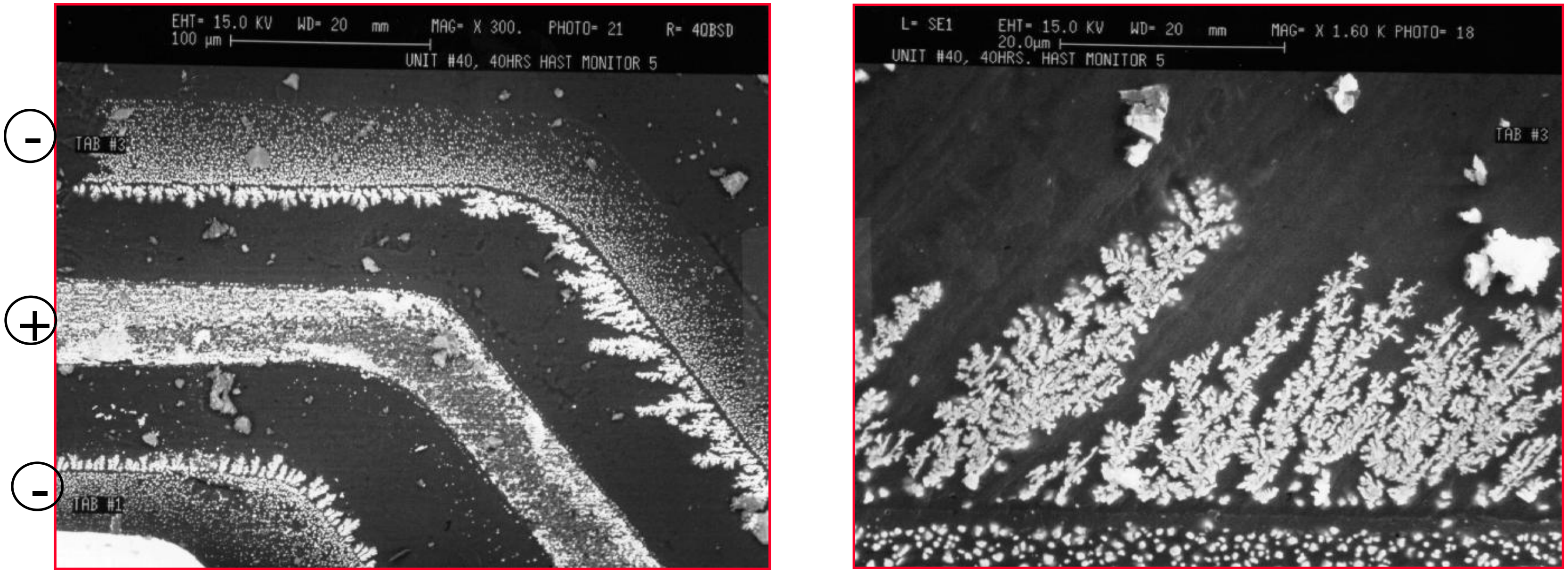
Acceleration factor is proportional to bias.

$$AF =$$

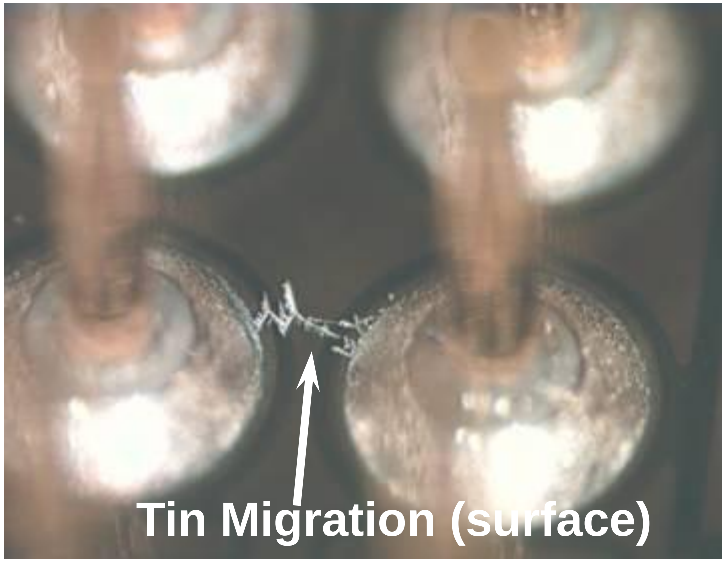
$$\text{Constant} \times V \times H^m \exp(-Q / kT)$$

Moisture: Internal Metal Migration

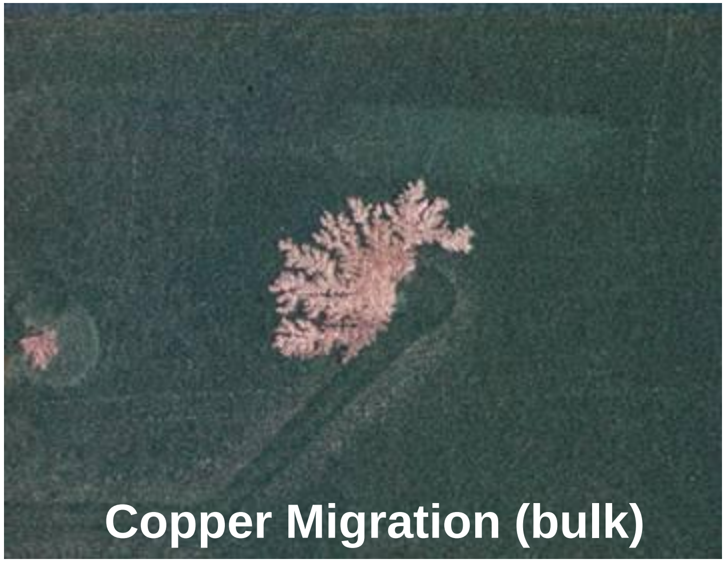
- TAB Inter-lead Leakage/Shorts
  - Accelerated by voltage, temperature and humidity
  - Seen as early as 20 hrs 156/85 HAST
  - Highly dependent on materials & process



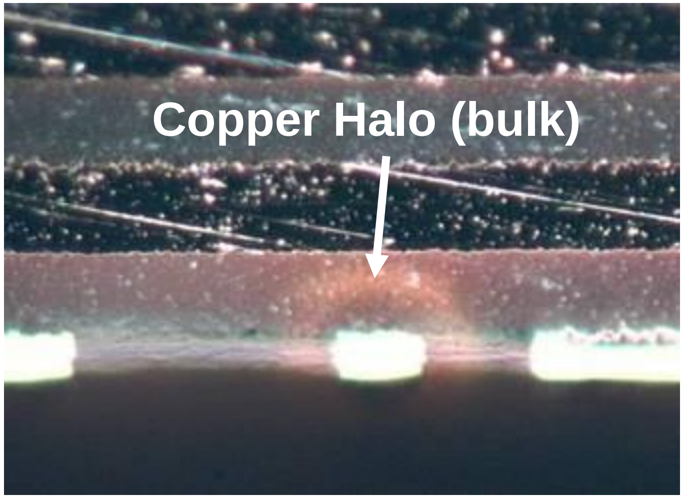
Copper dendrites after 40 hours of biased 156/85 HAST



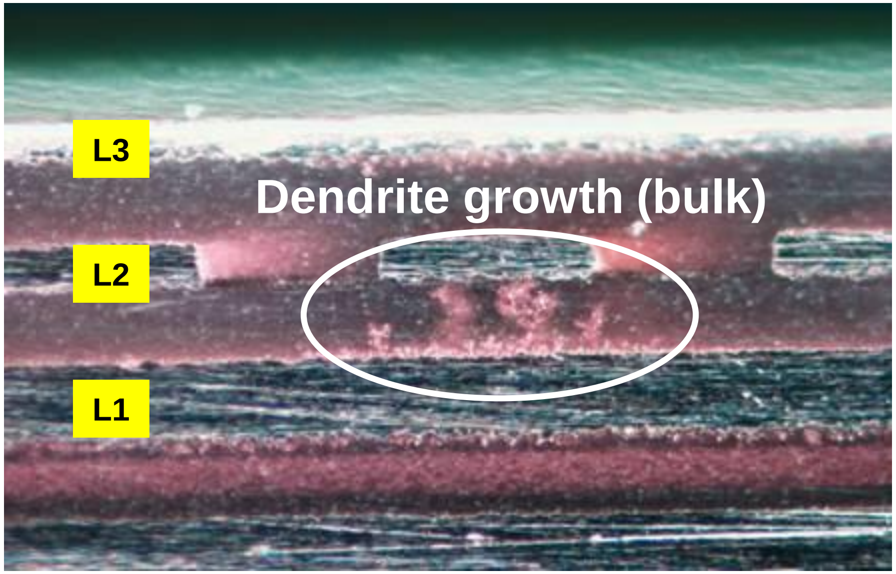
Tin Migration (surface)



Copper Migration (bulk)



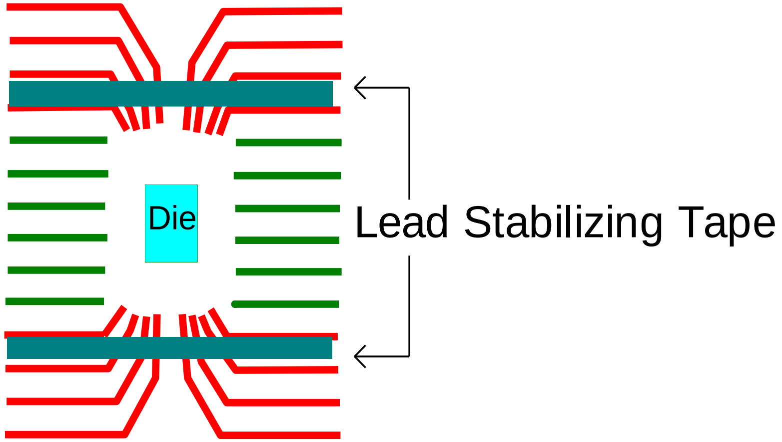
Copper Halo (bulk)



Dendrite growth (bulk)

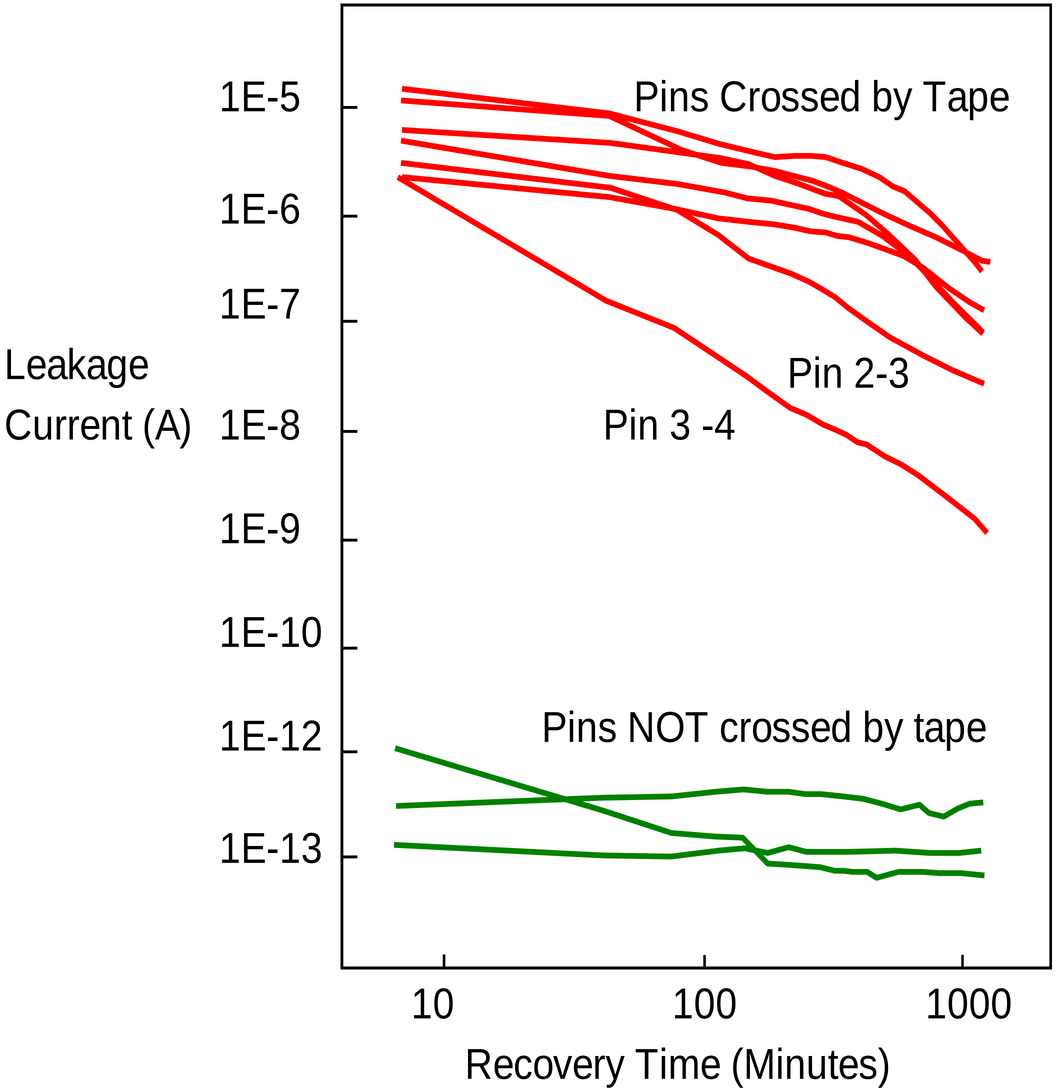
Lead-Stabilizing Tape Leakage

- A vendor process excursion.
- Leakage observed after 336 hours of steam.
- Re-activated by 48 hours at 70C/100% RH
- No leakage seen between leads not crossed by tape
- Rapid decay for leads crossing end of tape
  - Tape dries from exterior inwards



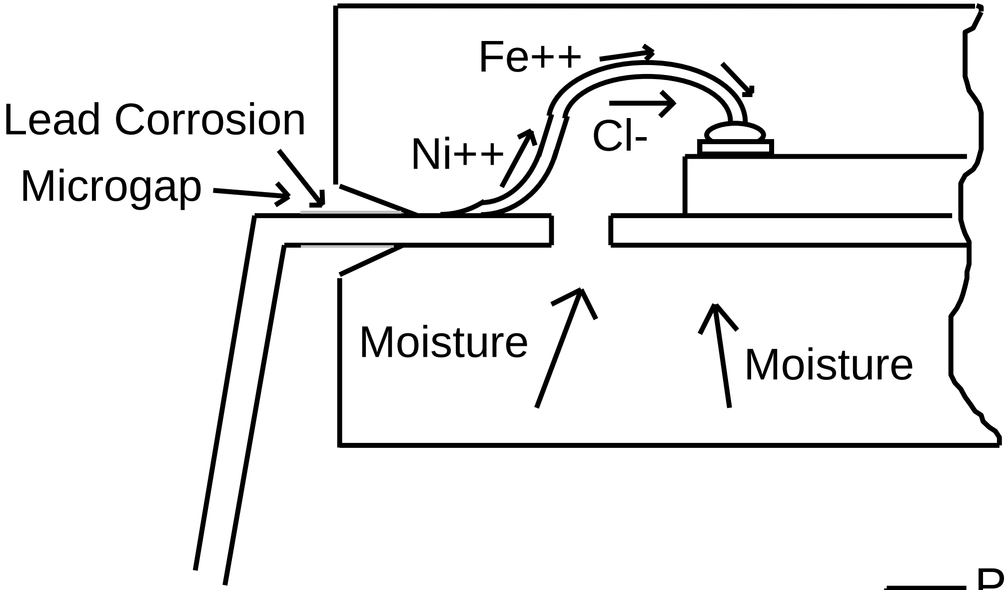
Tape provides mechanical stability to long leads during wirebond.

Lead-Stabilizing Tape Leakage



Source: S. Maston, Intel

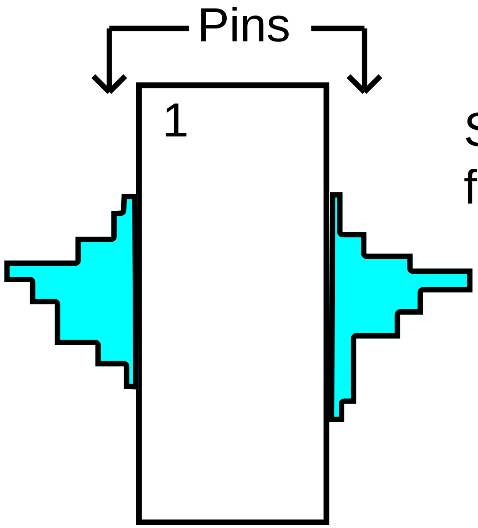
Aluminum Bond Pad Corrosion



$$AF =$$
$$\text{Constant} \times V \times H^{m} \exp(-Q/kT)$$

Source	m	Q (eV)
Peck (a)	2.66	0.79
Hallberg&Peck (b)	3.0	0.9

(a) IRPS, 1986; (b) IRPS, 1991.



Shortest path has highest failure rate.

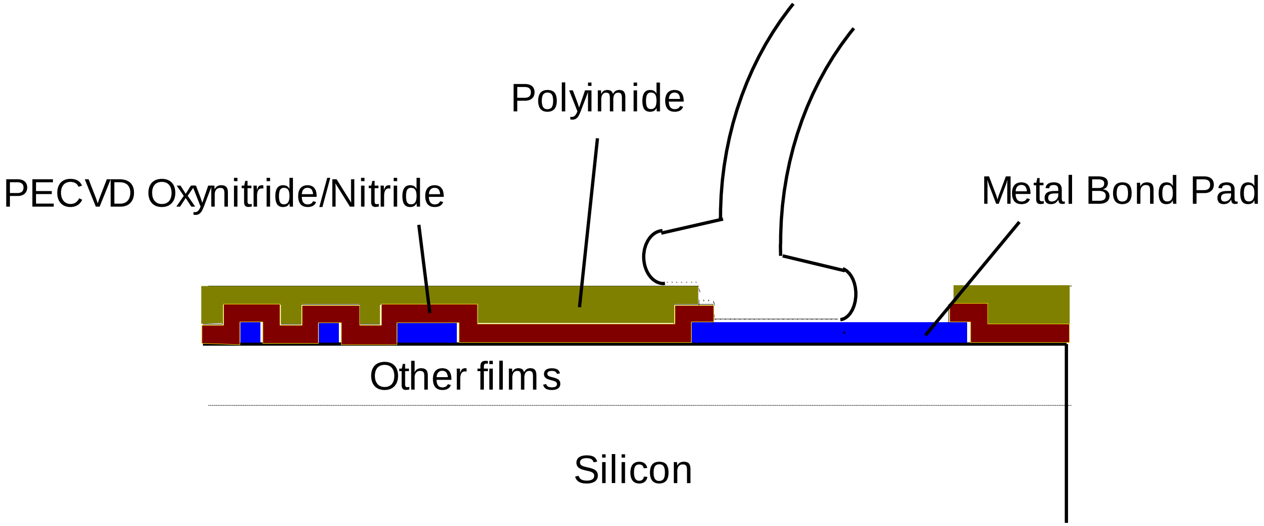
Source: P.R. Engel, T. Corbett, and W. Baerg, “A New Failure Mechanism of Bond Pad Corrosion in Plastic-Encapsulated IC’s Under Temperature, Humidity and Bias Stress” Proc. 33rd Electronic Components Conference, 1983.

Passivation in Plastic Packages

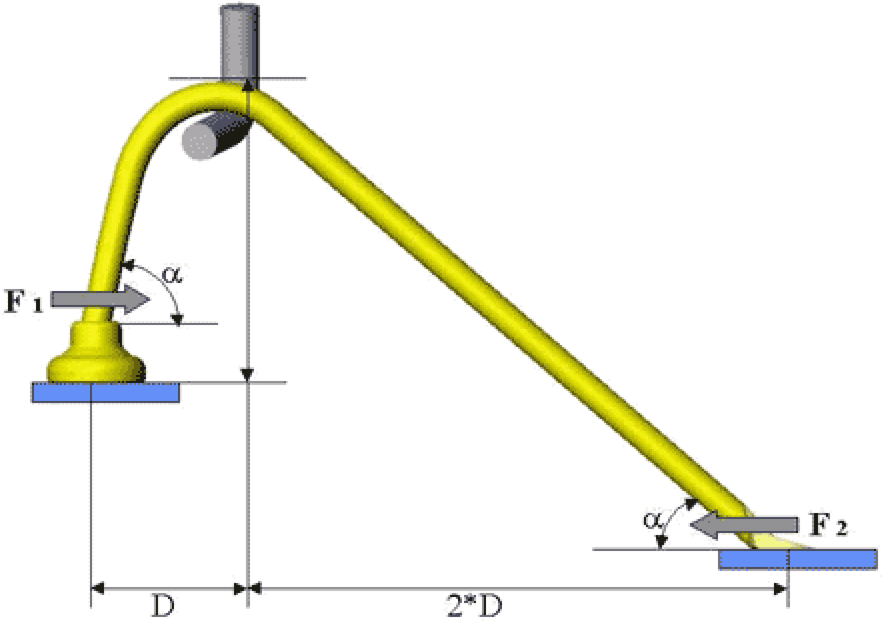
- Passivation is the final layer on the die.
- Passivation has two main functions:
  - Moisture Barrier
    - Molding compound is not a moisture barrier.
    - Silicon oxides are not good moisture barriers.
    - PECVD silicon nitride or silicon oxynitride film is a good barrier.
    - Film must be thick enough to avoid pinholes, coverage defects.
  - Mechanical Protection
    - Silicon nitride films are brittle.
    - Polyimide compliant film protects silicon nitride.
    - Polyimide can react with moisture (depending on formulation).

Polyimide/Au Bond Failure

- Bonds overlapping passivation don't necessarily violate design rules.
- But can activate polyimide-related "purple plague" failure mechanisms in combination with moisture.
- Acceleration modeling showed no field jeopardy.

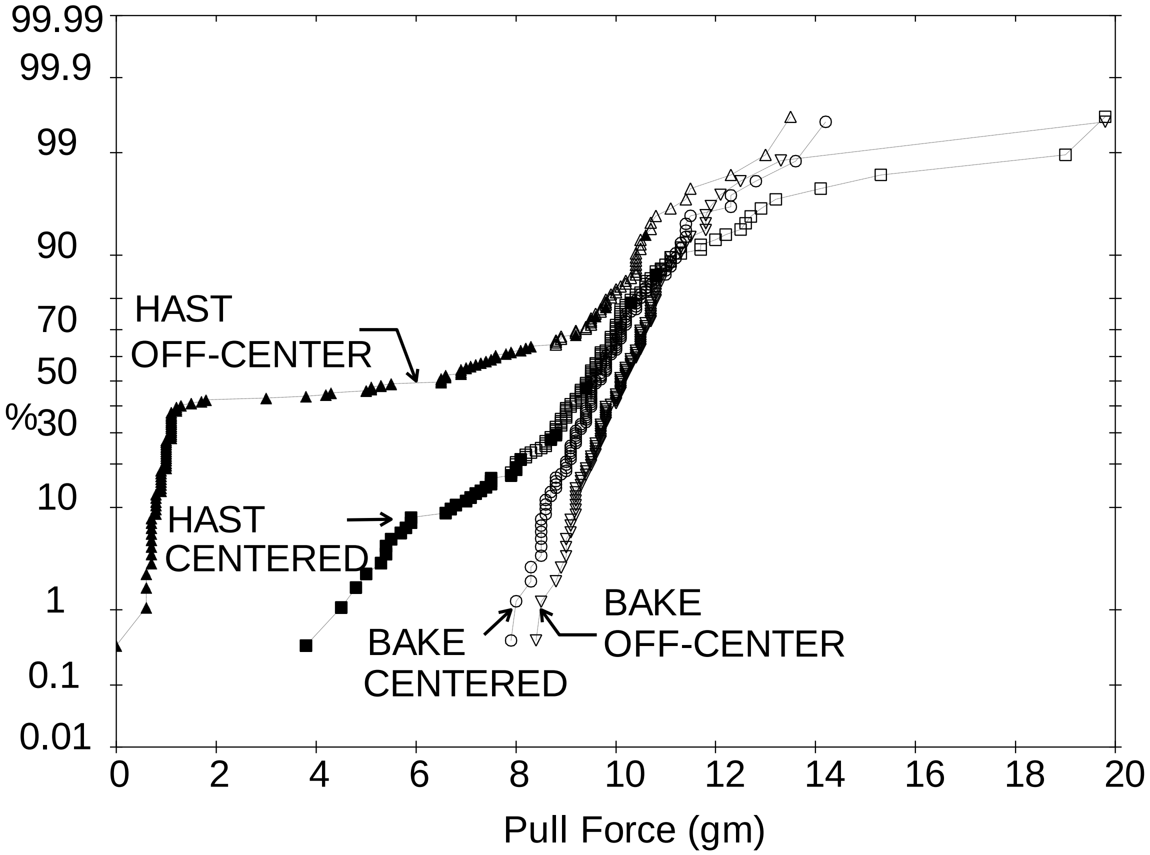


Wire Bond Pull Test



Moisture-Related Gold Bond Degrad’n

Effect of 80 hours of 156/85 HAST vs 156/0 Bake and Centered vs Off-Centered Bonds on Wire Pull Test Data

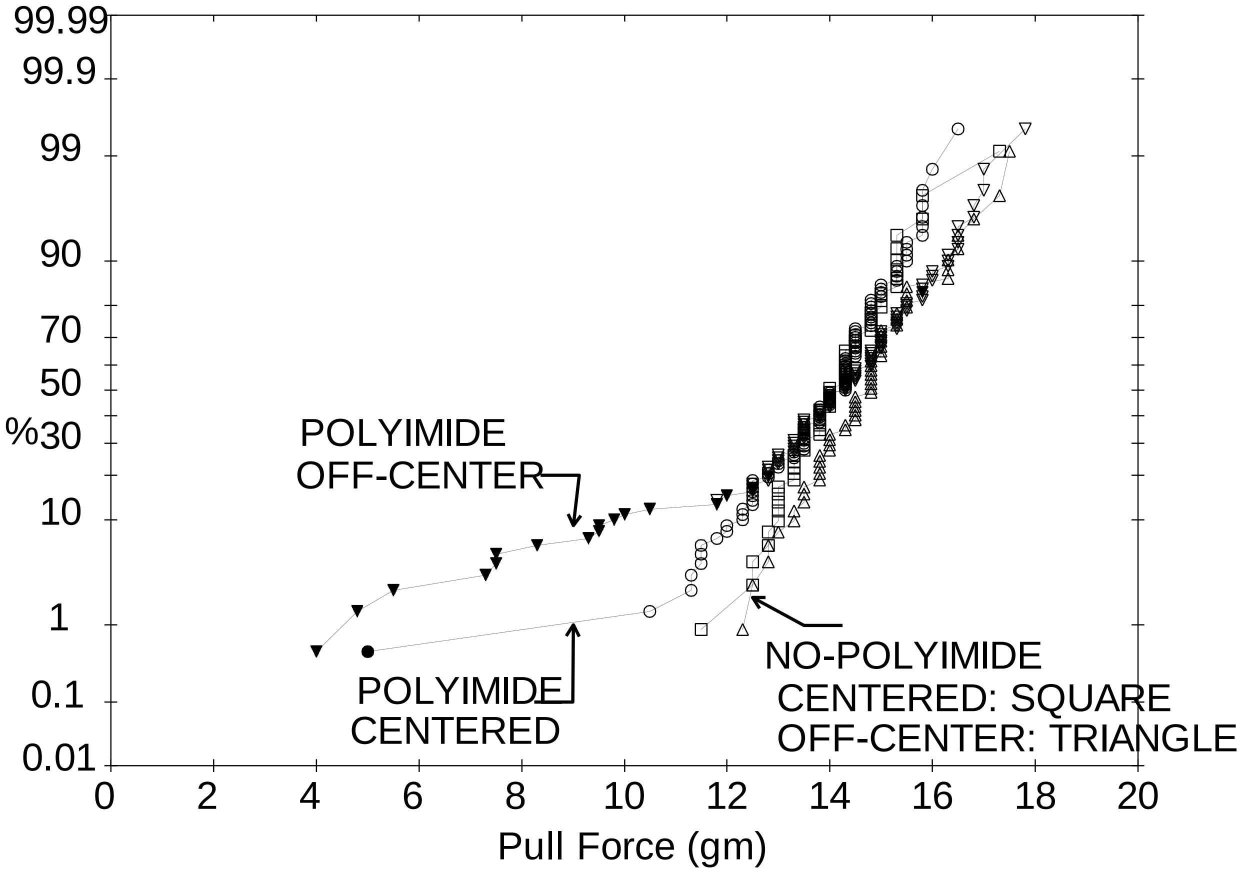


(all *with* polyimide)

Source: G. Shirley and M. Shell, IRPS, 1993

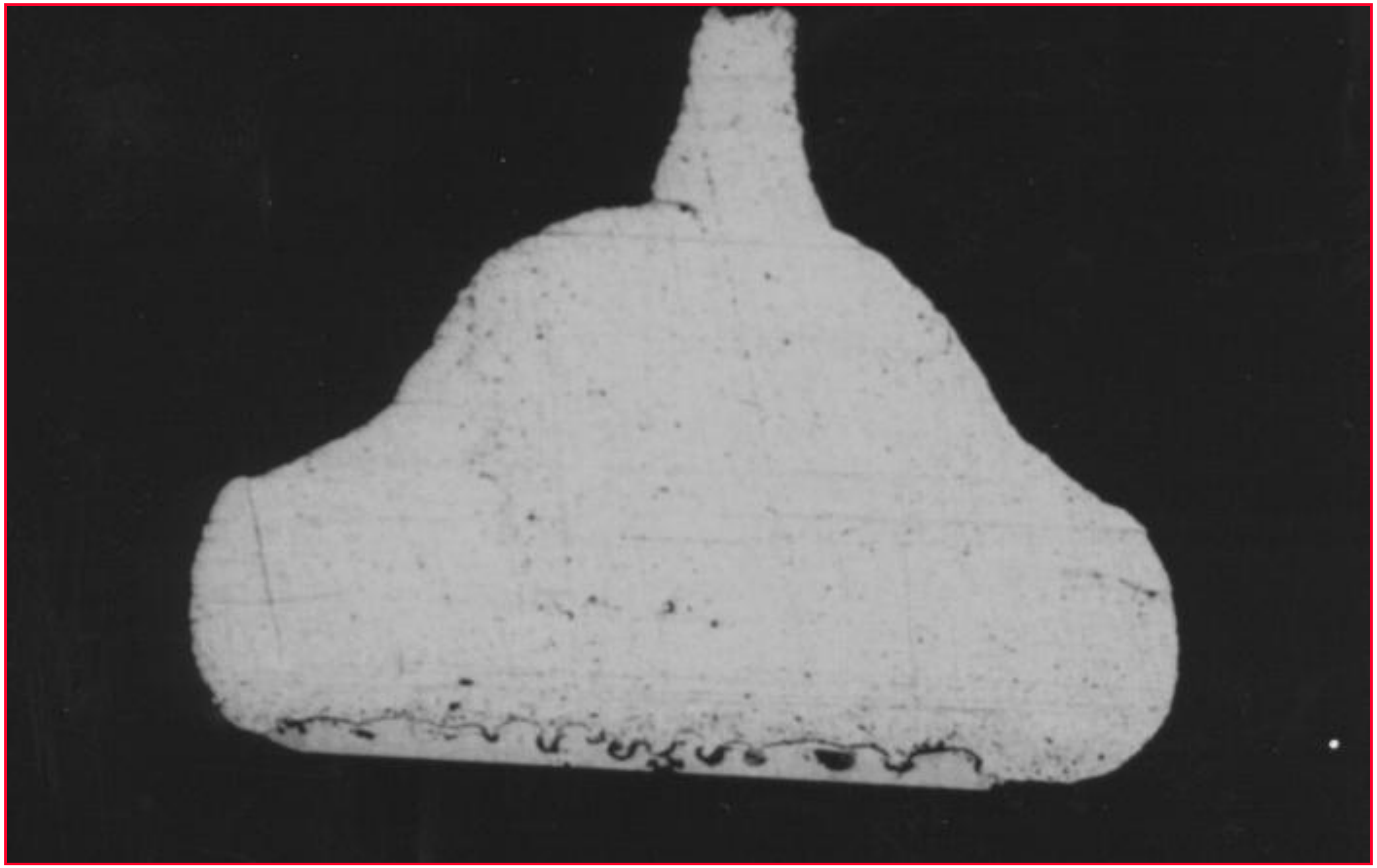
Moisture-Related Gold Bond Degrad'n

Wire Pull Strength of Polyimide vs No Polyimide and Centered vs Off-Centered Bonds after 40 hours of 156/85 HAST



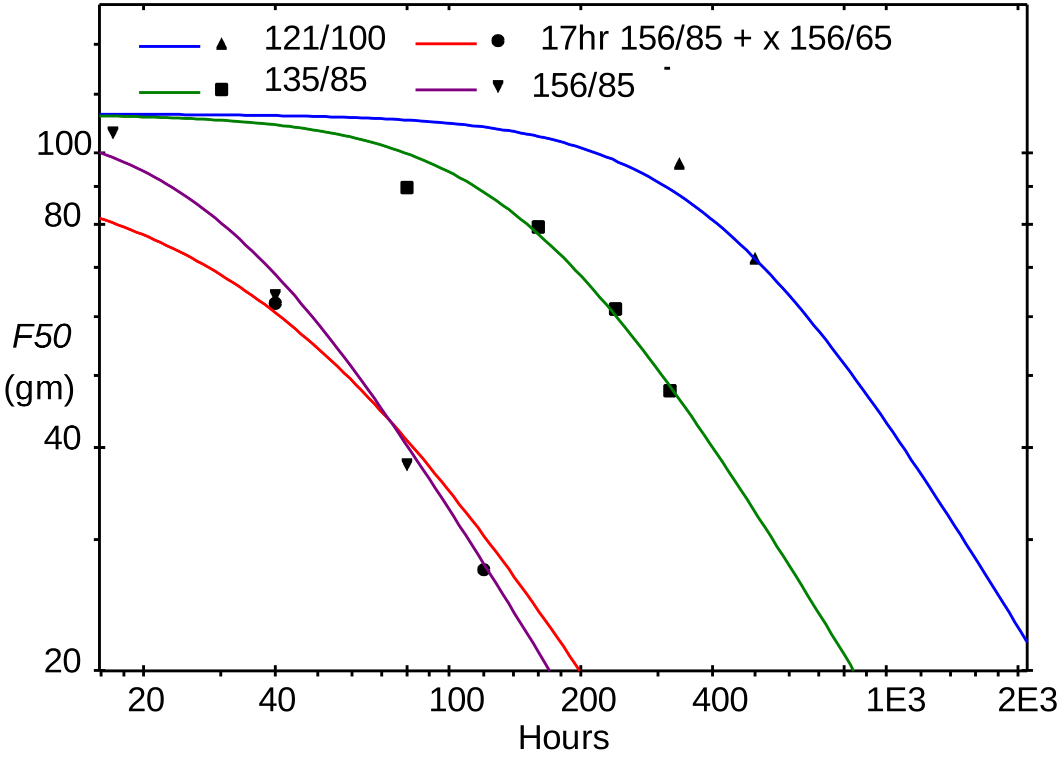
Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993

Moisture-Related Purple Plague



Cross-section of gold ball bond on aluminum pad
after 80 hours at 156C/85%RH

Moisture-Related Gold Bond Degrad'n



$$b = 112.7 \ \text{gm}$$

$$a_0 = 1.13 \times 10^{10} \ (\text{gm-hrs})^{-1}$$

$$m = 0.98; \quad Q = 1.15 \ \text{eV}$$

$$F_{50} = \frac{1}{\sqrt{(at)^2 + 1/b^2}}$$

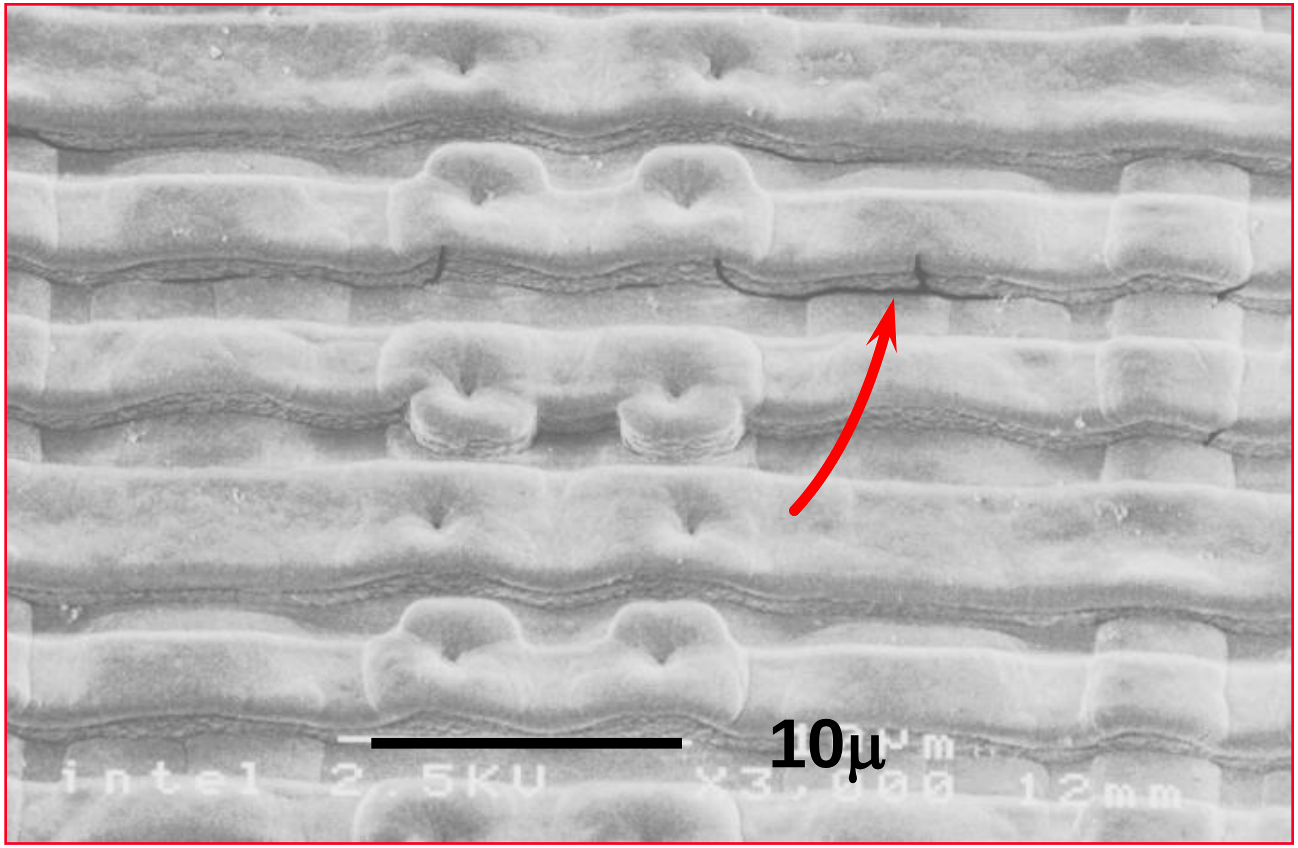
$$a = a_0 \times h^m \times \exp(-Q/kT)$$

$$F_P = F_{50} \times \exp(-\sigma \times Z_P)$$

$$\sigma = 0.17$$

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993

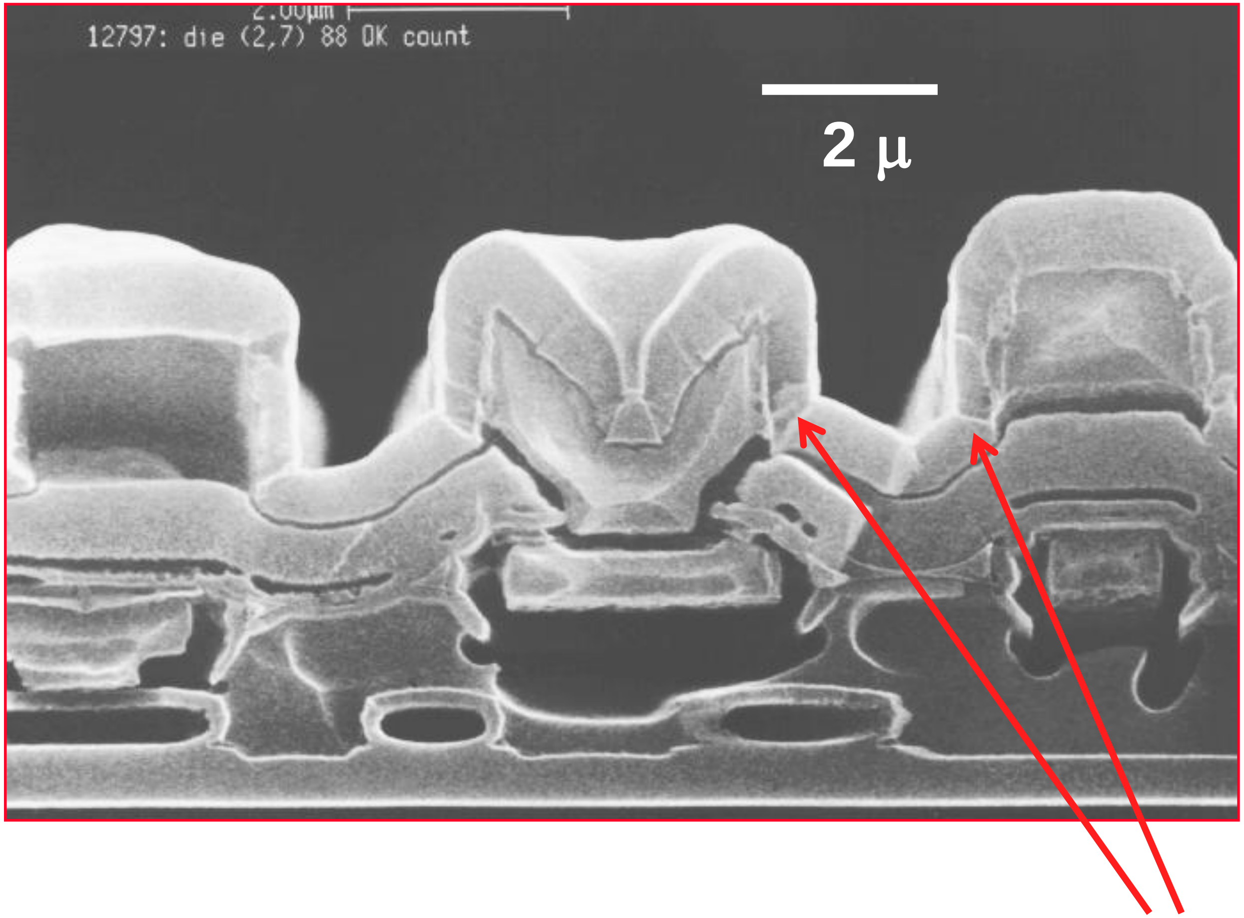
Circuit Failure Due to Passiv’n Defects



Site of failing bit. SRAM after HAST stress.

Courtesy M. Shew, Intel

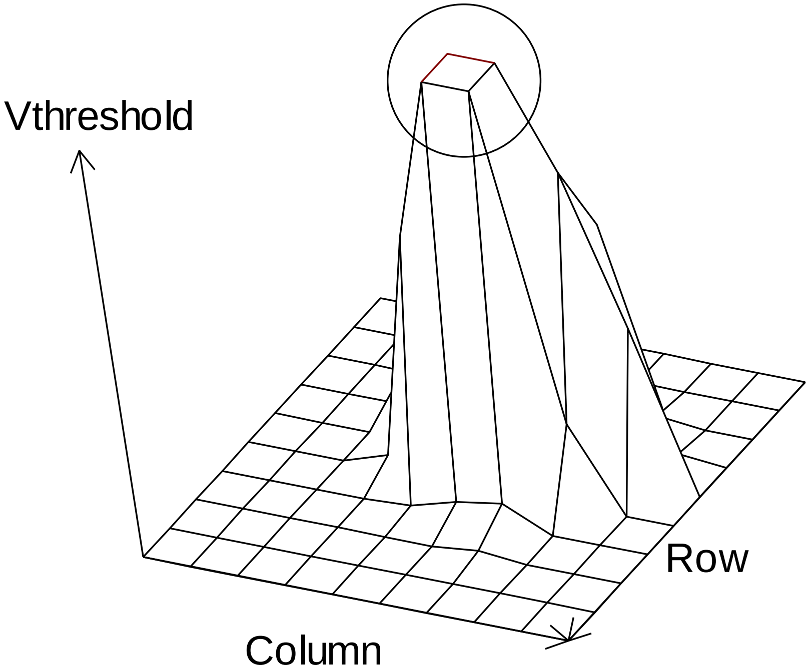
Circuit Failure Due to Passiv'n Defects



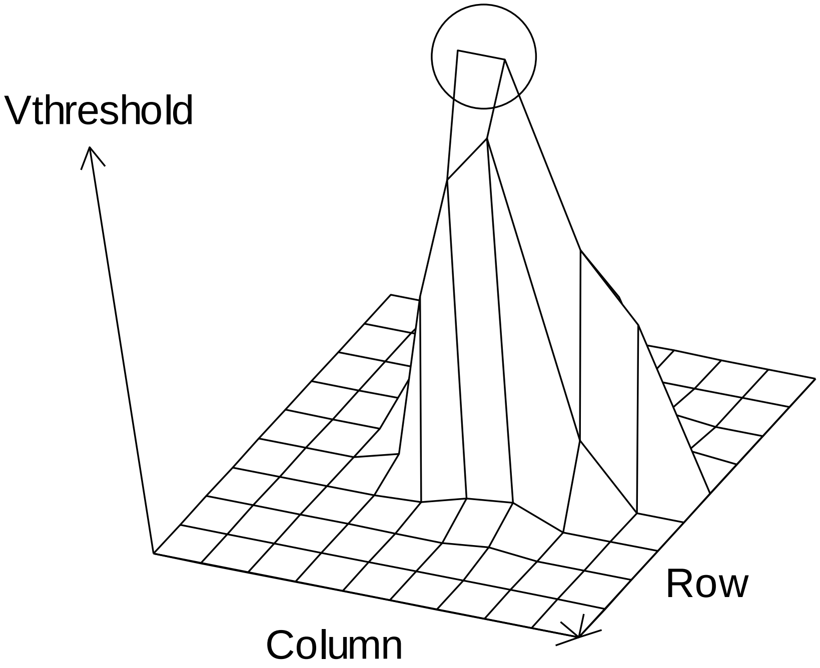
Etch-decorated cross-section of passivation. Note growth seams.

Circuit Failure Due to Passiv’n Defects

SRAM VOLTAGE THRESHOLD MAP FOR CELL PULLUP TRANSISTOR
(Baseline threshold is 0.89 V. Passivation is 0.6 μ nitride, no polyimide.)



After 120 h 156/85. 4 failed bits with Vt > 2.5 V

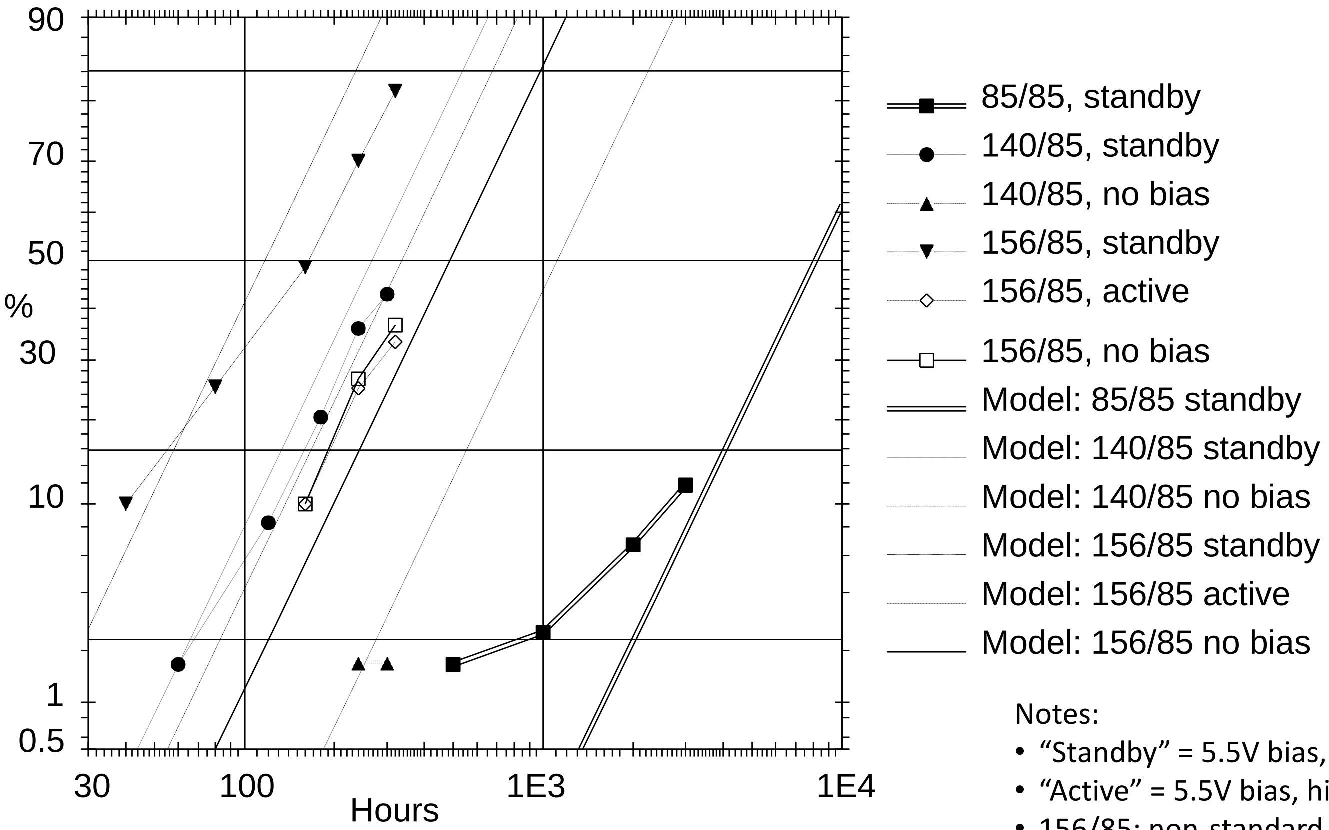


2 bits recover after further 2 hr bake at 150 C

Source: C. Hong, Intel

Acceleration Model Fit of HAST Data

SRAM HAST and 85/85 Bit Failures (No Polyimide)



$$AF = \text{Constant} \times (a + bV) \times H^m \times \exp(-Q/kT)$$

$$a = 0.24 \quad b = 0.14 \quad m = 4.64 \quad Q = 0.79 \ \text{eV}$$

Notes:

- "Standby" = 5.5V bias, low power
- "Active" = 5.5V bias, high power
- 156/85: non-standard, limit of pressure vessel.
- Source: C. G. Shirley, C. Hong. Intel

Peck Model Parameters

Mechanism	**Q(eV)**	**m**	**Q/m**	**Q/m < 0.42eV?**	**Hours of 130/85 ≡ 1kh 85/85**	**Reference**
MM Tape A	0.74	12	0.06	Yes	69	2
MM Tape B	0.77	5	0.15	Yes	62	2
Single Bit SRAM	0.79	4.6	0.17	Yes	57	3
Corrosion, THB (early Peck)	0.79	2.66	0.30	Yes	57	4
Corrosion, THB (later Peck)	0.90	3	0.30	Yes	39	5
Bond Shear	1.15	0.98	1.17	No	16	6

Yes/No: Increasing power dissipation at die, slows/accelerates the moisture mechanism.

1. Kitano, A. Nishimura, S. Kawai, K. Nishi, "Analysis of Package Cracking During Reflow Soldering Process," Proc. 26th Ann. Int'l Reliability Physics Symposium, pp90-95 (1988)
2. S. J. Huber, J. T. McCullen, C. G. Shirley. ECTC Package Rel. Course, May 1993. Package tape leakage acceleration data courtesy C. Hong.
3. G. Shirley and C. Hong, "Optimal Acceleration of Cyclic THB Tests for Plastic-Packaged Devices," in Proc. 29th Ann. Int'l Reliability Physics Symposium, pp12-21 (1991)
4. S. Peck, "Comprehensive Model for Humidity Testing Correlation," in Proc. 24th Ann. Int'l Reliability Physics Symposium, pp44-50 (1986).
5. Hallberg and D. S. Peck, "Recent Humidity Accelerations, A Base for Testing Standards," Quality and Reliability Engineering International, Vol. 7 pp169-180 (1991)
6. G. Shirley and M. Shell-DeGuzman, "Moisture-Induced Gold Ball Bond Degradation of Polyimide-Passivated Devices in Plastic Packages," in 31st Ann. Int'l Reliability Physics Symposium, pp217-226 (1993).

Homework 11

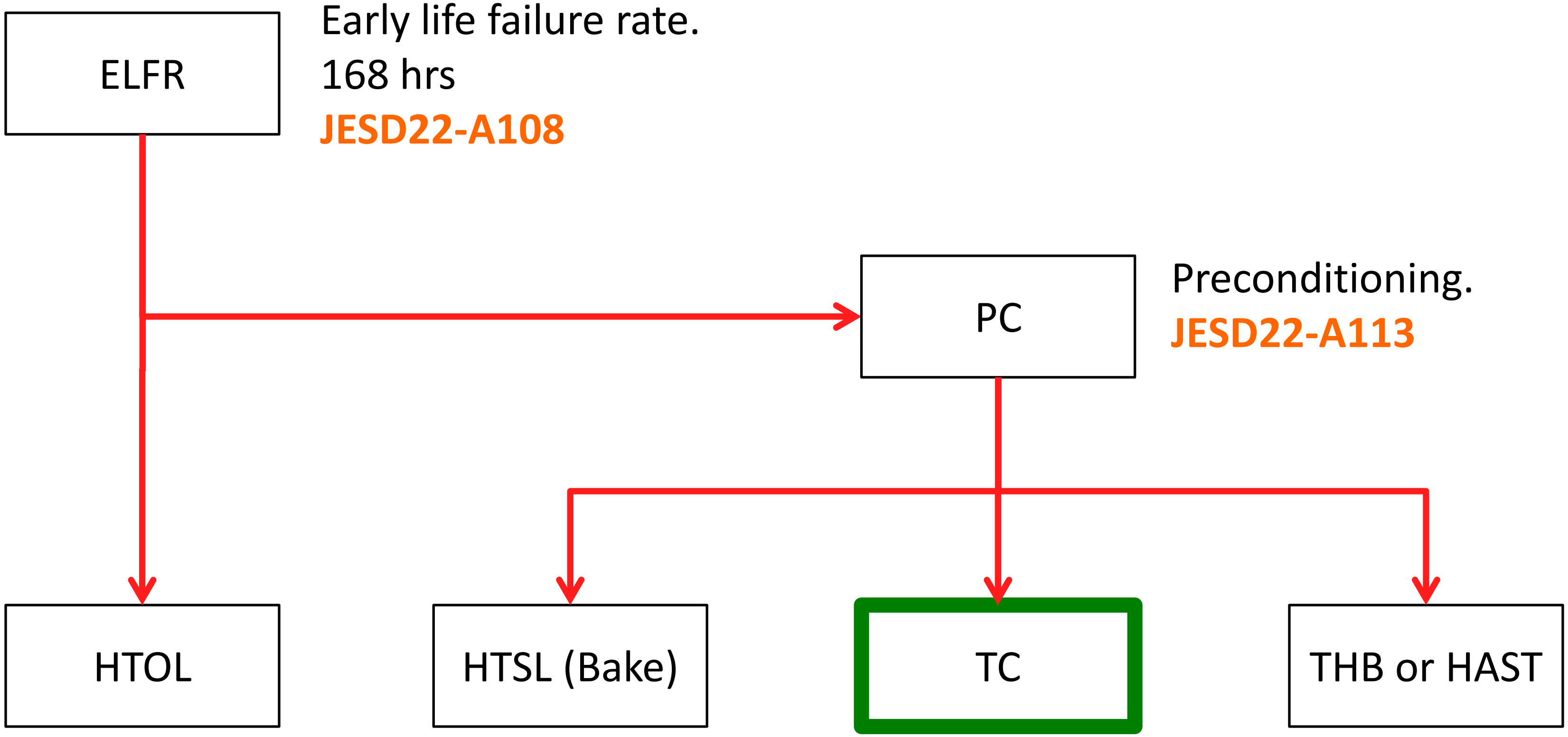
1. Show that, for the 6 moisture mechanisms on slide 40, 100 h of 130/85 stress is equivalent to 1000 h or more of 85/85 stress.
2. A product operates in an ambient of 25 °C and 85% RH. When in standby mode, the product dissipates negligible power. When in "active" mode the product dissipates sufficient power that the die temperature is 5 °C hotter than ambient. For each mechanism on slide 40, calculate the acceleration of the active mode relative to the standby mode.

Suggestion: Make a new sheet in the "Rel Calculator" tool. Useful functions (Psat and Arrhenius) are available there. AltF11 will allow you to see the code if you want to see documentation of the functions.

Outline

- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- ● Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- Technology Update

Thermomechanical Mechanisms



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

THB or HAST

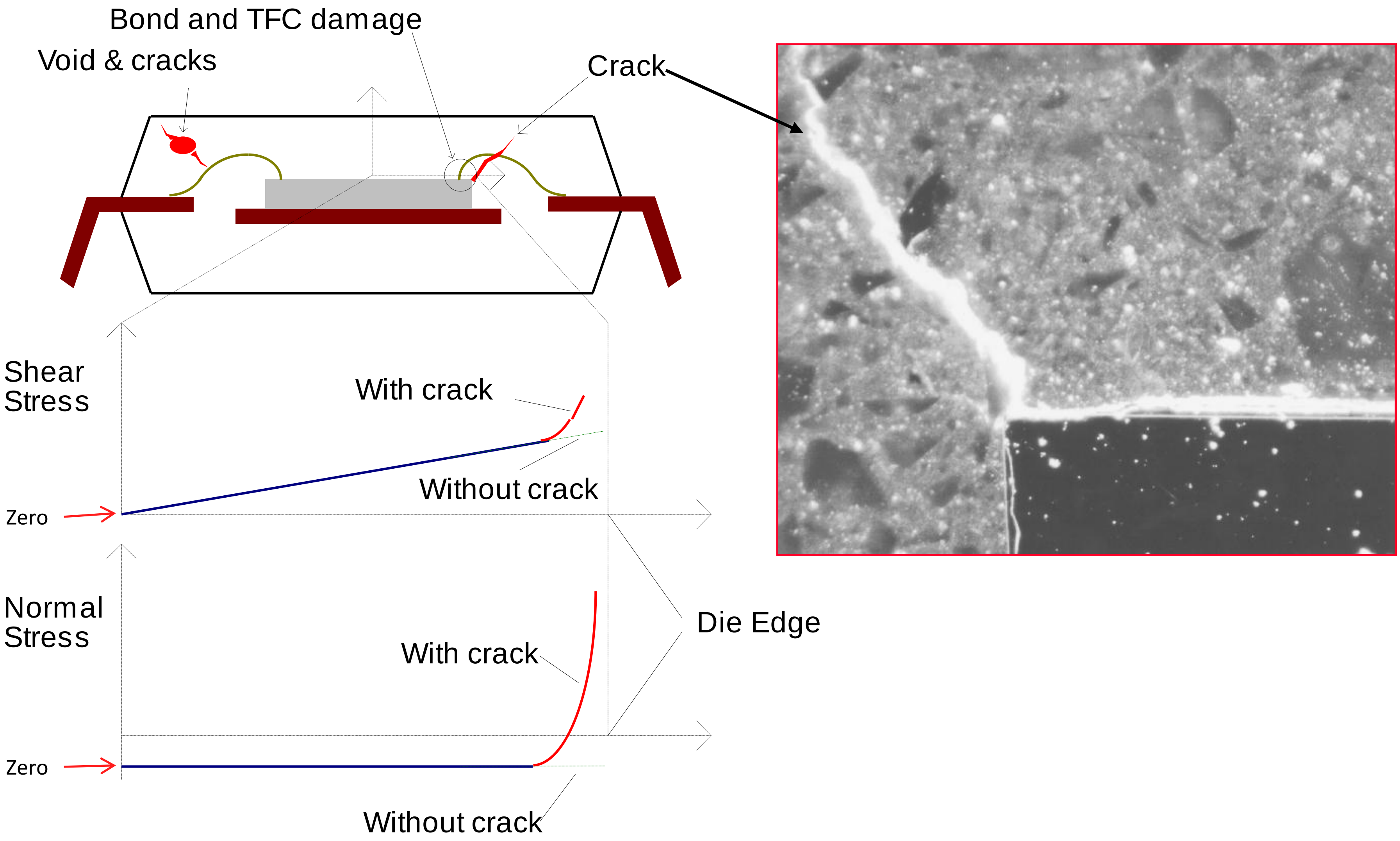
1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Key Material Properties

- Material properties which drive temperature cycling-induced failure mechanisms.

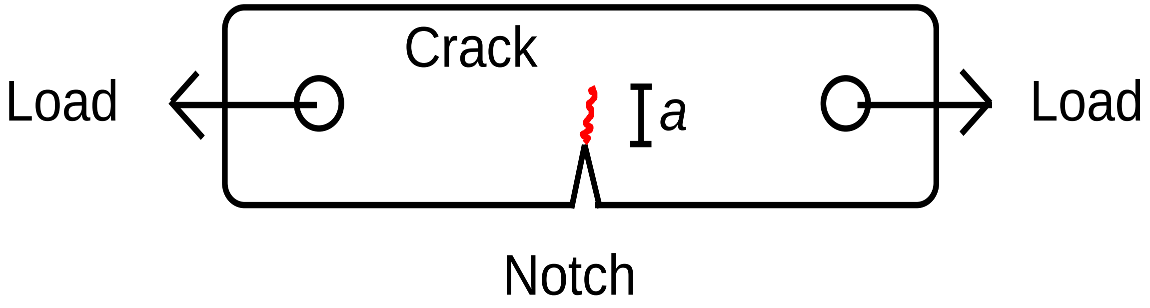
Material	Thermal Coeffic't of Expansion (ppm/°C) **"TCE"**	Young's Modulus (GPa)	Thermal Conductivity (W/m °C)
Copper	17	119	398
Alloy 42	5 Match!	145	15 Low!
Silicon	3	131	157
Molding Compound	21	18	0.6
Alumina	6.5	25	25
PC Board	15-17	11	25

Cracking Due to Temperature Cycle



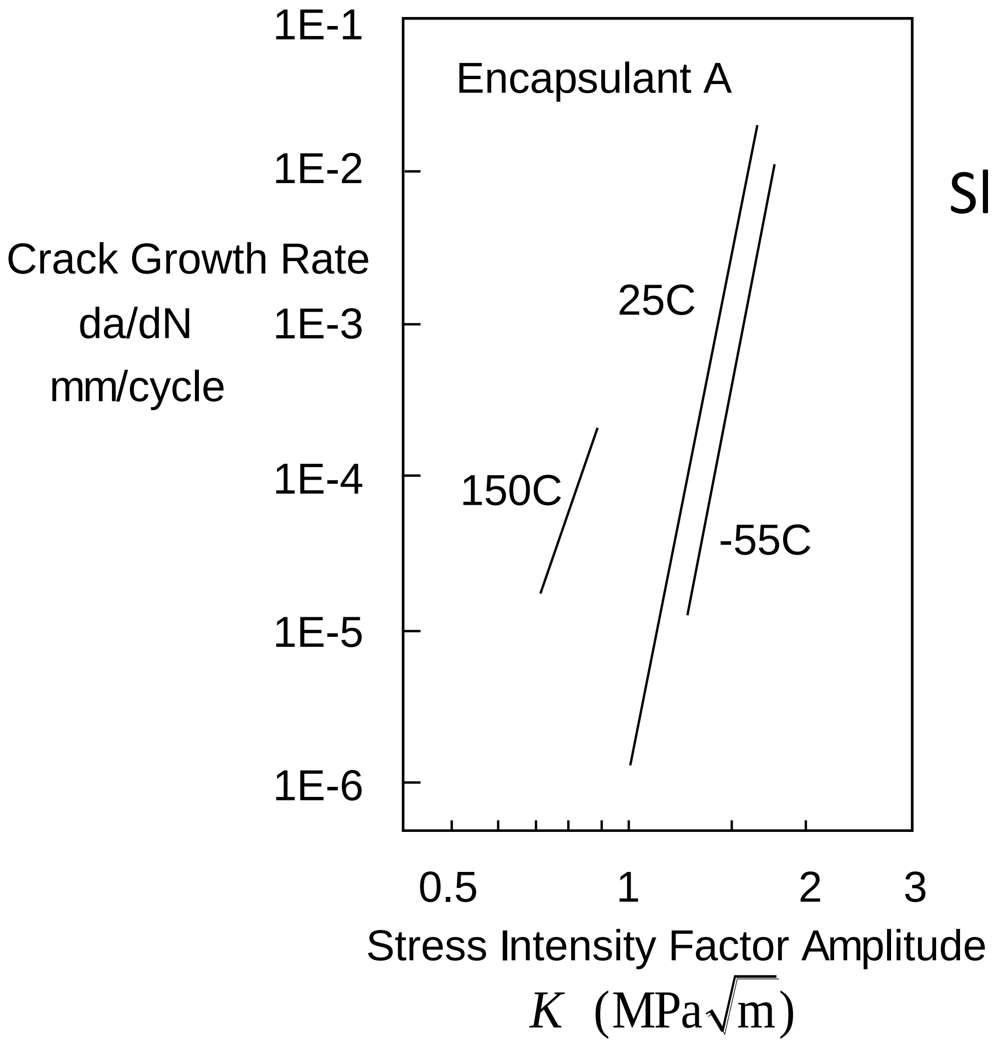
Crack Propagation in Test Conditions

- Tensile Test of Notched Samples
  - Measure crack growth rate for sinusoidal load:



  - Sample geometry and load determine stress intensity factor, *K*.
  - Plot crack growth rate da/dN versus *K* on log-log plot to determine Coffin-Manson exponent, *m*:

Crack Propagation in Test Conditions



Slope of lines on log-log plot

$$\frac{da}{dN} = Const \times (\Delta K)^m$$

$$m \approx 20$$

Source: A. Nishimura, et. al. "Life Estimation for IC Packages Under Temperature Cycling Based on Fracture Mechanics," IEEE Trans. CHMT, Vol. 10, p637 (1987).

Crack Propagation in Package

- The rate of crack propagation is also given by

$$\frac{da}{dN} = Const \times (\Delta K)^m$$

- But in plastic packages under temperature cycling, the stress concentration factor is

Important

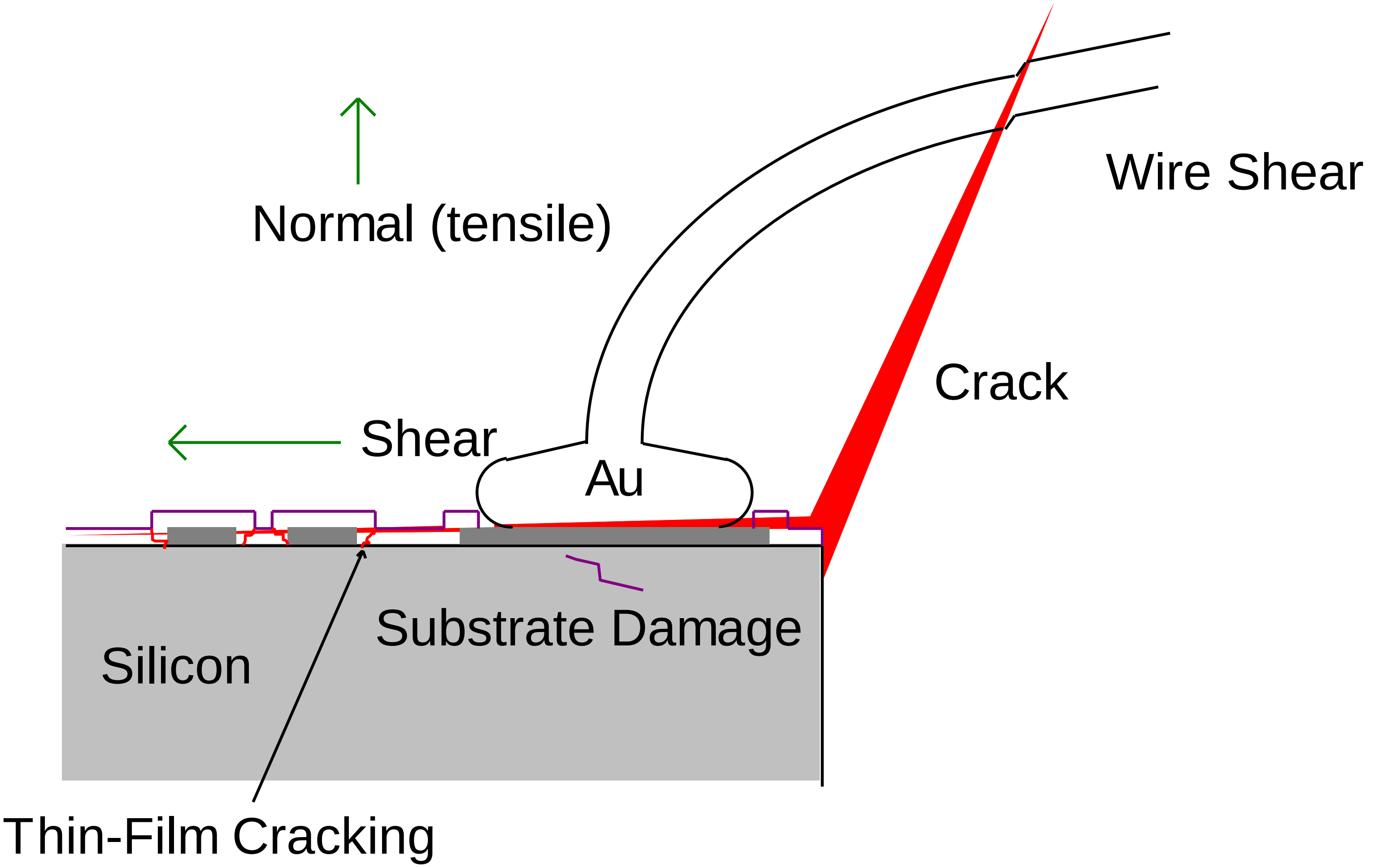
$$\Delta K = Const \times (\alpha_{moldingcompound} - \alpha_{silicon}) \times (T_{min} - T_{neutral})$$

- α is the TCE of MC.

ΔT in temperature cycling-driven models is the temperature difference between the neutral (usually cure) temperature, and the minimum temperature of the cycle. T_{max} is less important.

Package Cracking and Delamination..

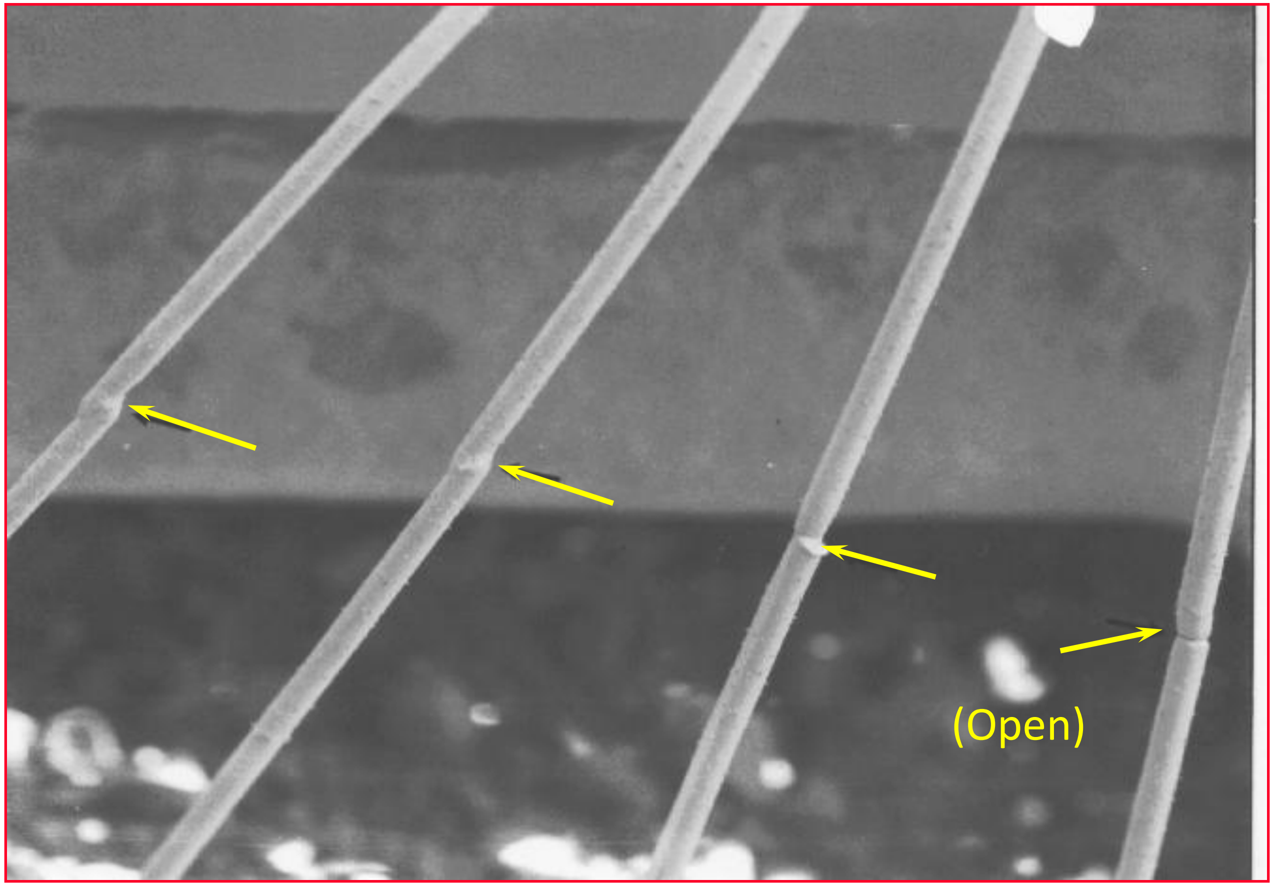
..damages Wires, Bonds, and Passivation Films.



Bond Damage: Wires and Ball Bonds

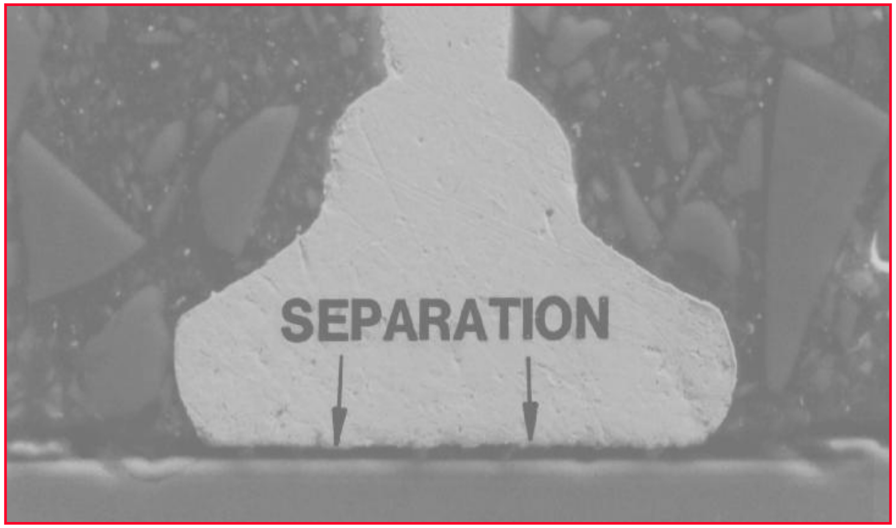
- Cracks can intersect wires, TAB leads.
- Bonds can be sheared at the bond/pad interface
- Shear and tensile normal stress can break wires at their necks.
- Substrate cracks induced during bonding can propagate and cause “cratering” or “chip-out”.

Wire Damage

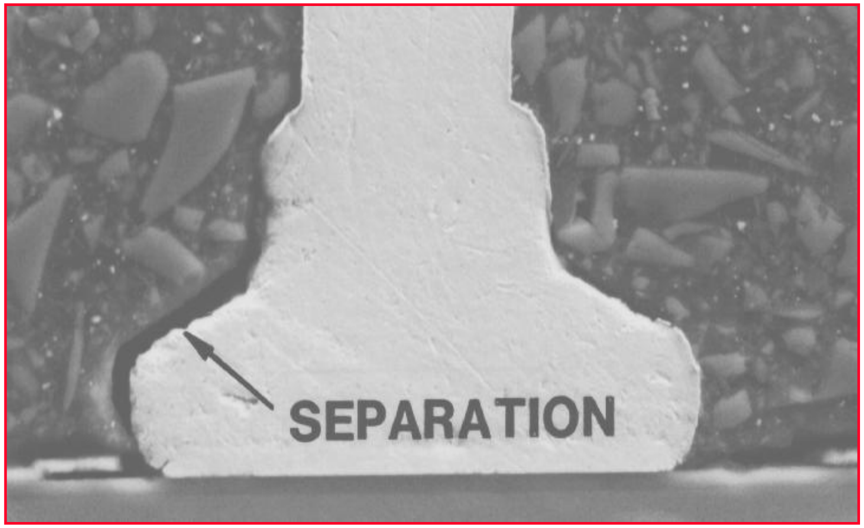


Wires sheared by wire crack

Bond Damage



Sheared Bond



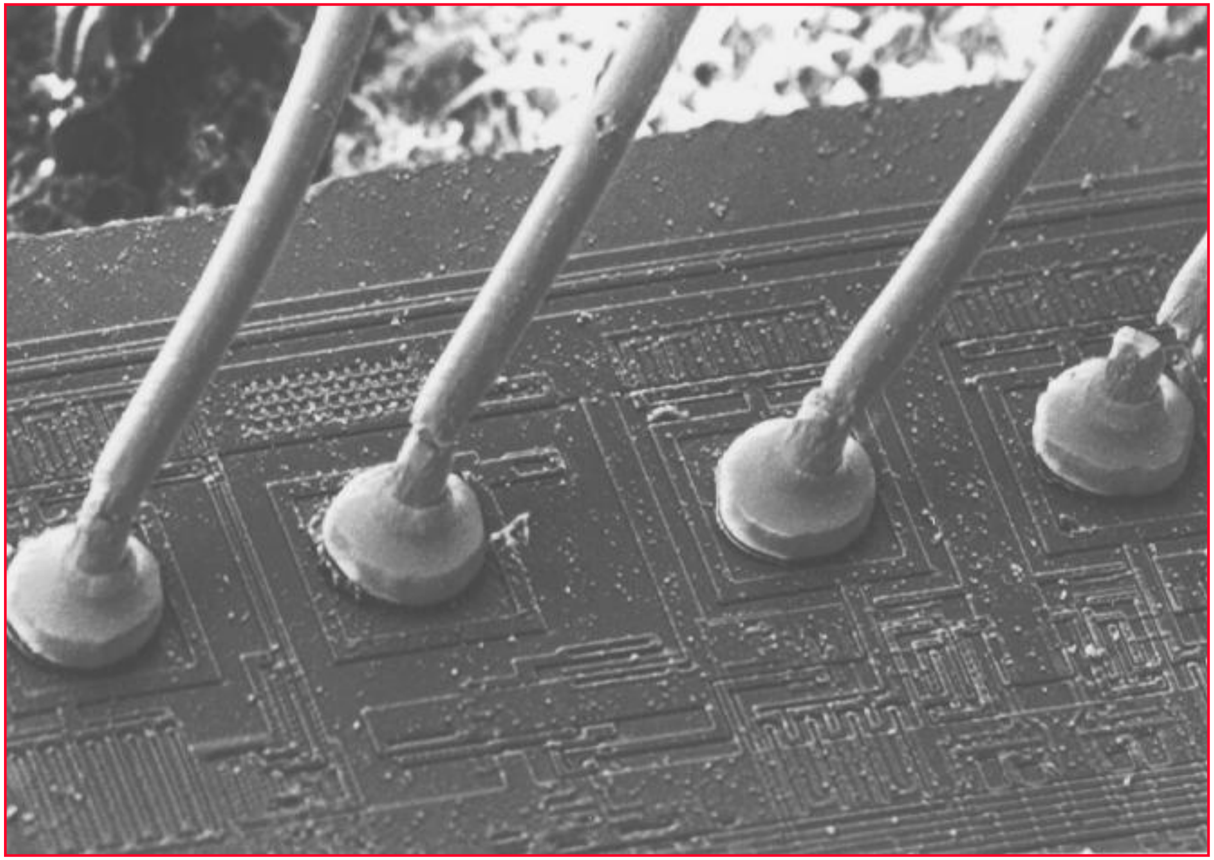
Unfailed Bond

20 μ

Die Corner →

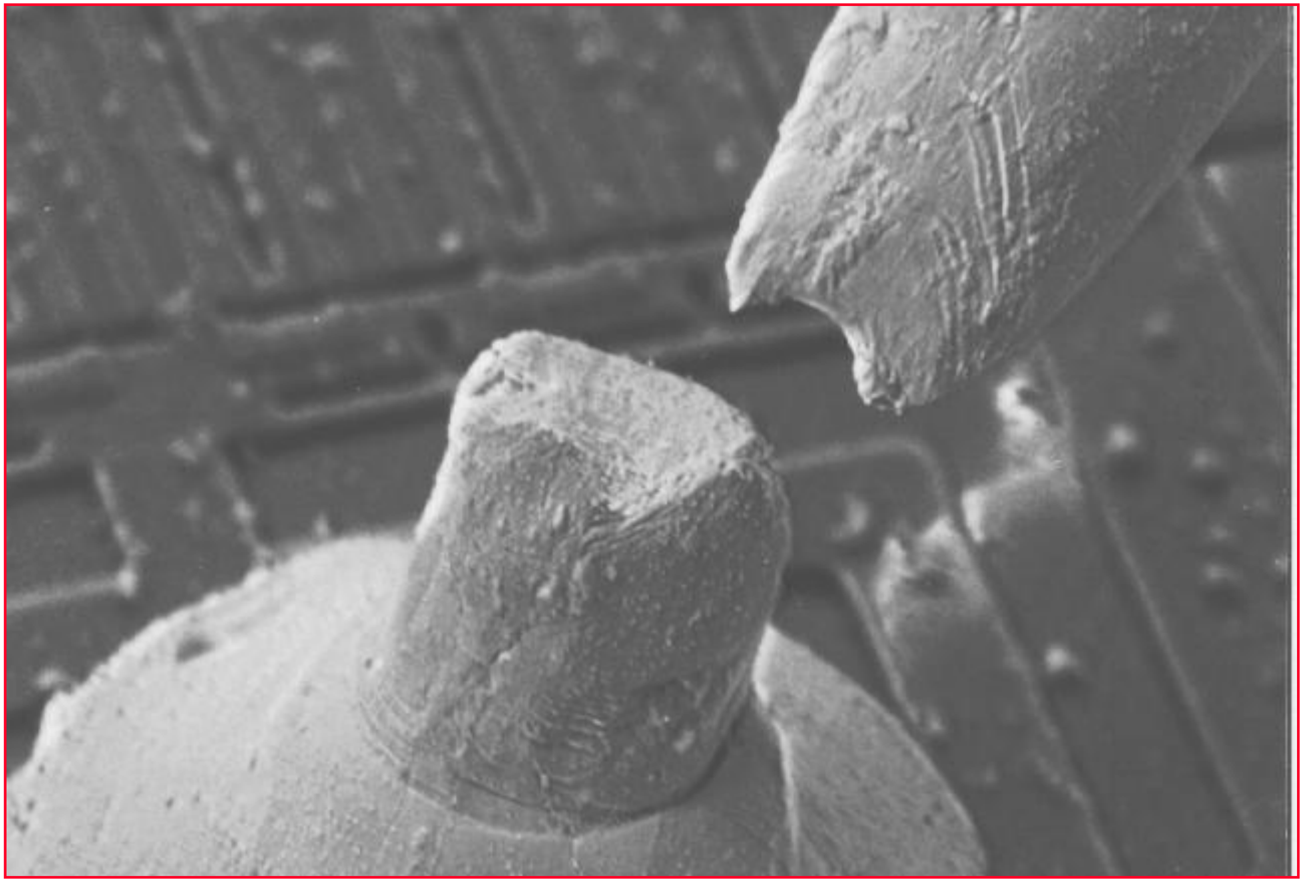
Ball bonds in plastic package after temperature cycle.

Bond Damage



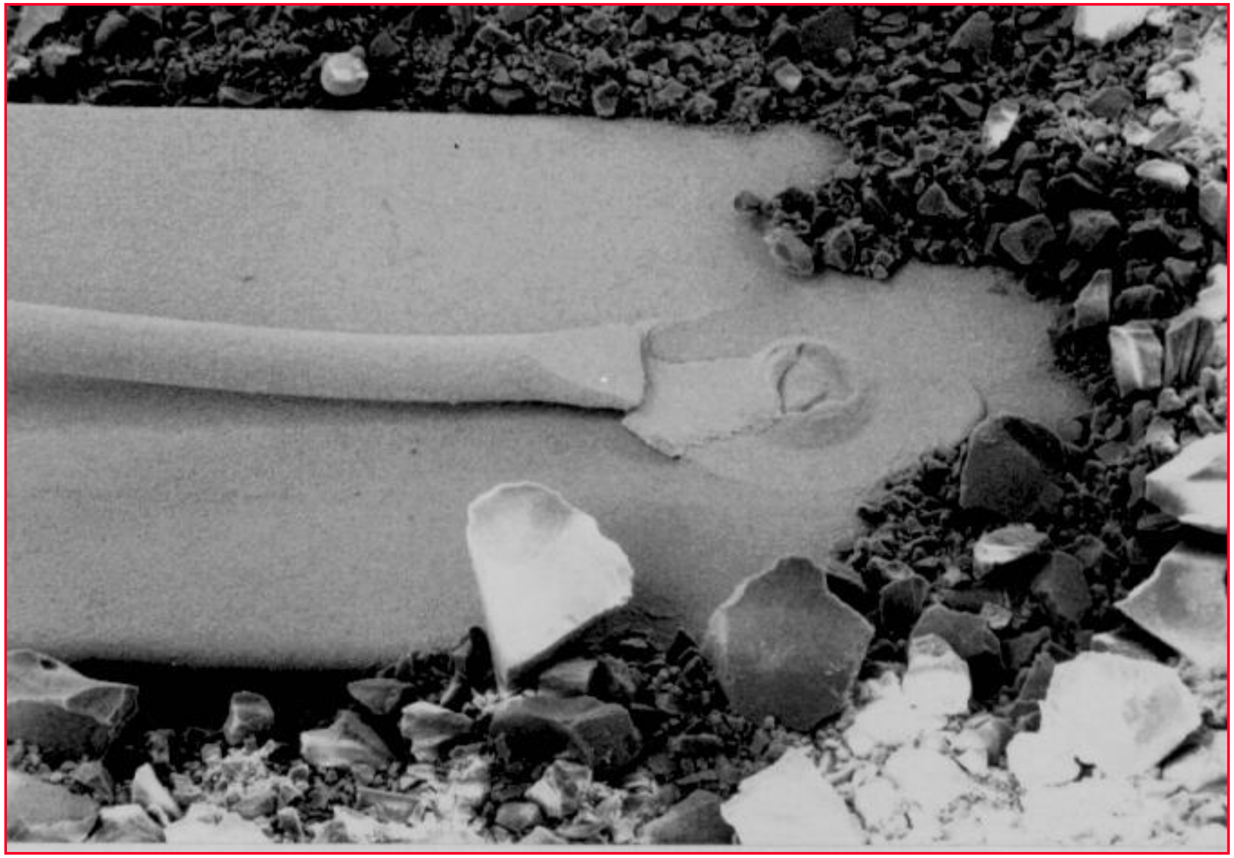
Necking Damage

Bond Damage



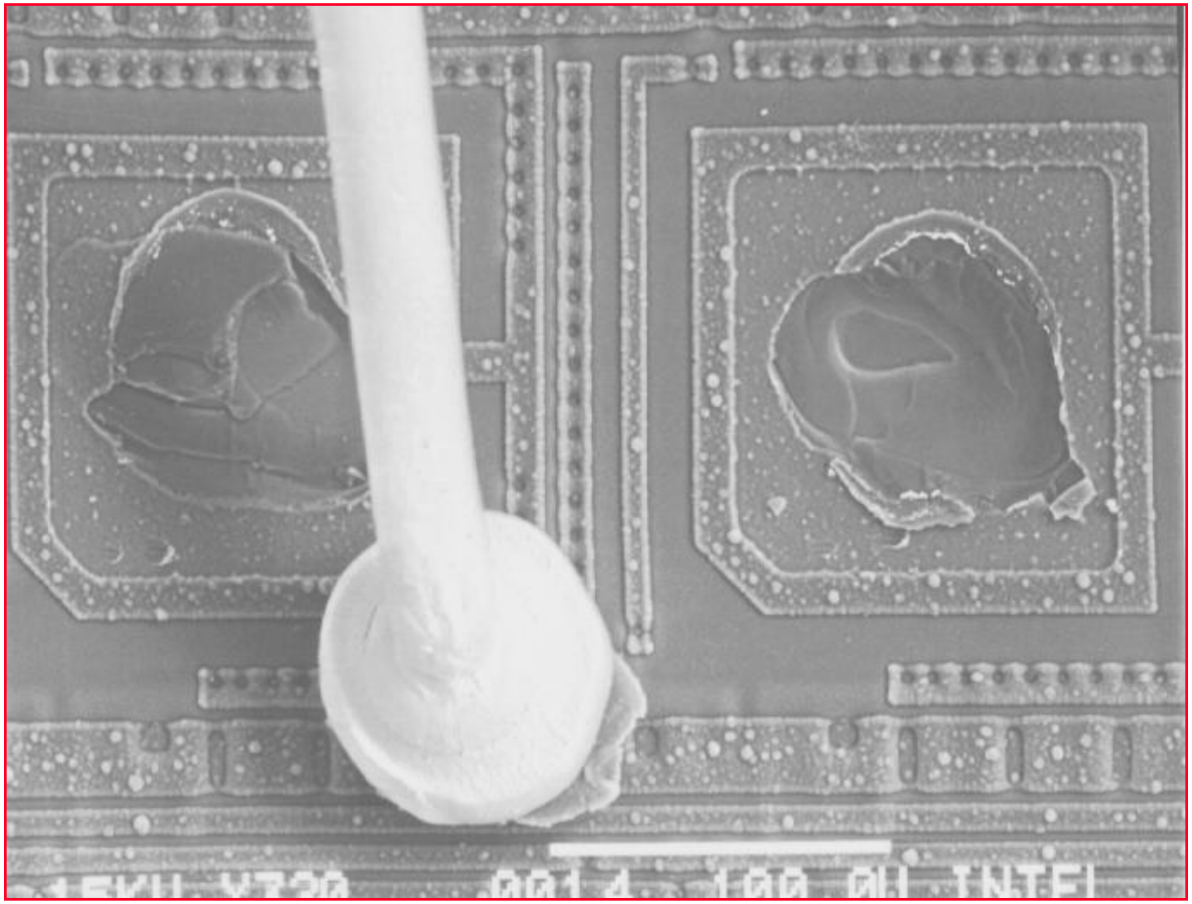
Necking fracture

Bond Damage



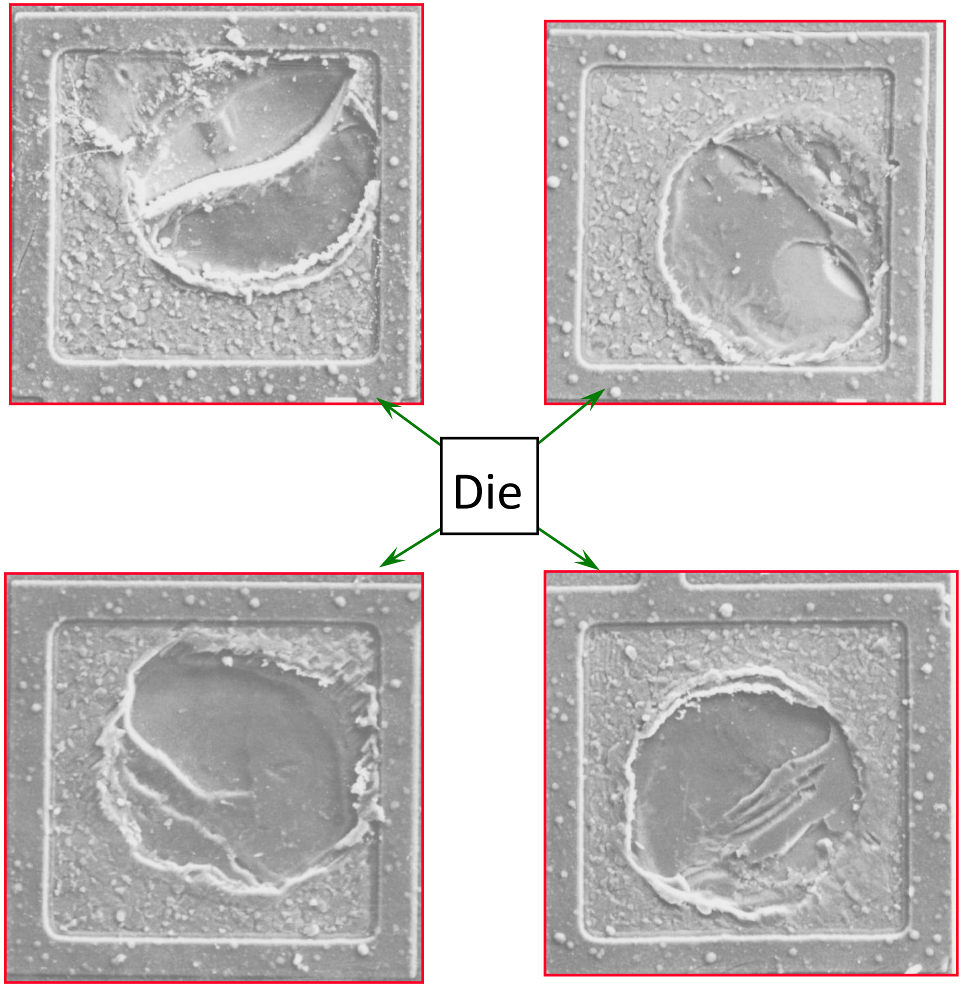
Delamination induced down bond fail after temperature cycle

Bond Damage



Cratering damage on bond pads

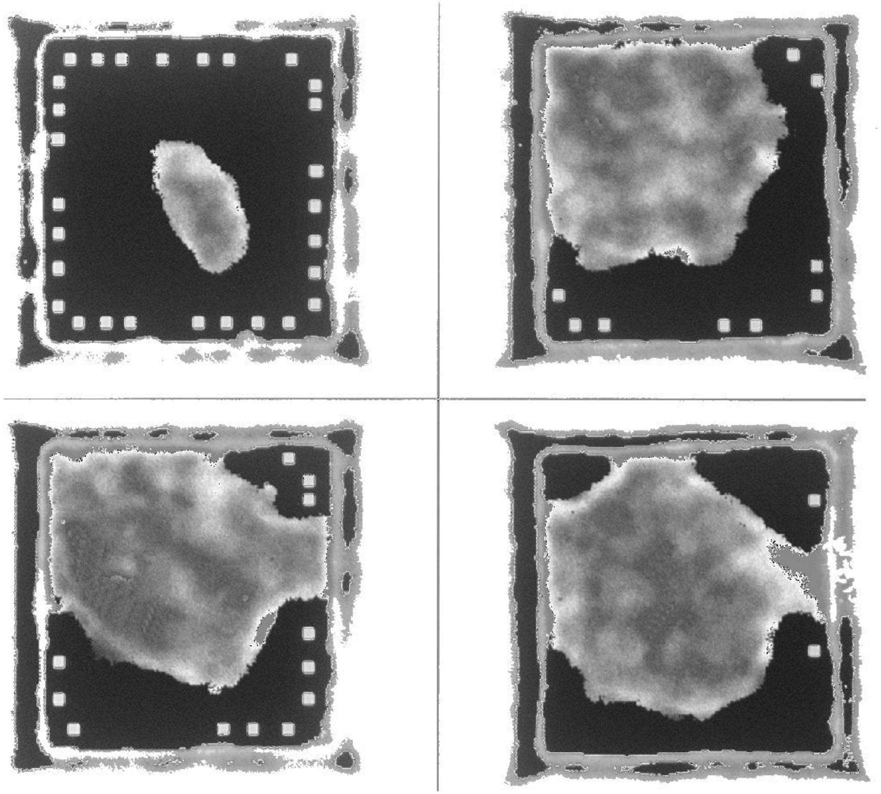
Bond Damage



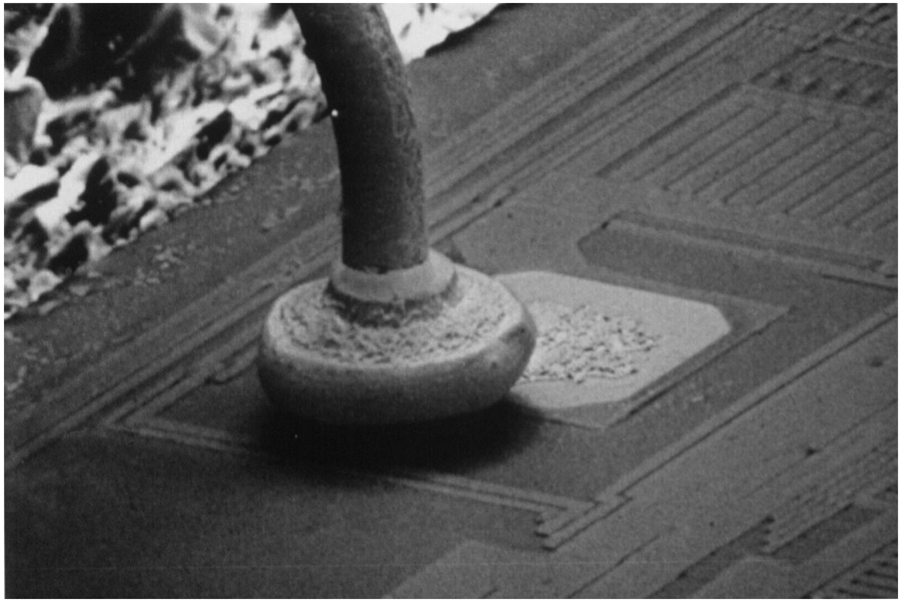
Die

Bond shear at die corners after temperature cycle

Bond Damage and Delamination



Pulse-echo acoustic image of mold compound/ die interface in four devices. Delamination is shown in black. White boxes added to show locations of low bond wire pull strength results.

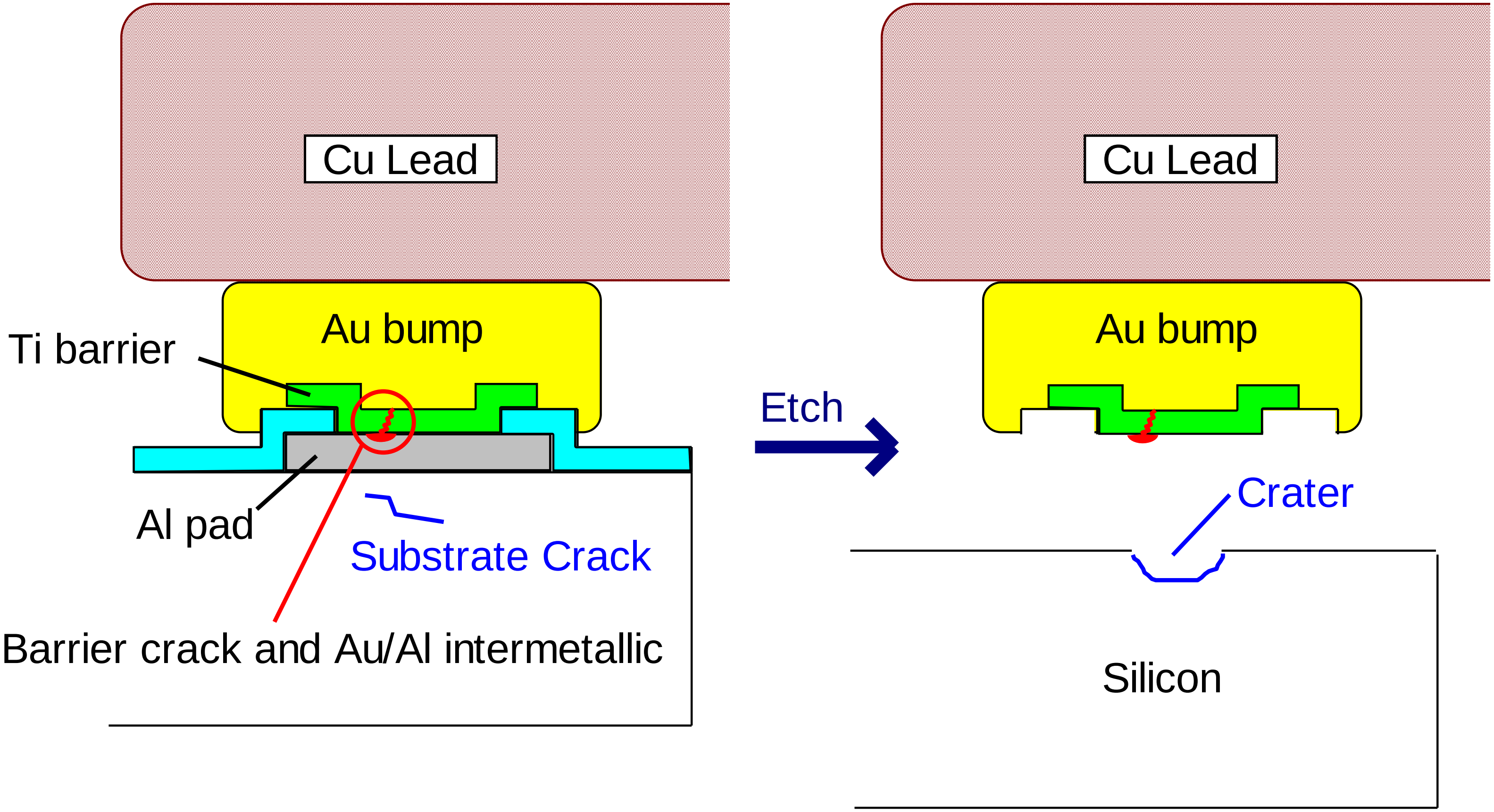


Intermetallic fracture at bond due to shear displacement.

44 PLCC devices that failed after solder reflow and 1000 cycles (-40 to 125C)

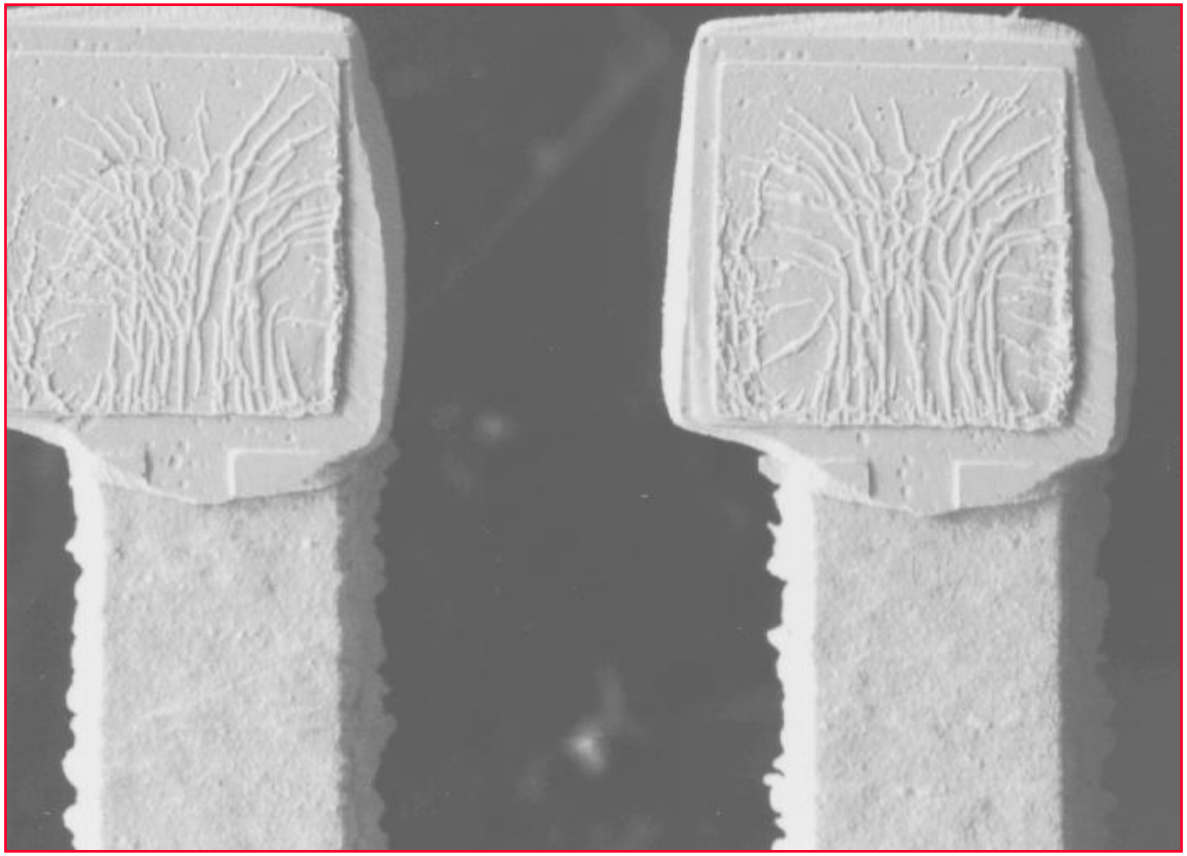
Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, IRPS 1991, 160-166.

Bond Damage (TAB)



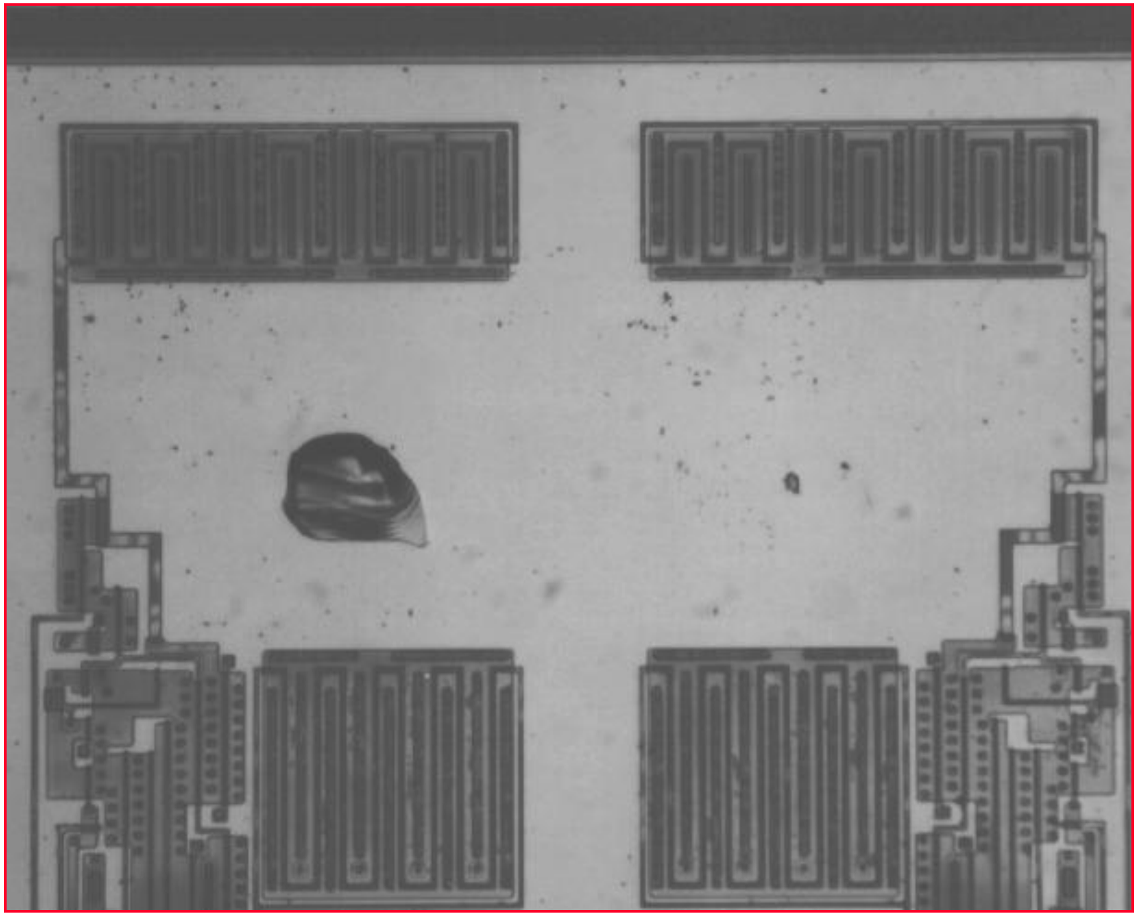
TAB cratering and diffusion barrier damage revealed by wet etch.

Bond Damage (TAB)



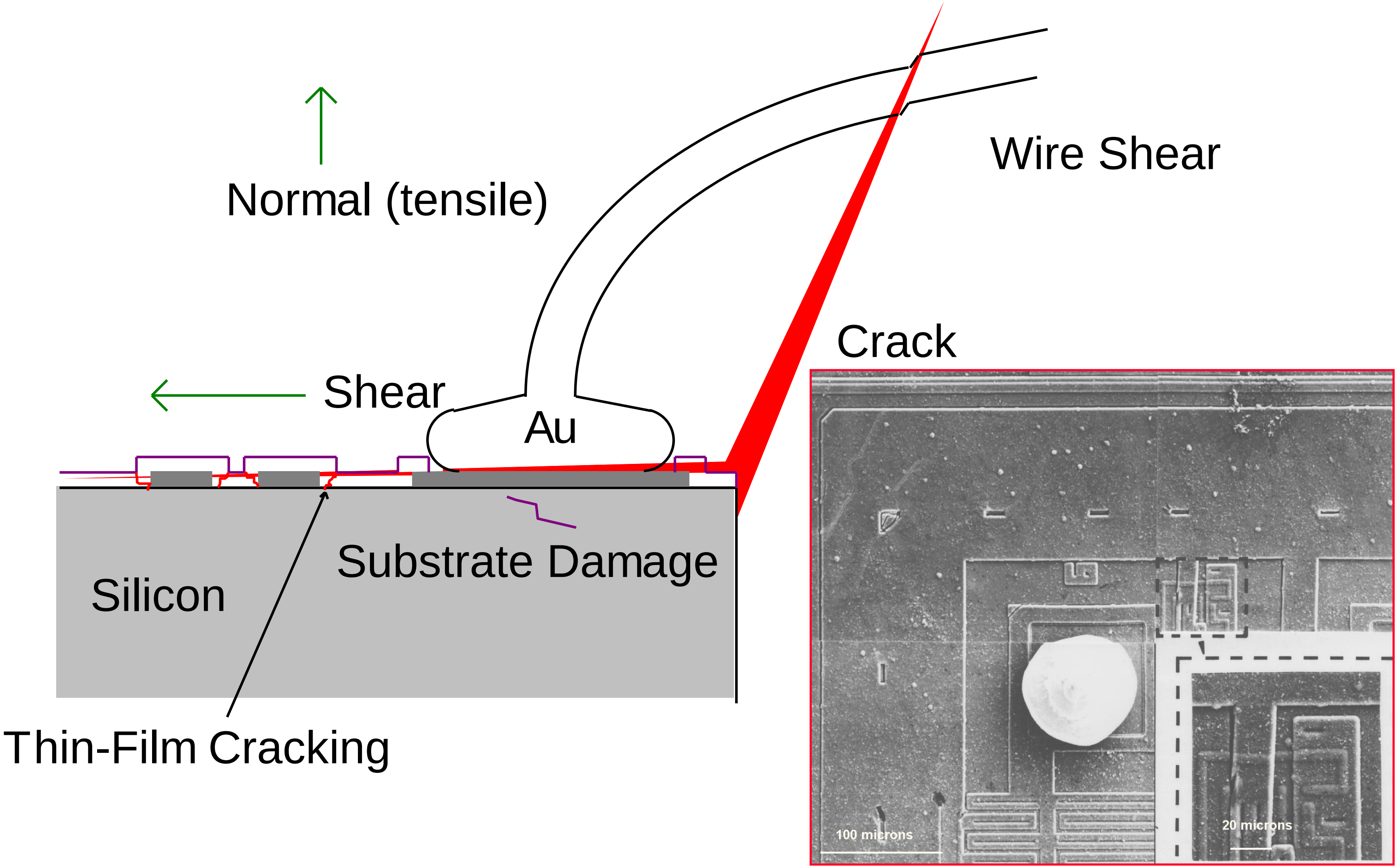
TAB bonds Au/Al intermetallic formed at cracks in Ti barrier

Bond Damage (TAB)



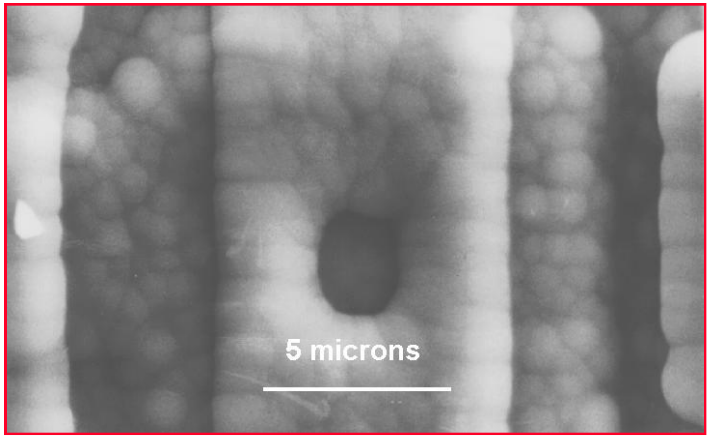
Crater under TAB bonds

Thin-Film Cracking (TFC)

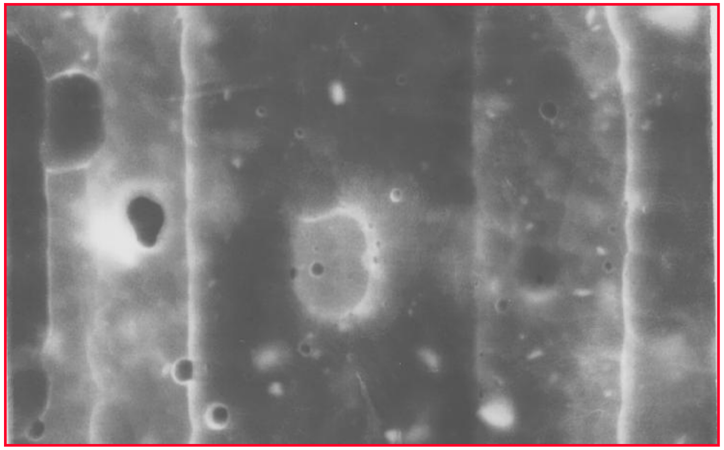


TFC - Plastic Conforms to Die Surface

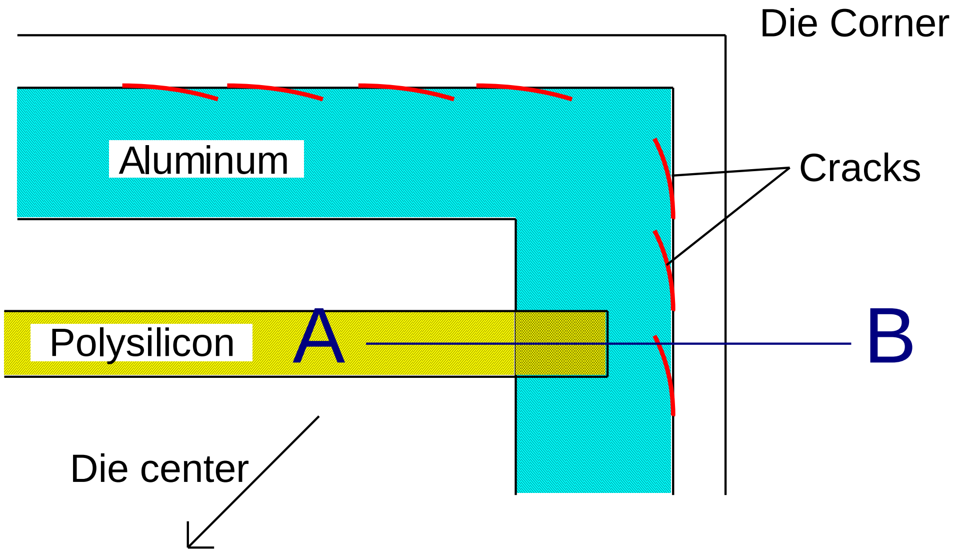
Die Surface

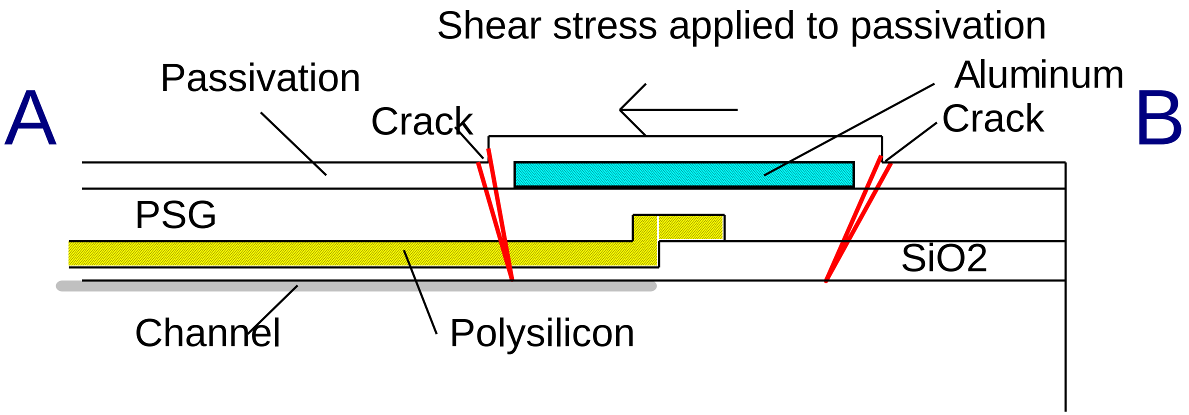


Replica in Plastic

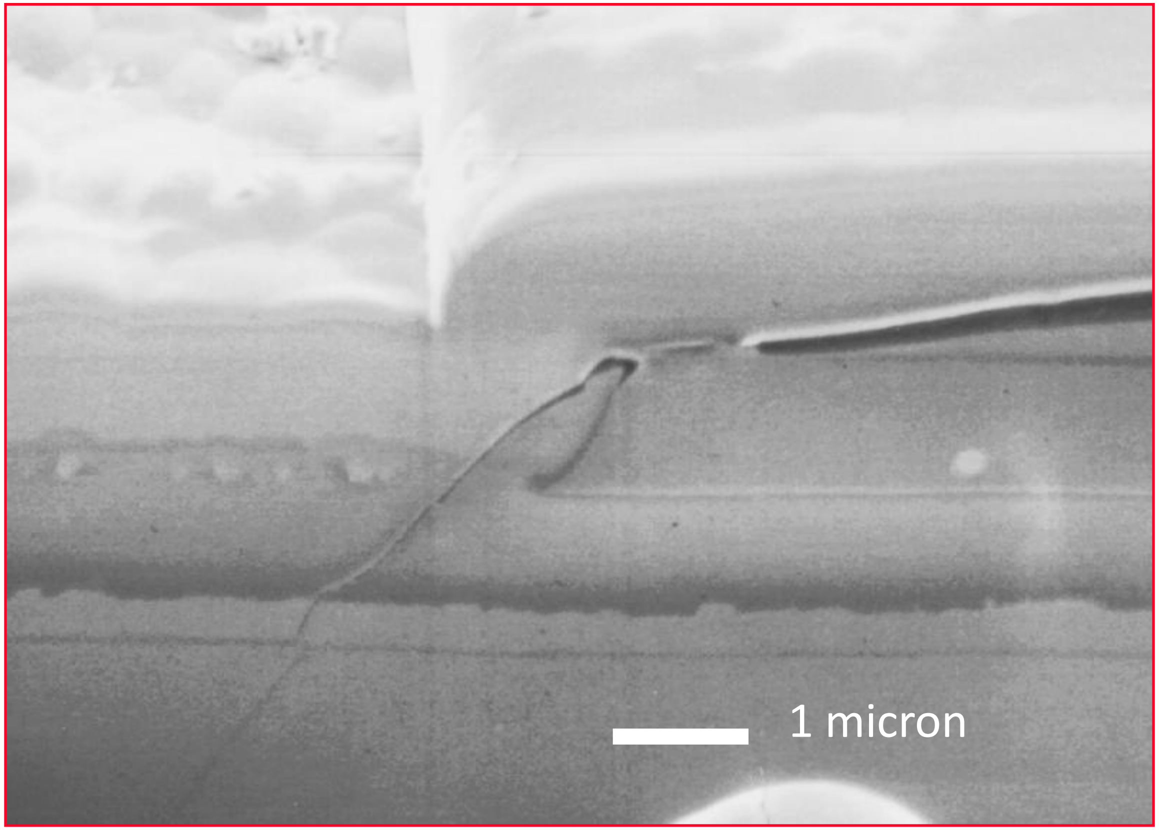


TFC – Effect on Thin Films





Thin-Film Cracking (TFC)

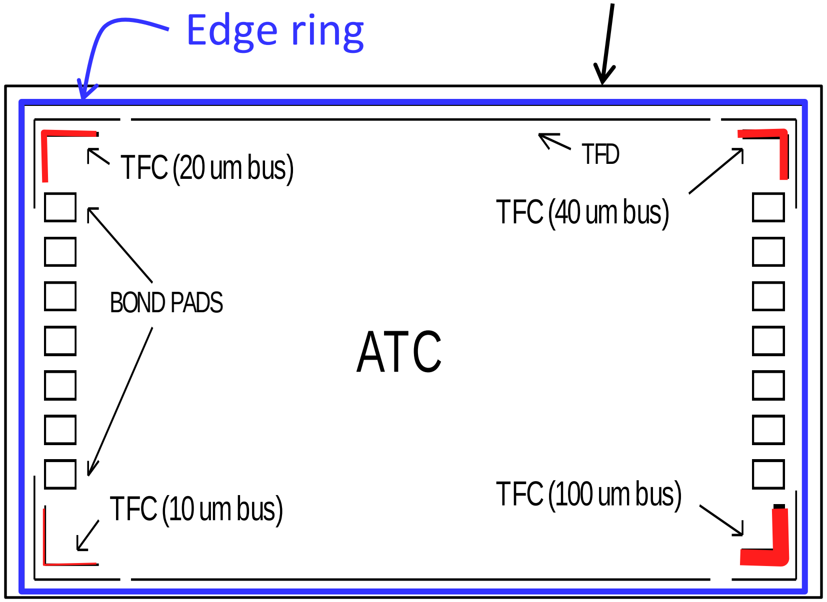


Source: K. Hayes, Intel

Passivation delamination crack propagates into substrate.

Test Chip

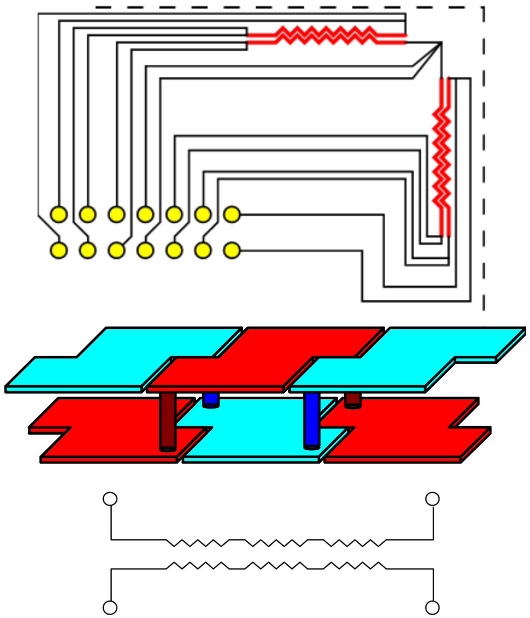
- Thin film cracking can be detected electrically by test structures in the corner of the die.
  - Sensitive to opens and to shorts.
- Buss width is varied to determine design rule.



Die edge (saw cut).

Edge ring

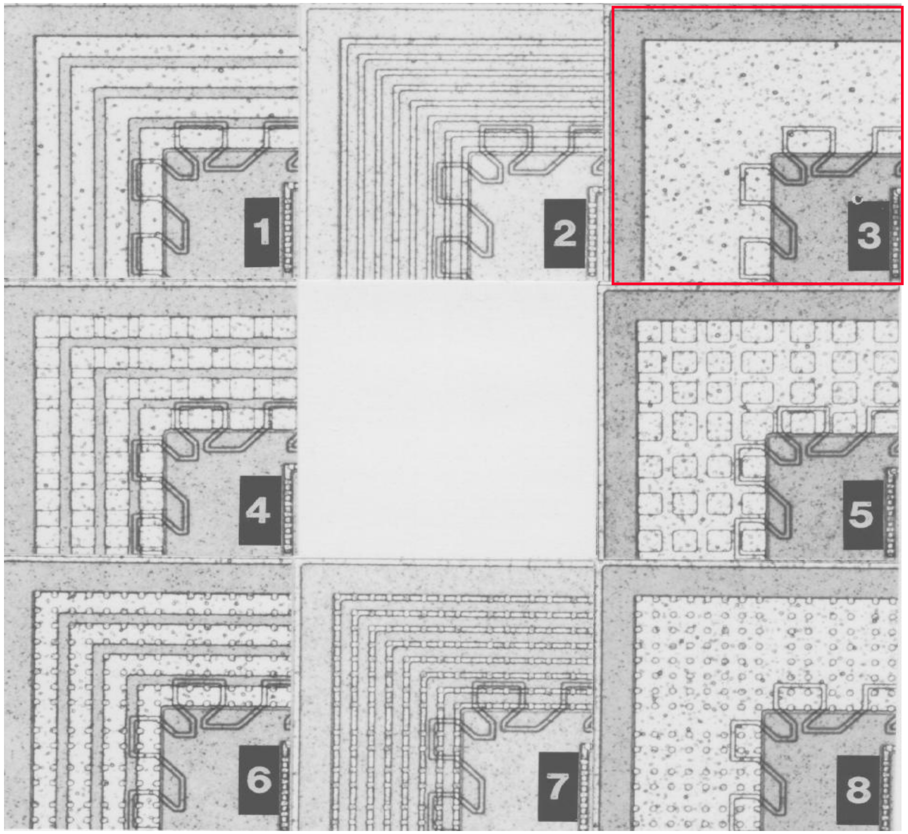
TFC sensor



TFC – Effect of Buss Width

Factors Affecting TFC: Buss Width Effect

Polysilicon meanders under buss edge are vulnerable to crack-induced opens.



No Contacts

17 µ contacts

3 µ contacts

Buss Widths

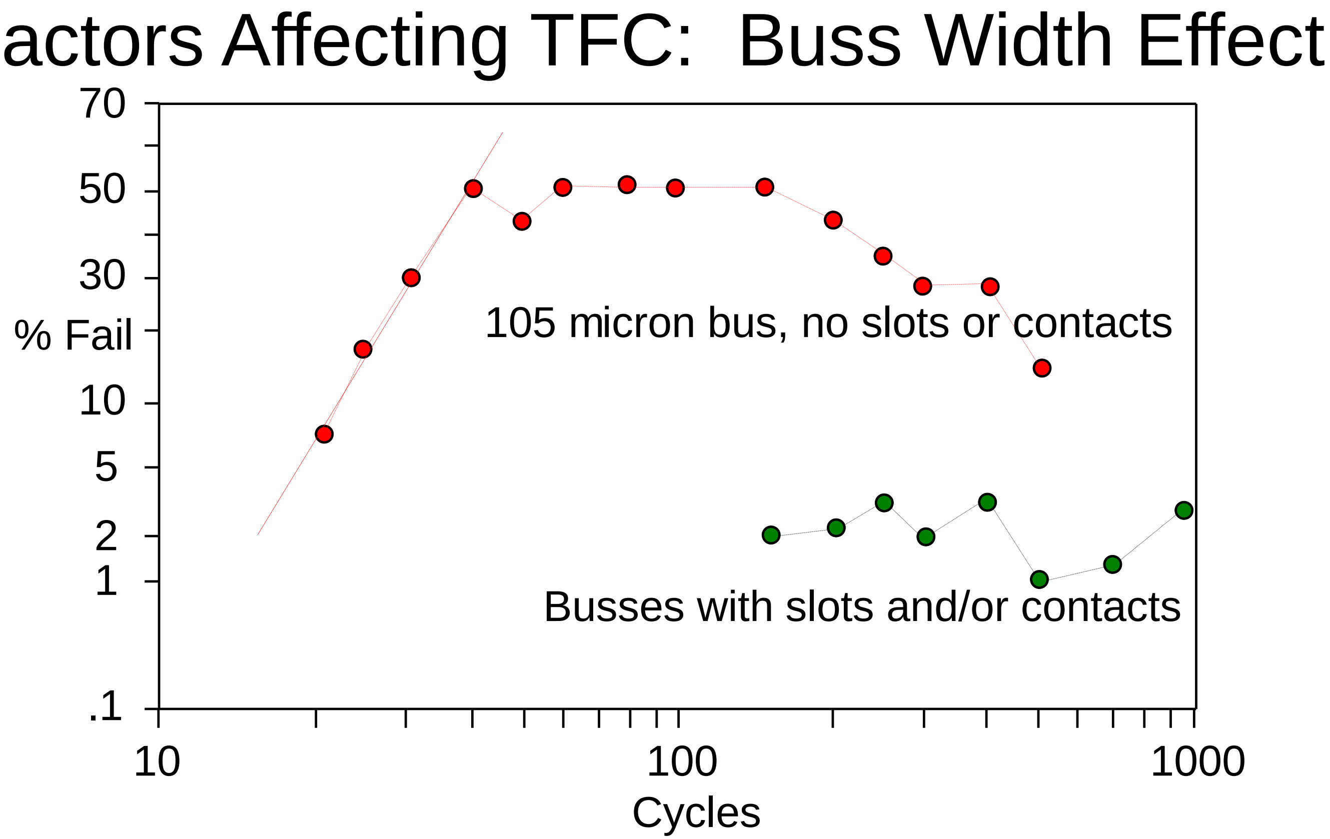
21 µ

7 µ

105 µ

Source: [Shirley & Blish, "Thin Film Cracking and Wire Ball Shear...," IRPS 1987.]()

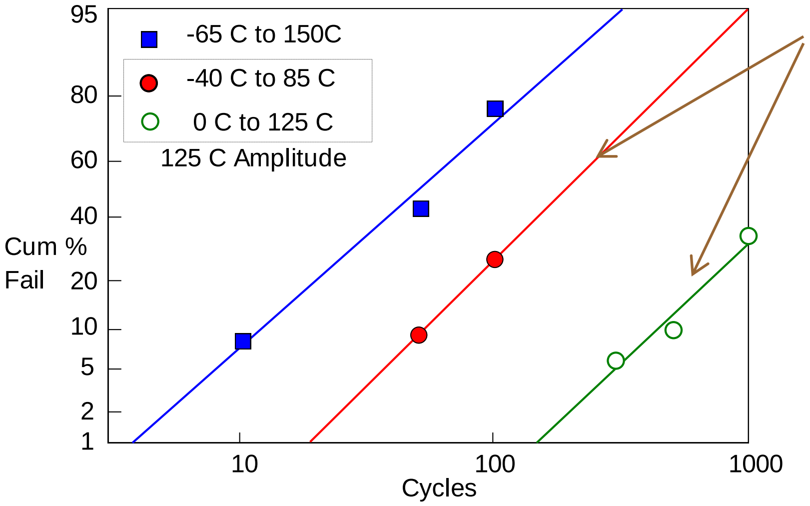
TFC – Effect of Buss Width, ct'd



Narrow buss, or contacts, stabilizes buss, reduces incidence of TFC. Leads to buss width design rules, and buss slotting in die corners.

TFC – Effect of Temperature Cycle

- Drivers: T/C conditions, and number of cycles.
- Mimimum T/C temperature, not amplitude, is key aspect of stress.
  - Stress depends on difference between cure temperature (neutral stress) and minimum stress temperature.

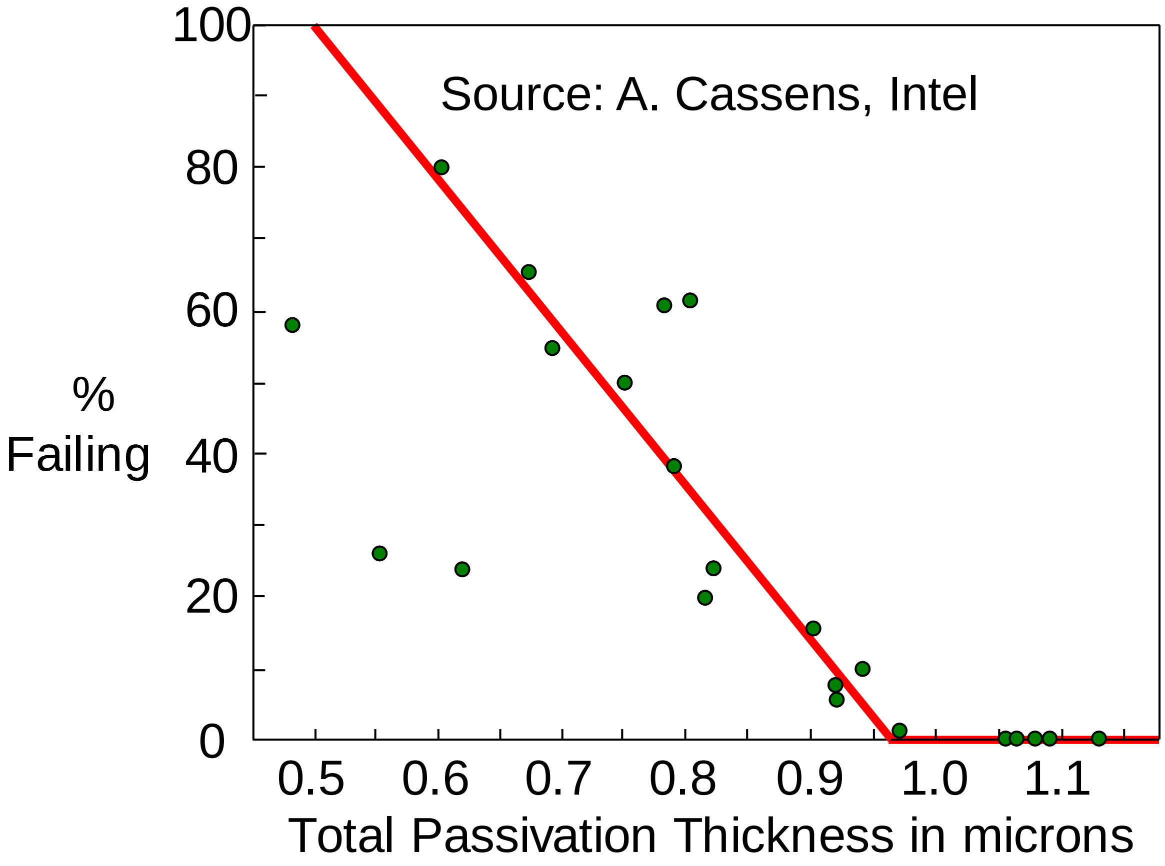


Same amplitude!

Source: C. F. Dunn and J. W. McPherson, “Temperature-Cycling Acceleration Factors for Aluminum Metallization Failure in VLSI Applications,” IRPS, 1990.

TFC – Effect of Passivation Thickness

- Fraction of PDIP-packaged SRAM failing.
- Post 1K cycle of T/C C.
- No Polyimide die coat.
- Thicker passivation is more robust.



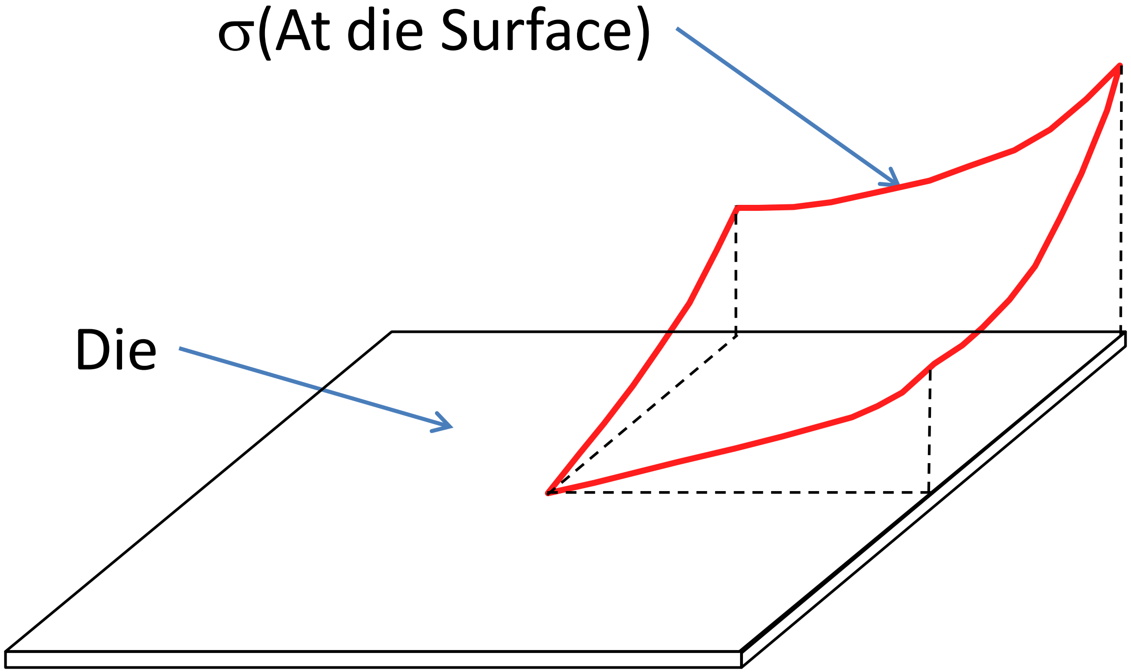
TFC – Effect of Compliant Overcoat

- SRAM in PDIP
- Temperature Cycle Condition C
- Polyimide Overcoat

	200 cycles	500 cycles	1000 cycles
No Polyimide	0/450	13/450	101/437
Polyimide	0/450	0/450	0/450

Theory of TFC

- Shear stress applied to die surface by MC
  - Is maximum at die corners
  - Zero at die center.



Theory of TFC, ct’d

- Buss width effect: Okikawa et. al.
- Passivation thickness effect: Edwards et al.
- TFC occurs when and where

$$\sigma(\text{Passivation Surface}) > K \times E \times \left(\frac{t}{L}\right)^2$$

  - K = dimensionless constant
  - E = Young’s modulus of passivation
  - t = Passivation thickness
  - L = Buss width

Thicker passivation, and/or narrower busses implies less TFC.

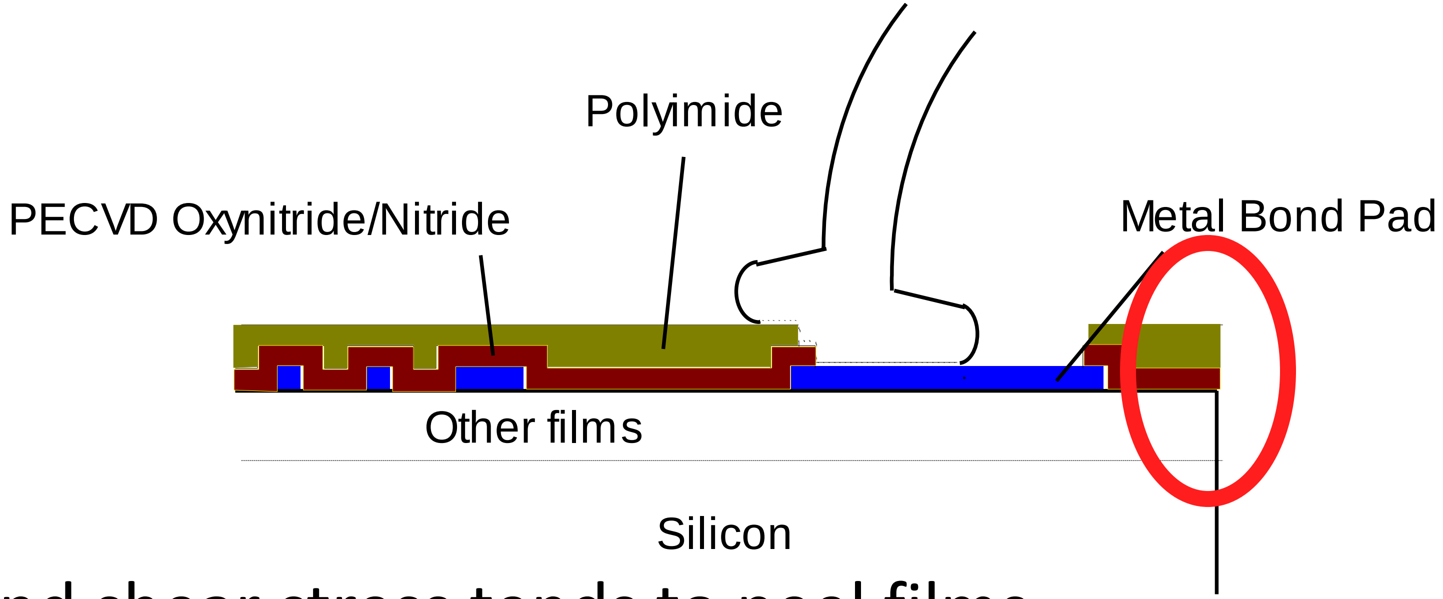
Sources: Okikawa, et al. ISTFA, Oct. 1983. Edwards, et al. IEEE-CHMT-12, p 618, 1987

Outline

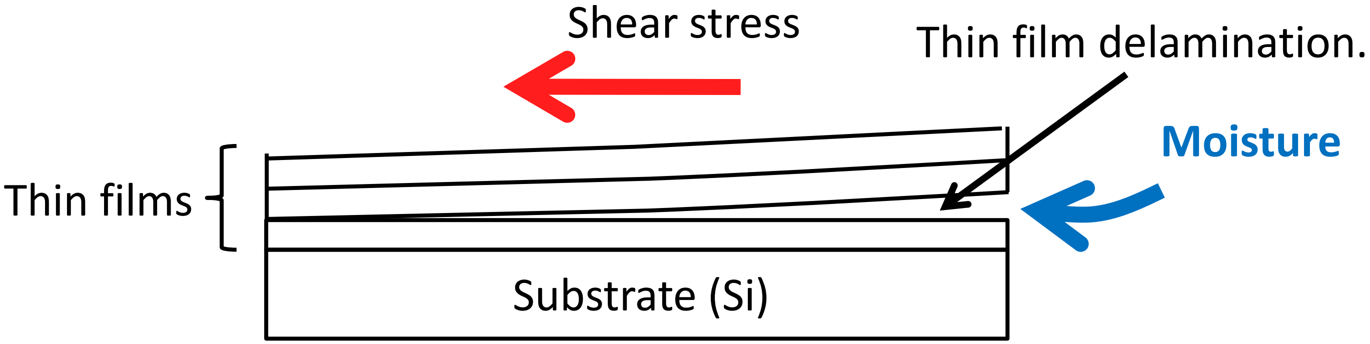
- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- ● Moisture-mechanical Mechanisms
- Technology Update

Thin Film Delamination

- Saw cut exposes thin film edges to moisture..

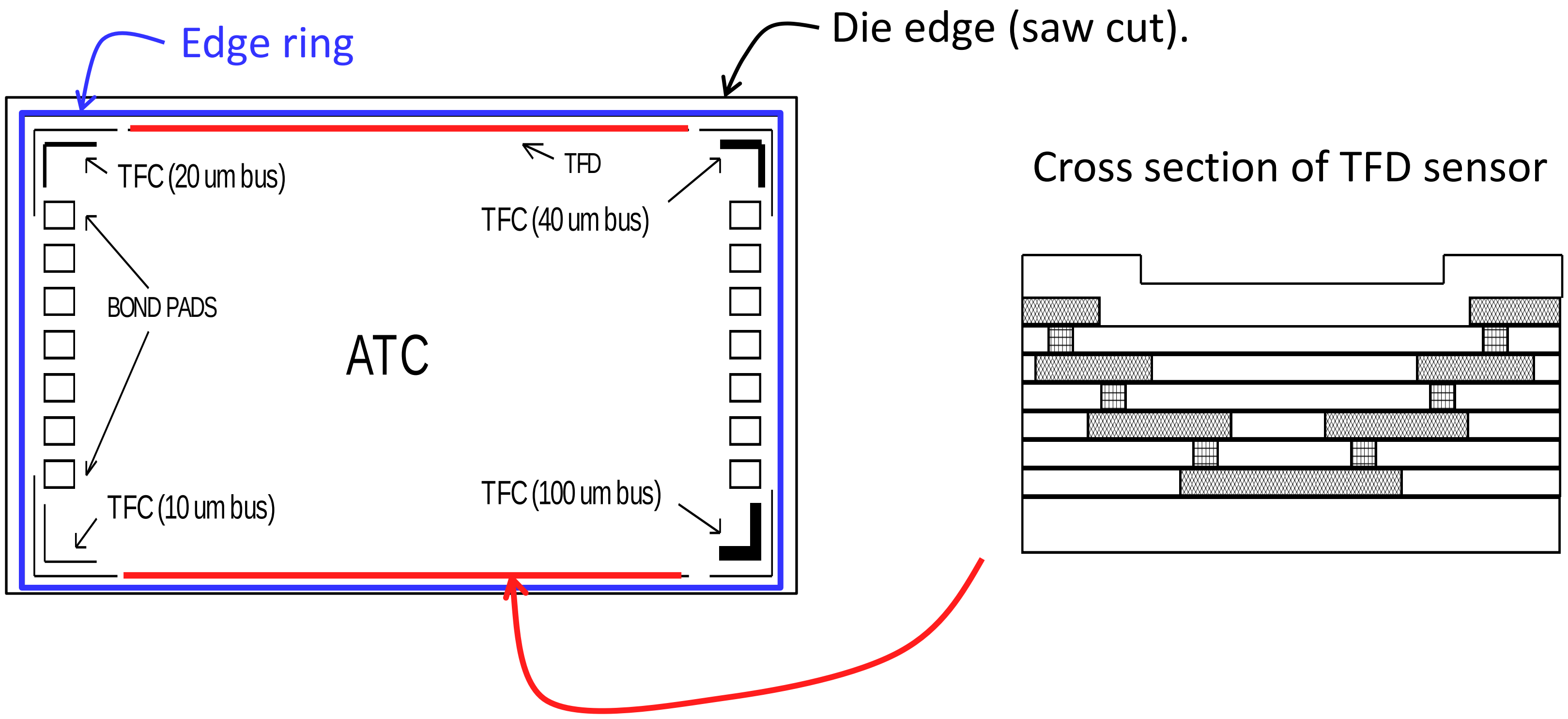


- And shear stress tends to peel films.

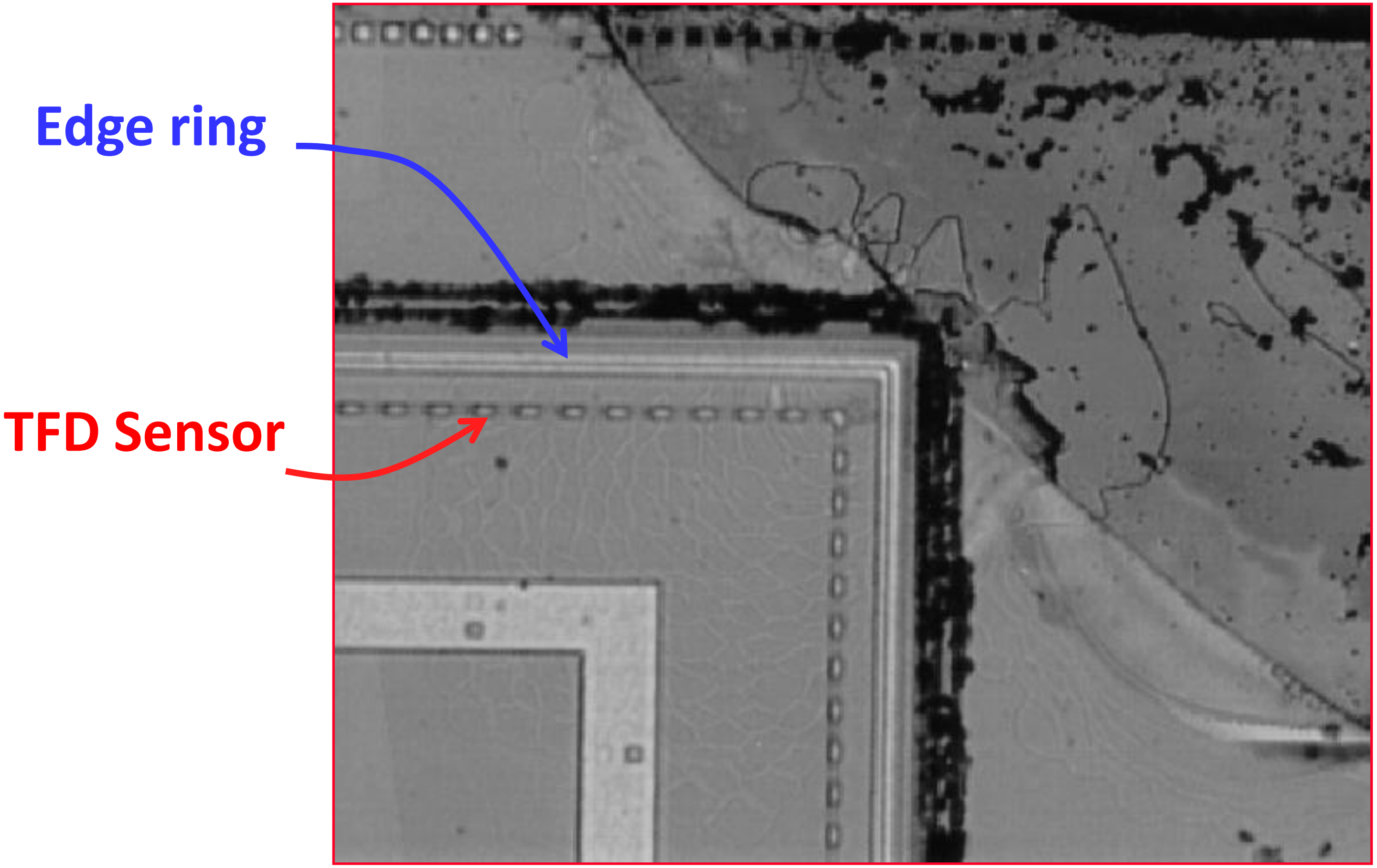


Test Chip

- "Edge rings" are lateral moisture barrier.
- Effectiveness of edge rings can be tested electrically by a TFD sensor on a test chip.



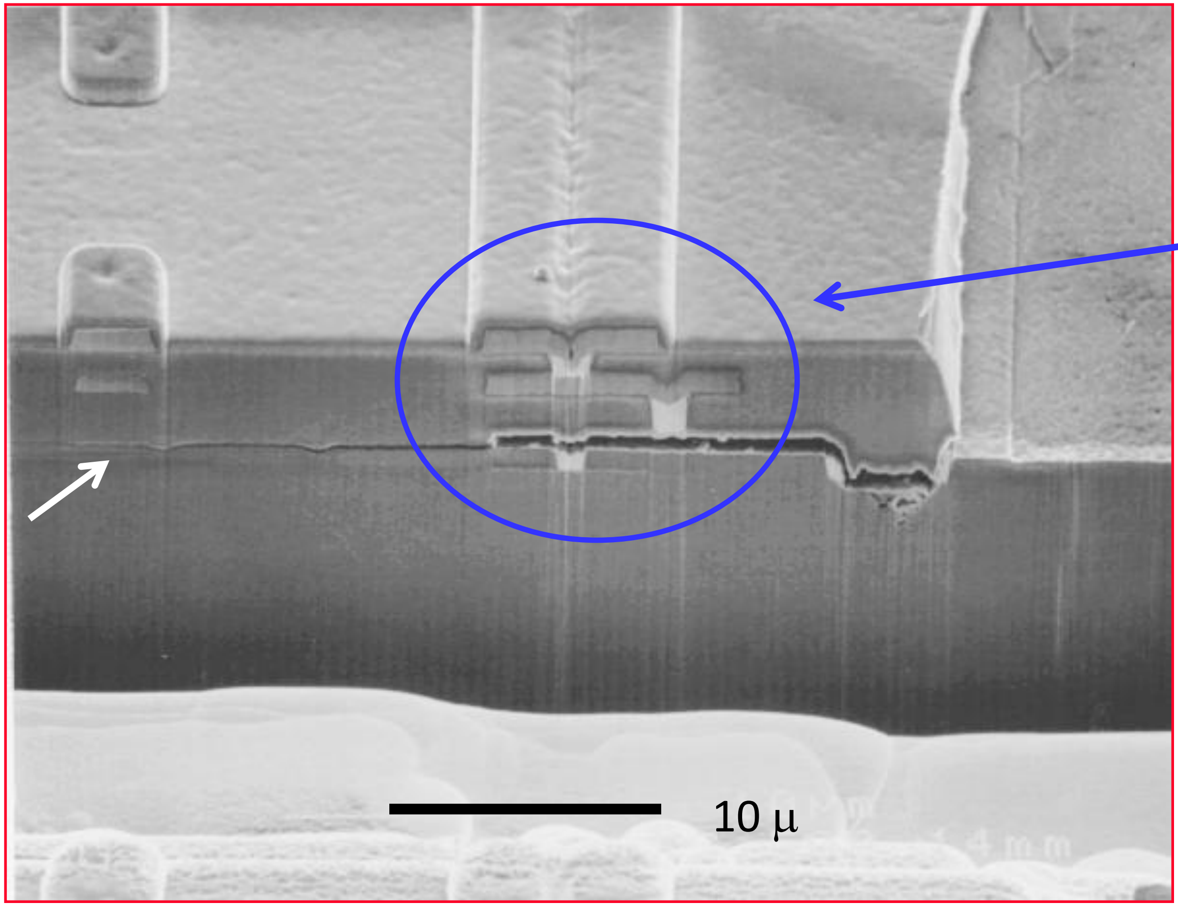
Thin-Film Delamination



Source: C. Hong
Intel

Delamination at die edge after 168 hours of steam.

Thin-Film Delamination



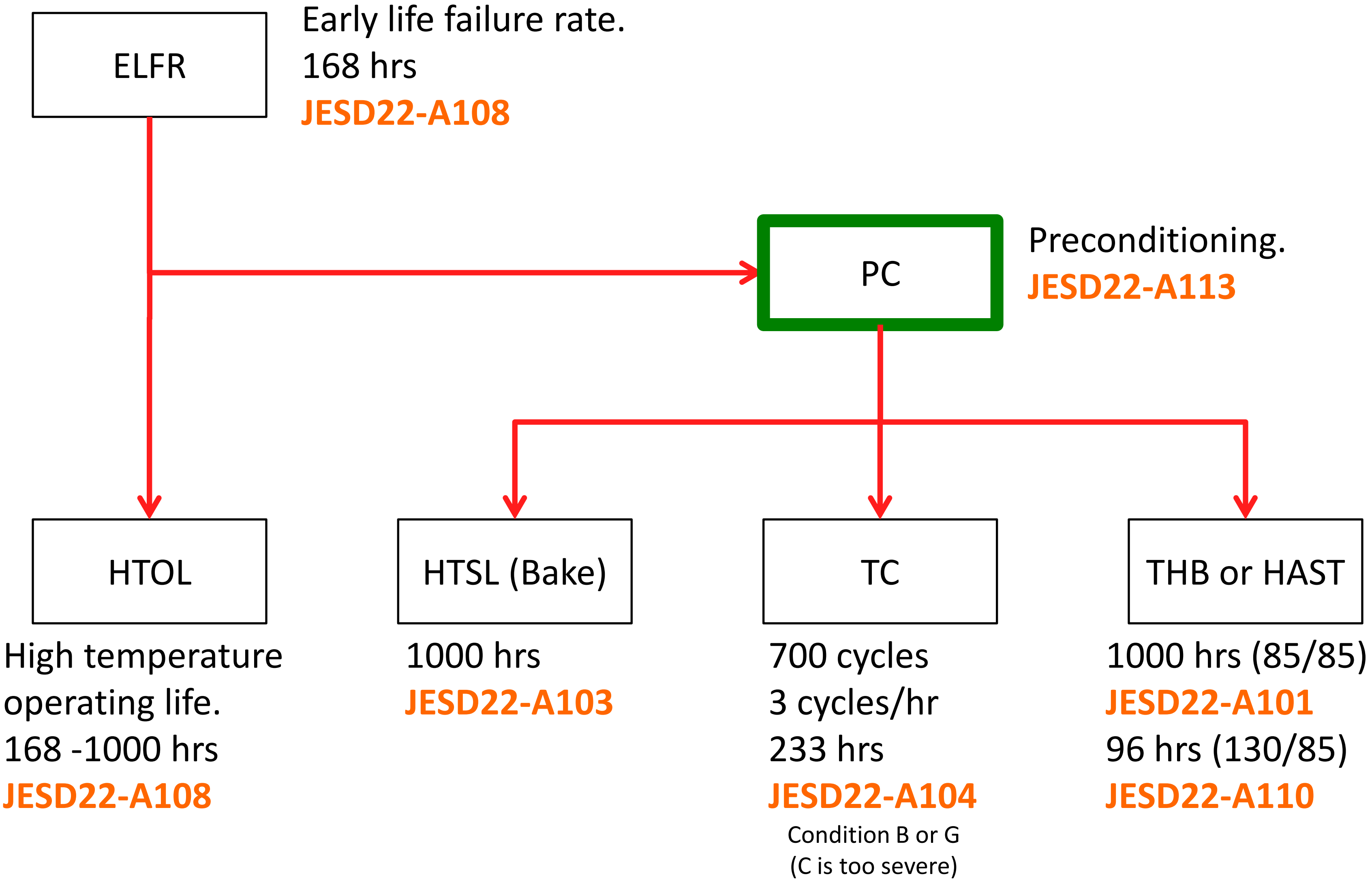
Edge Ring

Crack breaks continuity of **TFD sensor**

Source: C. Hong Intel

Delamination at die edge after 168 hours of steam.

Popcorn Mechanism



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

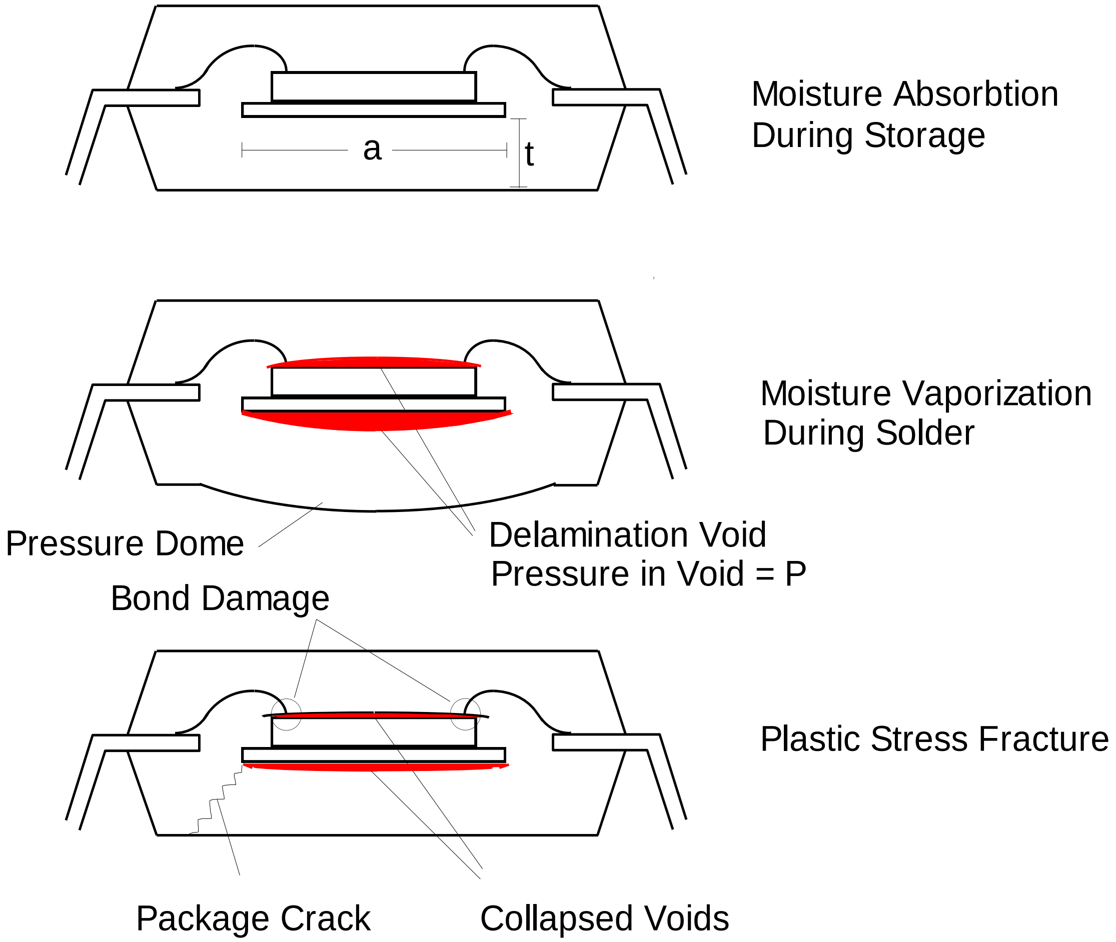
TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Popcorn Mechanism



Moisture Absorbtion
During Storage

Moisture Vaporization
During Solder

Pressure Dome

Delamination Void
Pressure in Void = P

Bond Damage

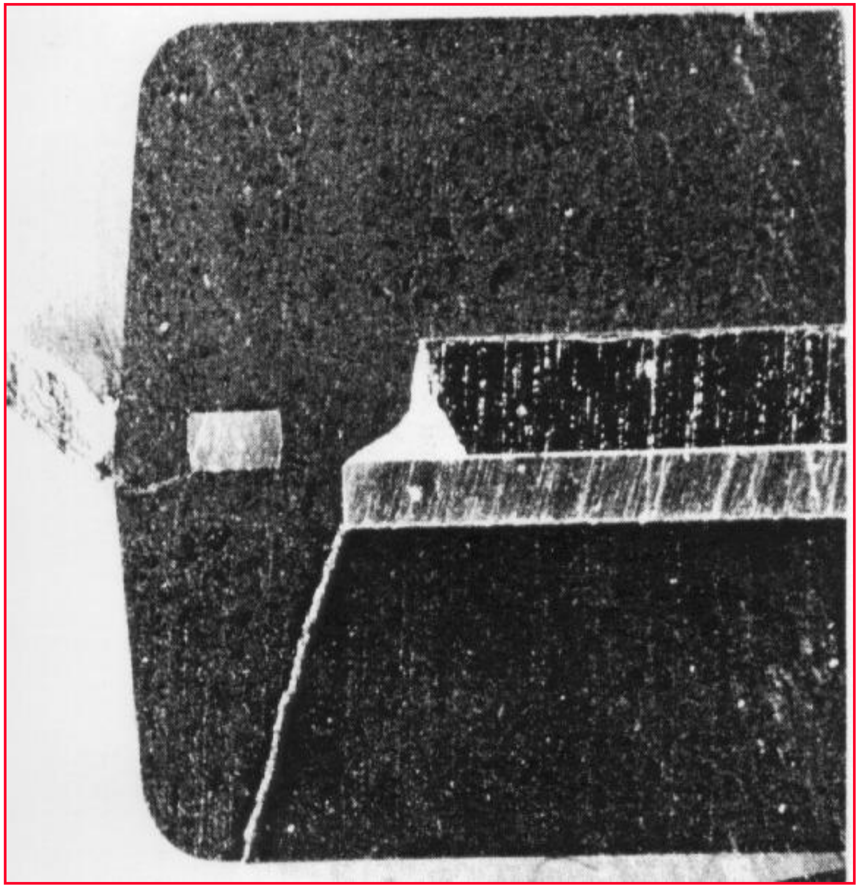
Plastic Stress Fracture

Package Crack

Collapsed Voids

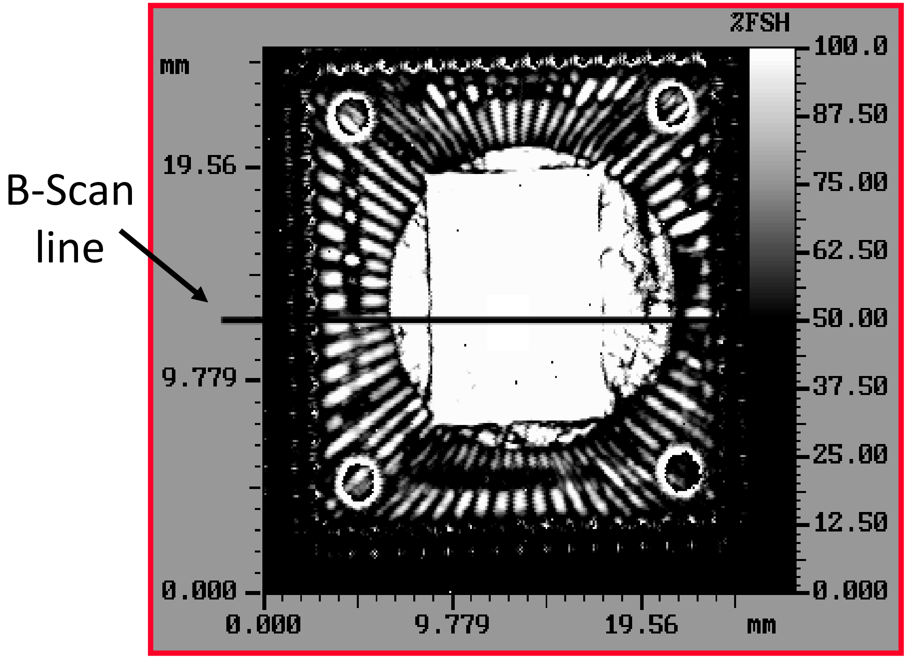
Plastic package cracking due to “popcorn” effect during solder reflow

Popcorn Damage

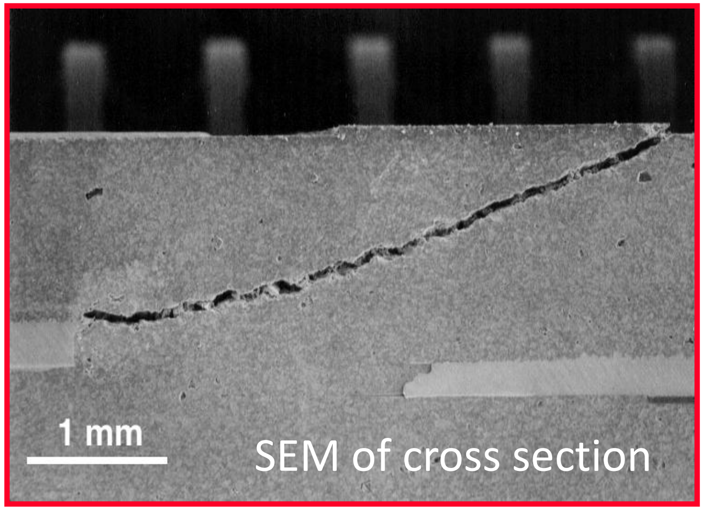


Plastic package cracking due to “popcorn” effect during solder reflow

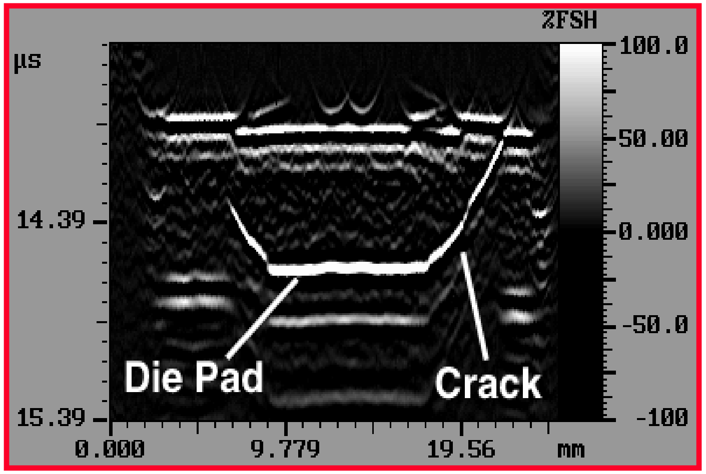
Popcorn Damage



Pulse-echo acoustic image through back of 68PLCC that developed popcorn cracks during solder reflow



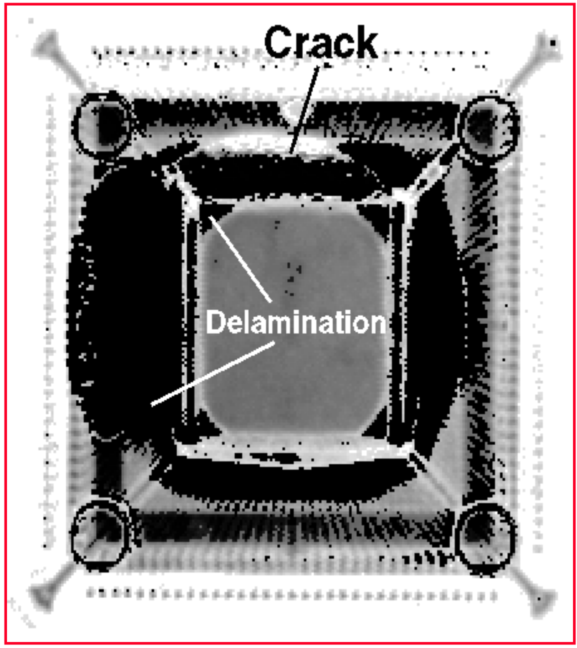
SEM of cross section



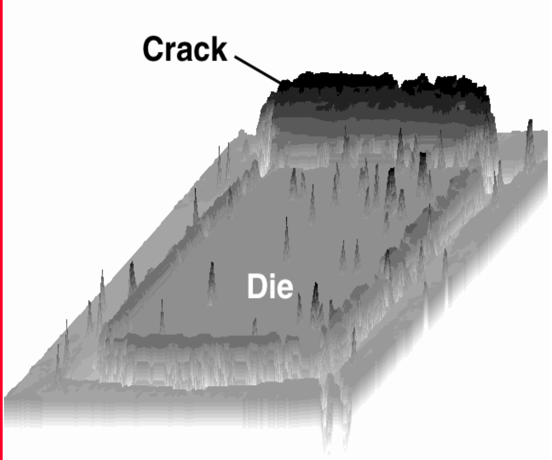
Acoustic B-scan

Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, in "Characterization of Integrated Circuit Packaging Materials", Butterworth-Heinemann, 79-96, 1993.

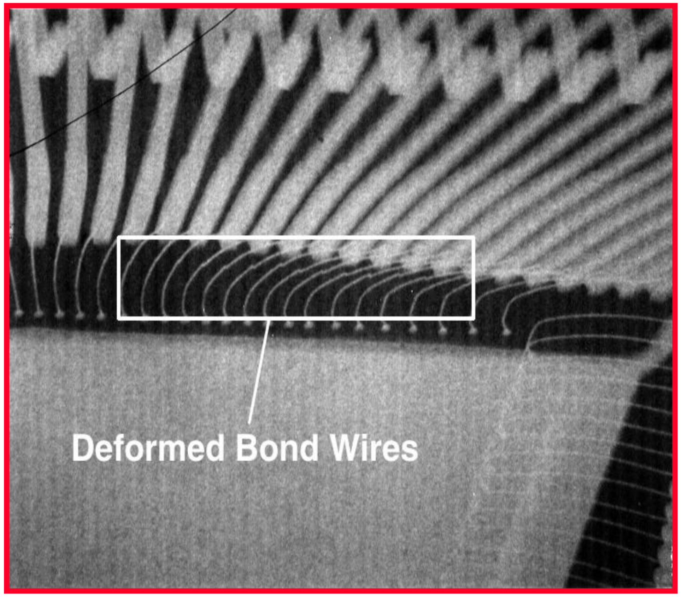
Popcorn Damage



Pulse-echo acoustic image through top (delamination in black)



Acoustic time-of-flight image indicating package crack



Real-time x-ray image showing deformation in wires where they intersect the crack

132 lead PQFP which was damaged during solder reflow.

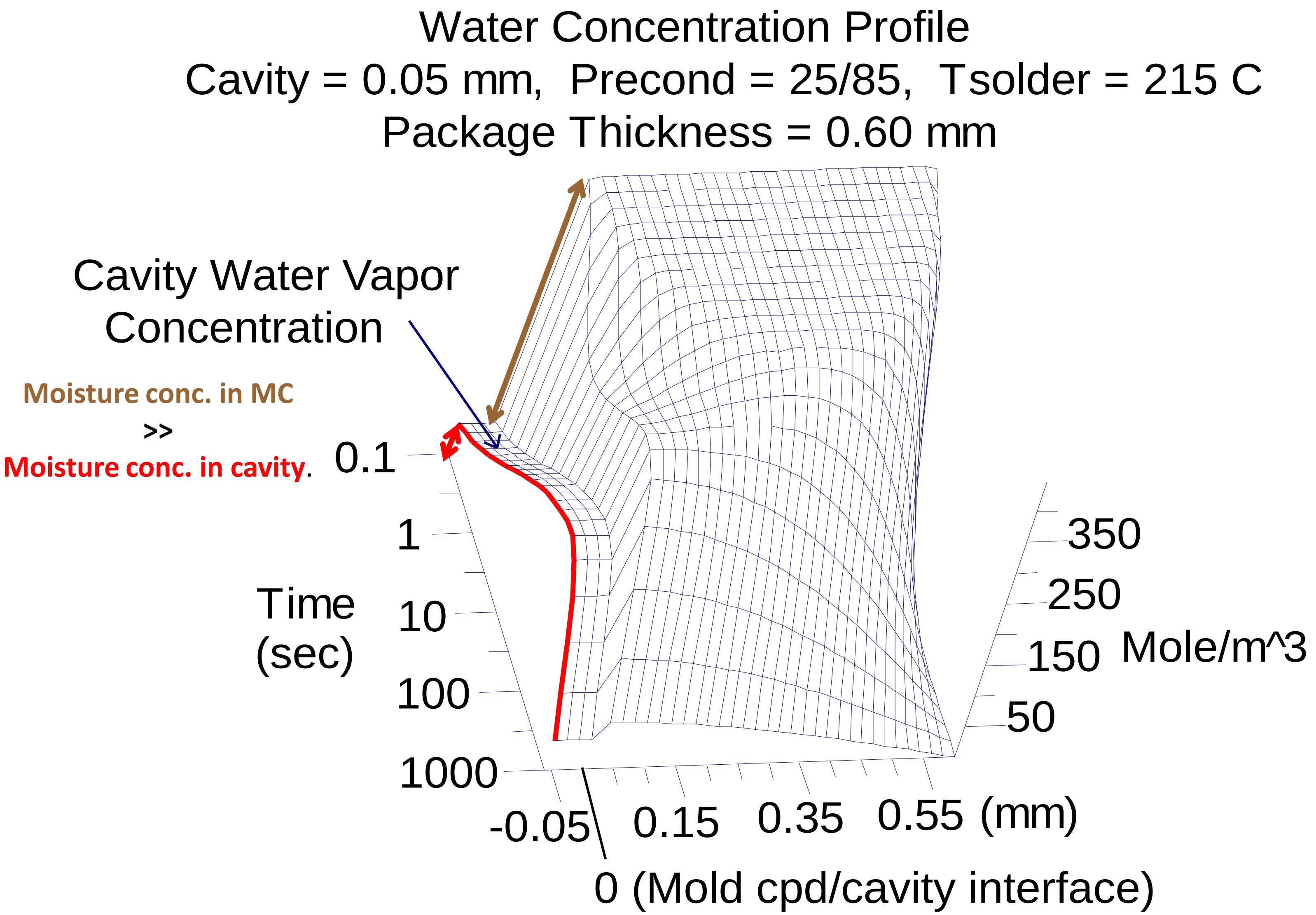
Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, in "Characterization of Integrated Circuit Packaging Materials", Butterwoth-Heinemann, 79-96, 1993.

Factors Affecting Popcorning

- Peak temperature reached during soldering.
- Moisture content of molding compound.
- Dimensions of die paddle.
- Thickness of molding compound under paddle.
- Adhesion of molding compound to die and/or lead frame.
- Mold compound formulation.

Not on this list: Pre-existing voids in the plastic package.

Popcorn Model, Internal Pressure



Popcorn Model, Internal Pressure

$$P_{\mathrm{cav}} \xrightarrow[l\to 0;\ w\to\infty\ (\text{or } t\to 0)]{} H_0 \times P_{\mathrm{sat}}(T_0) \times \frac{S(T_0)}{S(T_1)}$$

Delamination pressure exists even with no physical void.

Example:

- Unit preconditioned in 85/85 for a long time, then subjected to 215 C solder shock.
- Saturation coefficient has activation energy of 0.4 eV. (eg. Kitano et. al.)
- Steam table pressure at 85 C is 0.57 atm.

$$P_{\mathrm{cav}} = 0.85 \times 0.57 \times \exp\left\{ \frac{0.40\ \mathrm{eV}}{8.62\times 10^{-5}\ \ \mathrm{eV}/{}^\circ\mathrm{K}} \left(\frac{1}{273+85} - \frac{1}{273+215} \right) \right\}$$

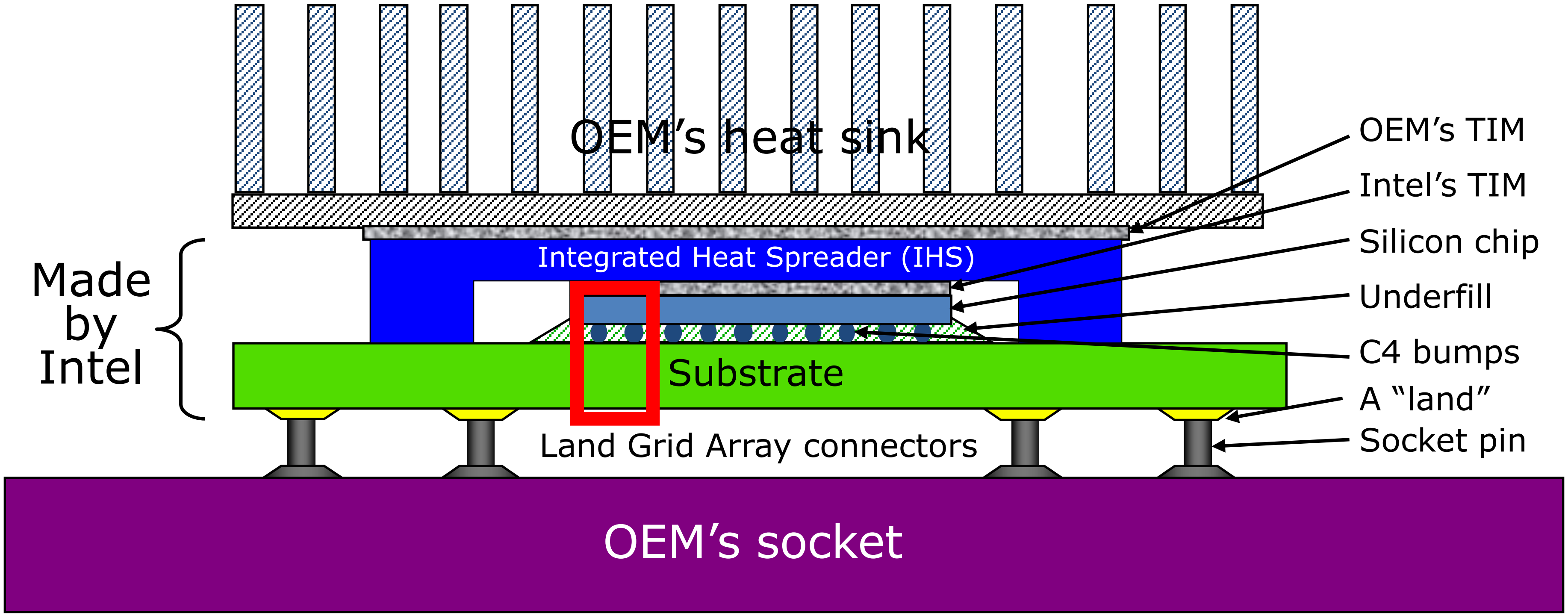
$$= 15.3\ \ \text{Atmospheres}$$

Wow!!

Outline

- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- ● Technology Update

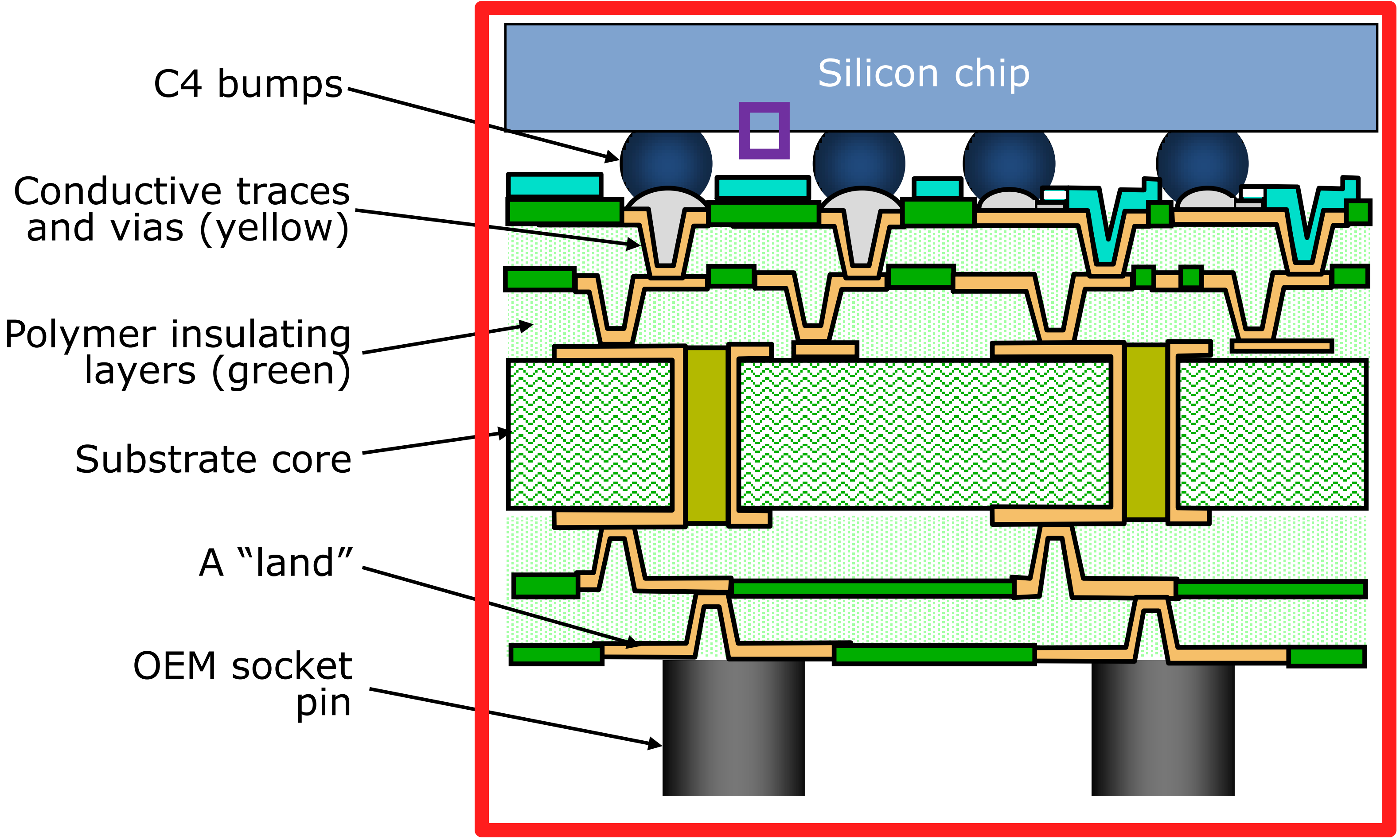
Package Anatomy



- This is an example of a packaged part as it might be used in a product

Slide: Scott C. Johnson

Package Anatomy

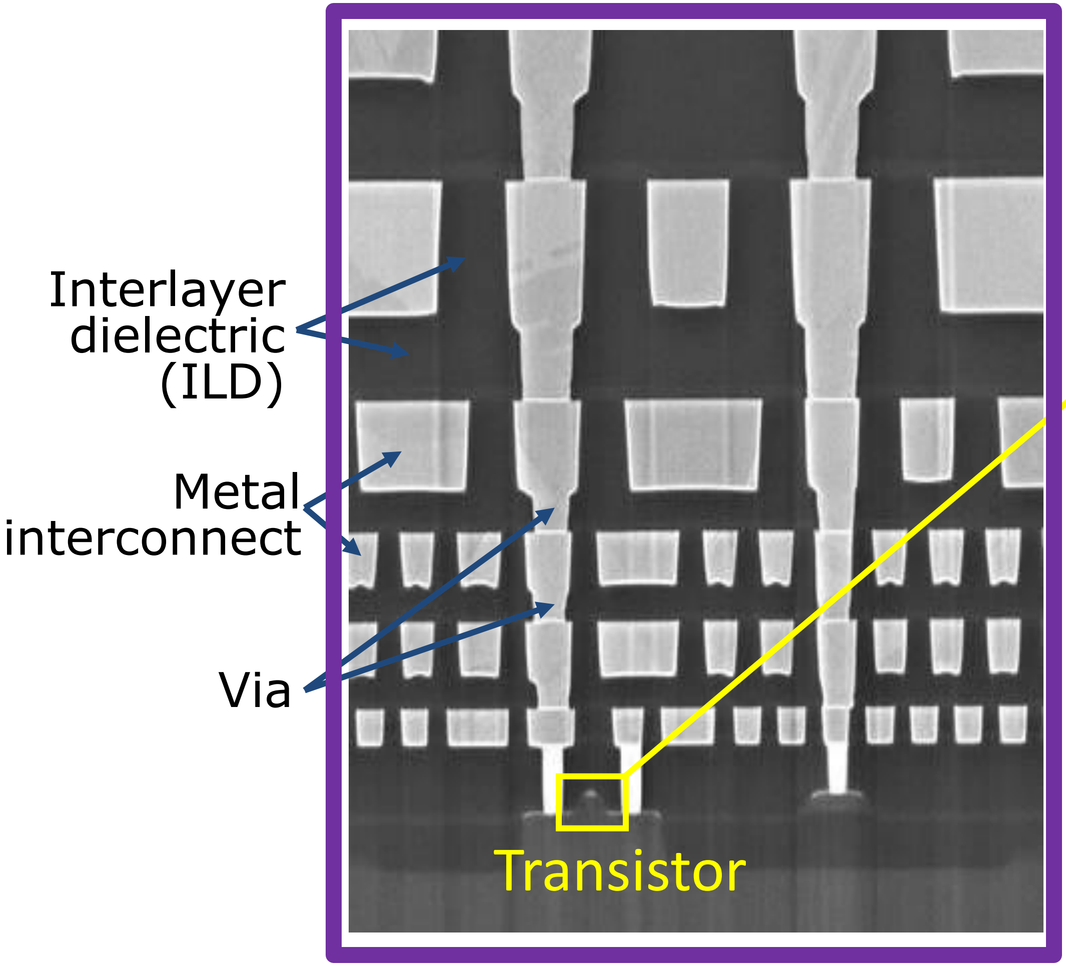


- This is a close-up of the package substrate showing the many layers of conductors and insulators

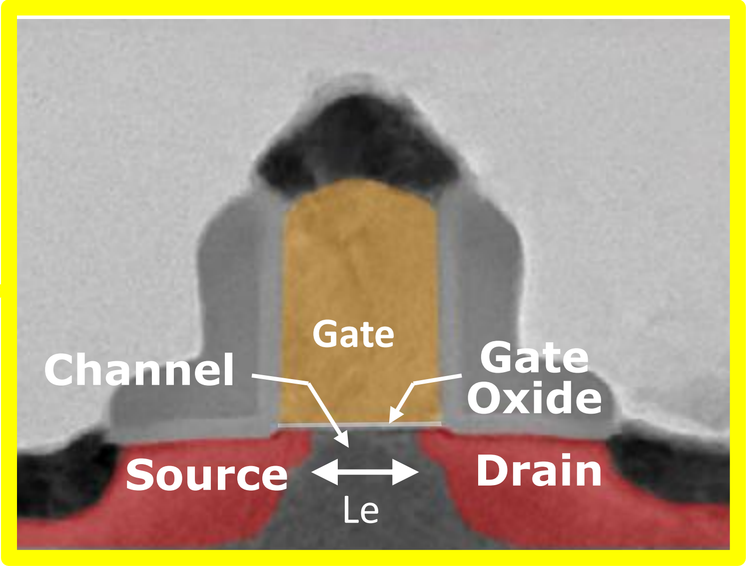
Slide: Scott C. Johnson

Location: Silicon (vs. Package)

“Back end” = interconnects



“Front end” = transistors



Slide: Scott C. Johnson