ECE 510, Lecture 10
Plastic Package Reliability, and Qualification Methodology

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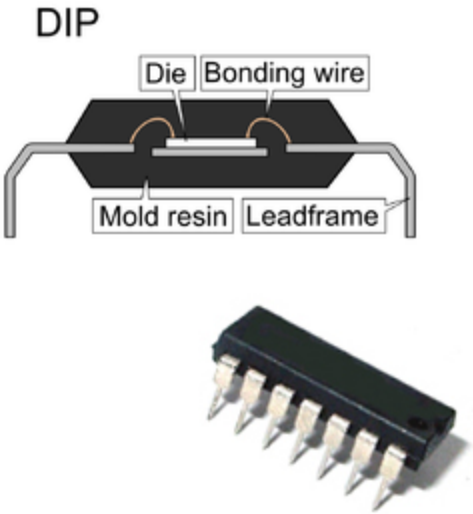
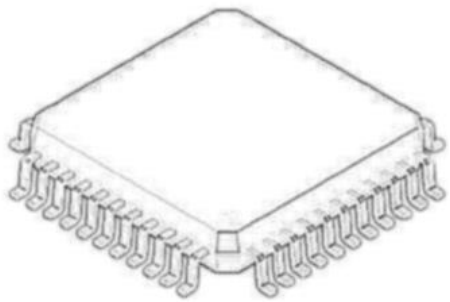
Outline

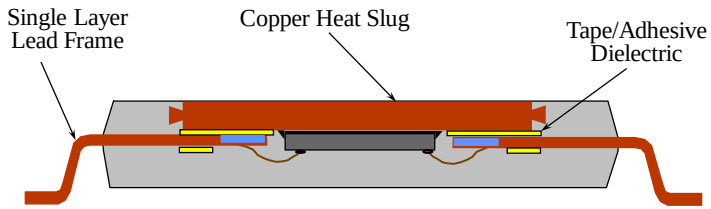
- Plastic Packages
- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- Technology Update

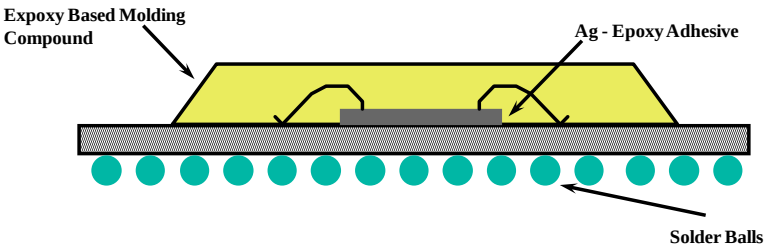
Plastic-Encapsulated Microcircuits

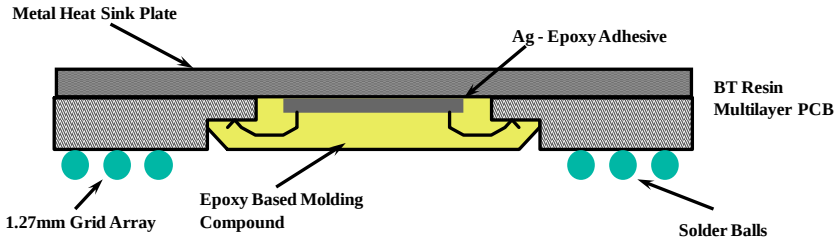
- The course covers plastic-encapsulated microcircuits.
- Molding compound (MC) in PEMs comes in direct contact with the die and chip connections.











Plastic-Encapsulated Microcircuits

- Die is mounted on a lead frame (A42 or Cu).
- Bonds are made by.
  - Wirebond: Au or Al; mostly Au.
  - TAB: Tape-Automated Bonding.
  - C4: Controlled Collapse Chip Connect.
- Assembly is encapsulated in molding compound.
  - Molding compound is in direct contact with die, wire bonds, etc.
- External leads are trimmed and solder plated.

<u>Alloy 42</u>
Fe 58% Ni 42% alloy
with CTE matching Si.

Molding Compounds

- MC is thermoset (curing) epoxy, typically novolac.
  - Cures at ~ 170-180°C.
  - Silica "filler" controls CTE and increases thermal conductivity.
  - MCs are (now) free of ionic contaminants.
- Glass Transition ~ 140°C.
- Moisture properties of MC:
  - Permeable to moisture.
  - Absorbs moisture. "Hygroscopic."

Note distinction between thermo*set* and thermo*plastic*.

Molding Compound Properties

- At the glass transition (> 140 °C)..

MC strength decreases

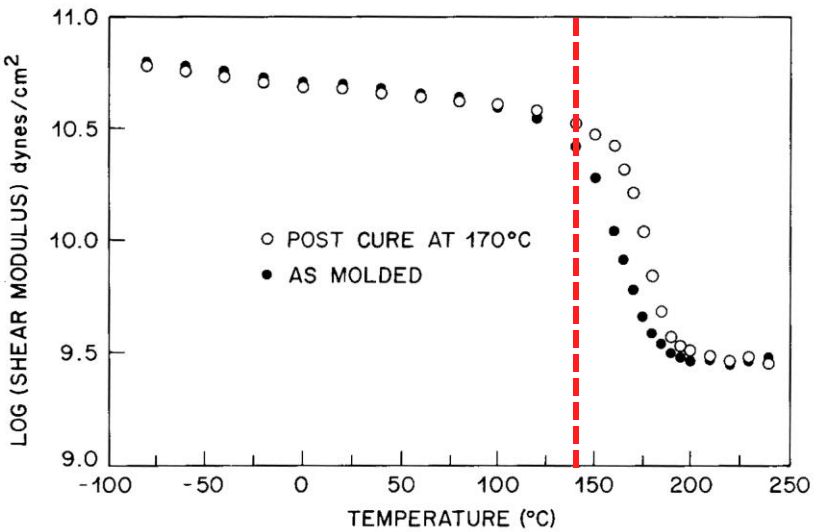


FIGURE 4-16 Shear modulus versus temperature data for an epoxy molding compound. Data show the effect of postcure on the thermomechanical properties. Frequency is 1 rad/sec.

CTE increases

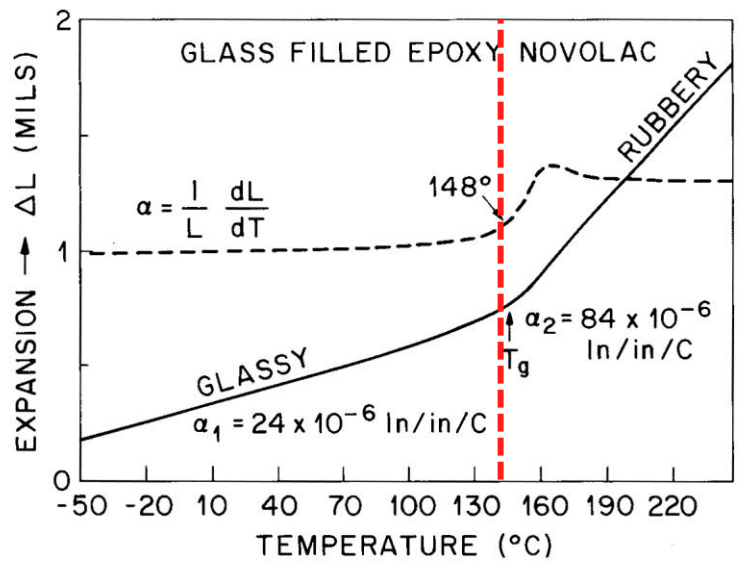


FIGURE 4-1 A plot of expansion versus temperature for an epoxy molding compound. The dashed line is the temperature derivative of expansion, which is defined as the coefficient of thermal expansion. Note the higher CTE above the glass transition temperature.

L. T. Manzione "Plastic Packaging of Microelectronic Devices," Van Nostrand Reinhold 1990.

Molding Compound Properties, ct'd

- Molding compound strongly absorbs water.
  - *Saturation* uptake is proportional to RH, and *independent of temperature.*
  - *Rate* of uptake *depends strongly on temperature*.

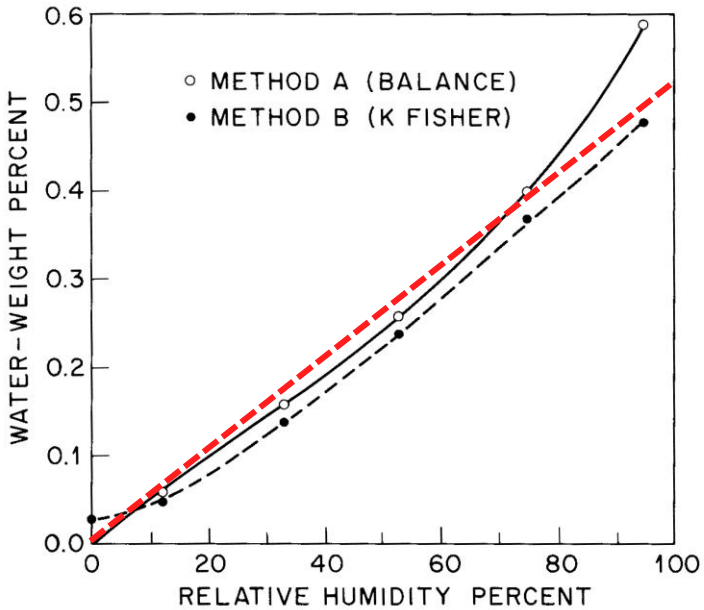


FIGURE 4-24 Plot of water uptake of epoxy molding compound preforms as a function of relative humidity of the conditioning atmosphere after three weeks of exposure at room temperature. K. Fisher is a hydrolysis technique for measuring water content. (Data of D. J. Boyle, J. T. Ryan and H. E. Bair, AT&T Bell Laboratories.)

L. T. Manzione "Plastic Packaging of Microelectronic Devices," Van Nostrand Reinhold 1990.

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- Stress and Test Flows
- Thermal Mechanisms
- Moisture Mechanisms
- Thermo-mechanical Mechanisms
- Moisture-mechanical Mechanisms
- Technology Update

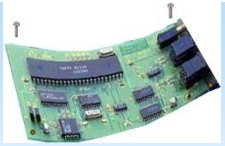
Life of an Integrated Circuit

Assembly → **Shipping** → **Storage** → **OEM/ODM Assembly** → **End-user Environment**

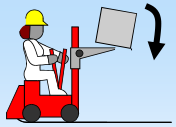
Desktop

Shipping Shock

Temperature Cycle

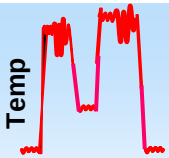


Bend Reflow



Handling

Temp, RH



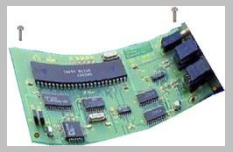
Power Cycle

Bent Pins, Singulation

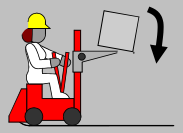
Mobile PC

Shipping Shock

Temperature Cycle



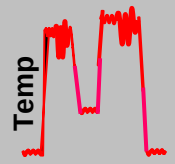
Bend Reflow



Handling

Temp, RH

User Drop & Vibe

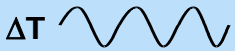


Power Cycle

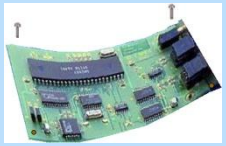
Bent Pins, Singulation

Handheld

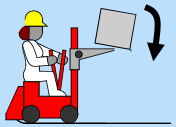
Shipping Shock



Temperature Cycle



Bend Reflow



Handling

Temp, RH

User Drop & Vibe

Keypad press

Slide by Scott C. Johnson.

Stress/Test Flow

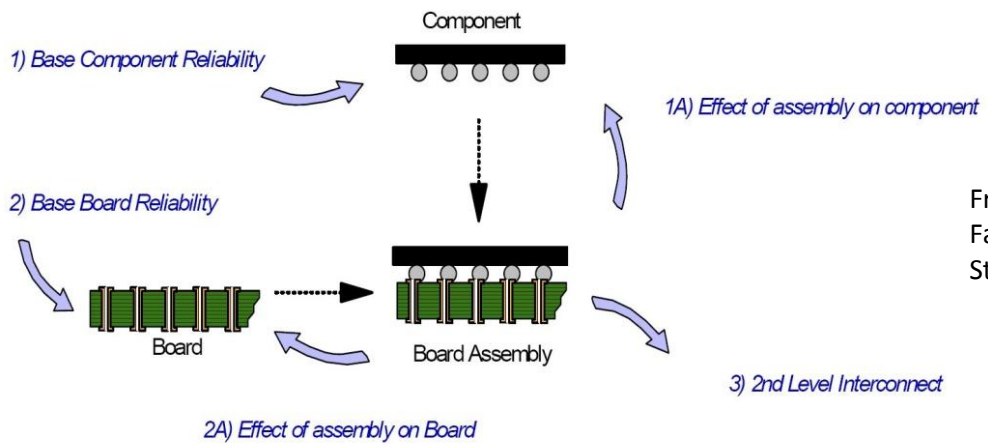


Figure 1 — Levels of Assembly - Interaction of packaging technical concerns

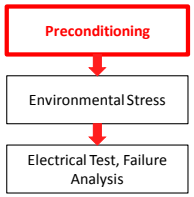
From: **JEP150** "Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components" (JEDEC)

Preconditioning	Simulate shipping, storing, and OEM board mounting process.
↓	
Environmental Stress	Simulate in-service end use conditions.
↓	
Electrical Test, Failure Analysis	Determine pass/fail. Diagnose failures.

Industry Reliability Standards

- International
  - ISO International Standard Organization
  - IEC International Electrotechnical Commission
- Europe
  - CEN, CENELEC Comite Européen de Normalisation Électrotechnique
- Japan
  - JIS Japanese Industrial Standard, EIAJ
- US
  - MIL (US Department of Defense), **EIA/JEDEC**

For US commercial products JEDEC standards have mostly superseded MIL standards.



Preconditioning

- Preconditioning simulates board assembly.
- Specified by
  - **JESD22-A113F** Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing.
  - IPC/JEDEC **J-STD-020D.01** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

http://www.jedec.org/

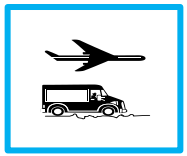
Free downloads, registration required.

Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Preconditioning Flow



JESD22-A113F

Annex A Typical Preconditioning Sequence Flow

Step	Item	Details	Section
1	Initial Electrical Test	- Replace any failing devices - Optional for testing by Supplier	4.1
2	Visual Inspection	- Replace any failing devices - Optional for testing by Supplier	4.2
3	Temperature Cycling	- 5 cycles -40 °C to 60 °C - Optional shipping simulation based on product requirements	4.3
4	Bake	- 24 h at 125 °C - Optional for testing by Supplier	4.4
5	Moisture Soak	- Soak time and conditions per IPC/JEDEC J-STD-020 based on device MSL level	4.5
6	Reflow	- 3 reflow cycles using profiles per IPC/JEDEC J-STD-020, document rev of J-STD-020 used - SnPb or Pb-free profile based on device end use process	4.6
7	Flux Application	- 10 s full immersion dip in activated water soluble flux - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.7
8	Cleaning	- DI water rinse - Remove all flux residual - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.8
9	Drying	- Room ambient drying - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.9
10	Final Electrical Test	- **If all devices pass then ready for Reliability Testing** - If valid failures are found then devices may have been tested to the wrong MSL level or something is substandard with the devices - Optional for testing by Supplier	4.10

Slide 50

IPC/JEDEC J-STD-020D.01

Table 5-1 Moisture Sensitivity Levels

LEVEL	FLOOR LIFE TIME	FLOOR LIFE CONDITION	SOAK REQUIREMENTS STANDARD TIME (hours)	STANDARD CONDITION	ACCELERATED EQUIVALENT[1] eV 0.40-0.48 TIME (hours)	eV 0.30-0.39 TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

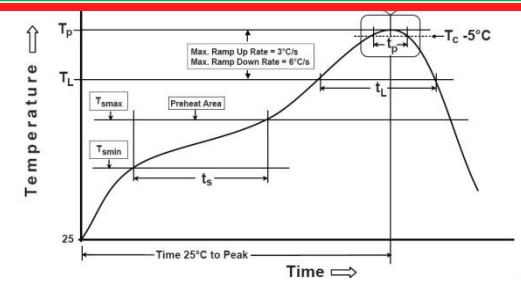
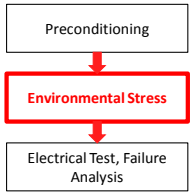


Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

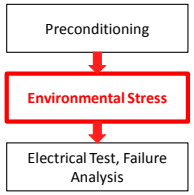
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.



Environmental Test

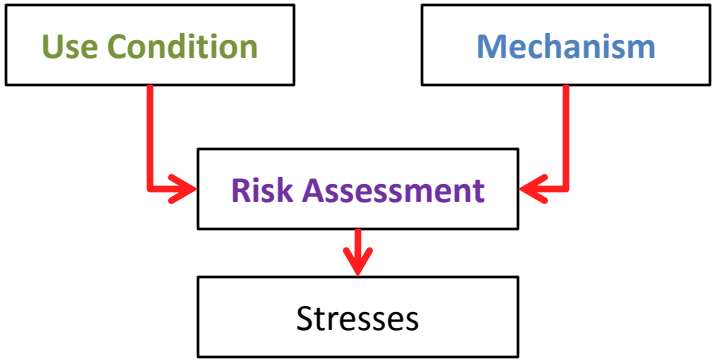
- Stress-based testing (traditional).
  - Standards: **JESD47**, MIL-STD-883.
  - Pro:
    - Well-established standards. Lots of historical data. Good for comparisons.
    - Little information about mechanism or use is required.
  - Con:
    - Overstress: May foreclose a technology.
    - Understress: Misses a mechanism.
      - May not accurately reflect a use environment.
- Knowledge-based testing.
  - Risk assessment of Use and Mechanism guides test.

To keep things simple, we'll follow this approach.



Knowledge-Based Test

- Knowledge-Based Testing
  - Stress depends on knowledge of **use conditions** and **mechanisms**.
  - **Risk assessment**, using methods
    - JEDEC: **JESD94**, **JEP143**, **JEP148**
    - **Sematech**: "Understanding and Developing Knowledge-based Qualifications of Silicon Devices" **#04024492A-TR**
  - Pro:
    - Stresses fit the product and its use. May make a product feasible.
  - Con:
    - Easy to miss mechanisms in new technologies and overlook use conditions in new applications.
    - Tempting to misapply to "uprate" devices, relax requirements.



Preconditioning
↓
Environmental Stress
↓
Electrical Test, Failure Analysis

JESD47 Example

5.5 Device qualification requirements

Table 1 — Device qualification tests

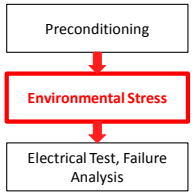
Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	Tj ≥ 125 °C Vcc ≥ Vccmax	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	Tj ≥ 125 °C Vcc ≥ Vccmax	See ELFR Table	48 ≤ t ≤ 168 hrs
Low Temperature Operating Life	JESD22-A108	LTOL	Tj ≤ 50 °C Vcc ≥ Vccmax	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	Ta ≥ 150 °C	3 Lots / 25 units	1000 hrs / 0 Fail
Non-Volatile Memory Cycling Endurance	JESD22-A117	NVCE	25 °C and 85°C ≥Tj ≥ 55 °C	3 Lots / 77 units	Up to Spec. Max Cycles per note (e) / 0 Fails
Data Retention for Non-Volatile Memory: High Temperature	JESD22-A117	HTDR	Option 1: Tj = 100 °C	3 Lots / 39 units	Cycles per NVCE (≥55 °C) / 96 and 1000 hrs / 0 Fail / note (f)
			Option 2: Tj ≥ 125 °C		Cycles per NVCE (≥55 °C) / 10 and 100 hrs / 0 Fail / note (f)
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A117	LTDR	Ta = 25 °C	3 Lots / 38 units	Cycles per NVCE (25 °C) / 500 hrs / 0 Fail / note (g)
Latch-Up	JESD78	LU	Class I or Class II	1 Lot / 3 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	Ta per datasheet
Human Body Model ESD	JS-001	ESD-HBM	Ta = 25 °C	3 units	Classification
Charged Device Model ESD	JESD22-C101	ESD-CDM	Ta = 25 °C	3 units	Classification
Accelerated Soft Error Testing	JESD89-2, JESD89-3	ASER	Ta = 25 °C	3 units	Classification
"OR" System Soft Error Testing	JESD89-1	SSER	Ta = 25 °C	Minimum of 1E+06 Device Hrs or 10 fails.	Classification

5.6 Nonhermetic package qualification test requirements

Table 2 — Qualification tests for components in nonhermetic packages

Stress	Ref.	Abbv	Conditions	Requirements	
				# Lots / SS per lot	Duration /Accept
MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 -A113	PC	Per appropriate MSL level per J-STD-020		Electrical Test (optional)
High Temperature Storage[1]	JESD22 -A103 & A113	HTSL	150 °C + Preconditioning if Required	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature[2] Humidity bias (standard 85/85)	JESD22 -A101	THB	85 °C, 85 % RH, Vccmax	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature[2,3] Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22 -A110	HAST	130 °C / 110 °C, 85 % RH, Vccmax	3 Lots / 25 units	96/264 hours or equivalent per package construction / 0 Fail
Temperature Cycling	JESD22 -A104	TC	B[4] -55 °C to +125 °C	3 Lots / 25 units	700 cycles / 0 Fail
			G[4] -40 °C to +125 °C		850 cycles / 0 Fail
			C[4] -65 °C to +150 °C		500 cycles / 0 Fail
			K[4] 0 °C to +125 °C		1500 cycles / 0 Fail
			J[4] 0 °C to +100 °C		2300 cycles / 0 Fail
Unbiased Temperature/Humidity (Unbiased HAST[3])	JESD22 -A118	UHAST	130 °C / 85% RH 110 °C / 85% RH	3 Lots / 25 units	96 hrs / 0 Fail 264 hrs / 0 Fail
Unbiased Temperature/Humidity (Autoclave[5])	JESD22 -A102	AC	121 °C / 100% RH	3 Lots / 25 units	96 hrs / 0 Fail **Not Recommended**
Solder Ball Shear	JESD22 -B117	SBS	Characterization	30 balls / 5 units	
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Bond Shear	JESD22 -B116	BS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Solderability	M2003 JESD22 -B102	SD	Characterization	3 lots / 22 leads	0 Fail
Tin Whisker Acceptance	JESD22 -A121 through rqmts of JESD 201	WSR	Characterization per JESD201	See JESD 201	See JESD201, Based on Appropriate Classification

Note: TS (**JESD22-A106**) and AC (Steam) (**JESD22-A102**) are not recommended. *Very* different from use.



Example Stress Flow

ELFR

Early life failure rate.
168 hrs
JESD22-A108

<u>Assumptions</u>
168 h is equivalent to early life requirement
SS computed from goal. eg. **3x611 = 1833**

This lecture.

PC

Preconditioning.
JESD22-A113

(Lots x Units)

3 x 77

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

3 x 25

HTSL (Bake)

1000 hrs
JESD22-A103

3 x 25

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

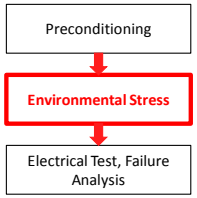
3 x 25

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Sampling

- **JESD47** sample requirements are minimal.
  - Single "snapshot" is a crude validation of the reliability of the product.
  - Small SS does not generate failures to give clues to process weaknesses.
- Risks.
  - Qualification hinges on single failures.
    - Moral hazard to "invalidate" a failure is high.
  - Lot-to-lot variation, excursions.
    - Incoming materials, fab lots, assembly lots, test lots.



Sampling, ct'd

- Number of lots covers risks of machine-to machine, day-to-day, etc. variation.
- Often minimum SS to validate a goal is chosen.
  - Pro: Saves $, and there are no failures to explain.
  - Con: Pass/fail of the qual is at the mercy of a single failure.
    - Verrry tempting to invalidate a failure.
  - Con: No mechanism learning.

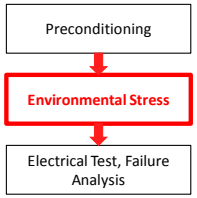
(Accept/Reject $\Rightarrow$ 0/1)

- eg. To validate 500 DPM at ELFR using minimum SS at 60% confidence, 1833 units are required.
  - 500 DPM is a typical goal (see ITRS)

$$SS = \frac{-\ln(1-cl)}{D}$$

Useful "mental furniture"

$$1833 = \frac{-\ln(1-0.6)}{500 \times 10^{-6}}$$



Sampling, ct'd

- For environmental stress, 3x77 is a typical SS, why?

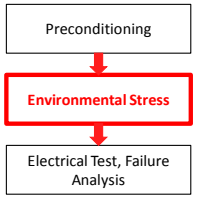
$$\text{Fail Fraction UCL} = \frac{-\ln(1-cl)}{3\times 77}; \quad \frac{-\ln(1-0.9)}{231} = \frac{-\ln(.1)}{231} = \frac{2.3026}{231} = 1\%$$

  – So, 0/1 accept/reject validates, to 90% confidence, a failure rate less than 1% at the accelerated condition.

- If the stress corresponds to the lifetime (eg. 7 years) then the average failure rate is

$$FR = \frac{1\times 10^{-2}}{7\times 365\times 24}\times 10^{9} = 163 \;\; Fits$$

  – This falls into the range of ITRS wearout goals.



Reliability Goals from ITRS 2009

http://www.itrs.net/reports.html

Table PIDS6 Reliability Technology Requirements

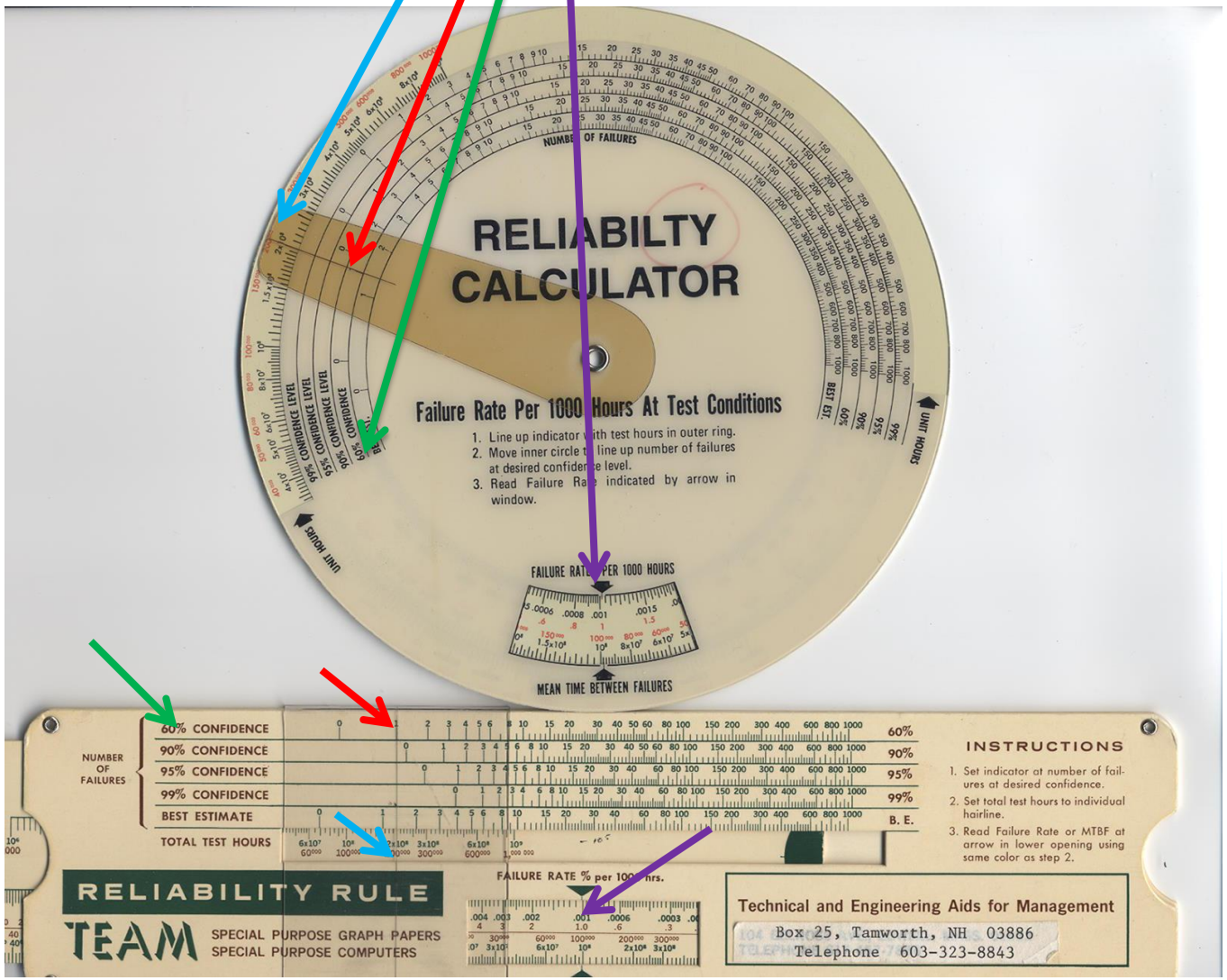
Year of Production	*2009*	*2010*	*2011*	*2012*
DRAM 1/2 Pitch (nm) (contacted)	*52*	*45*	*40*	*36*
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)	*54*	*45*	*38*	*32*
MPU Physical Gate Length (nm)	*27*	*24*	*22*	*20*
Early failures (ppm) (First 4000 operating hours) [1]	2–2000	2–2000	2–2000	2–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	1-1000	1-1000	1-1000	1-1000
SRAM Soft error rate (FITs/MBit) [3]	11,000	11,000	11,000	11,000
Relative failure rate per transistor (normalized to 2009 value) [4]	1.000	0.71	0.50	0.35
Relative failure rate per meter of interconnect (normalized to 2009 value) [5]	1.00	0.50	0.50	0.25

Infant Mortality

Wear-out

Constant fail rate

Reliability Calculator		Fail Fraction Calculator	
Confidence (%)	60	Confidence (%)	60
Number of Failures	1	Number of Failures	1
Device Hours	200	Number of Units	200
FR (%/h)	1.01	Fail %	1.01
FR (%/kh)	10111.16	DPM	10111.57
FITs	10111566.23		



Excel Reliability Calculator

- Handy tool for quick calculations.
- Has user-functions "binomial upper/lower confidence limits (one-sided)" that can be used in a worksheet.
- Doubles as a failure rate calculator if the sample size is taken as device hours.
  - Used for calculating average failure rates (AFR).
- Failure rates are computed assuming constant failure rate. FR = # Fails ÷ Device Hours.

Best Estimate AFR

- A "best estimate" defined in TT is

$$AFR_{BE} = \frac{\text{Number of Failures}}{\text{Device Hours}}$$

$$\text{Device Hours} = \text{Hours of Stress} \times \text{Number of Devices}$$

- Reliability Ruler Best Estimate
  - Because of the difficulty with zero failures, the reliability ruler uses the 50% one-sided UCL as the best estimate.
  - BUCL1(Number of Failures, Device Hours, 0.5)
- There are uses for either way of specifying "BE".
  - Neither is "wrong".

Homework 10

- Use “Rel Ruler” to answer the following 3 questions.
  - Type and explain answers on a copy of the rel ruler tool and send in the tool.

1. The goal for 1000 h of 85/85 testing is 1% or less.
   - What is the minimum sample size to validate the goal at 90% confidence?
   - What is the accept on 1, fail on 2 SS at 90% confidence?
2. The goal for ELFR is AFR < 1000 FITs in the first year.
   - What is the minimum sample size to validate the goal at 90% confidence?
   - What is the accept on 1, fail on 2 SS at 90% confidence?

Homework 10, ctd.

3. 100 units are stressed for 1000 hours, failures occur at 100 hours, 400 hours, 700 hours. (An example of “time-censored” data, or “Type I censoring”.)
   - Compute the following estimates of the average failure rate: BE(TT), BE(50% UCL), 60% UCL, 90% UCL

Example Data

- Additional attributes enhance value of data.
  - Device type
  - Date code
  - Package type
  - Readouts
  - Failure analysis

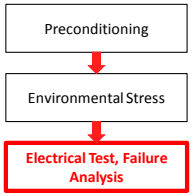
[Maxim product reliability report RR-1H]

TABLE 11. TEMPERATURE AND HUMIDITY (85/85) TEST RESULTS

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS.) 192	500	1000	NOTE
MAX232	9032	16 PDIP	45	0	0	0	
MAX690	9032	8 PDIP	69	0	0	0	
ICL7109	9033	40 PDIP	75	0	0	0	
MAX690	9033	8 PDIP	77	0	0	0	
MAX232	9033	16 PDIP	60	0	0	1	OXIDE DEFECT
MAX691	9033	16 PDIP	70	0	0	0	
OP290	9034	8 PDIP	24	0	0	0	
MAX172	9035	24 PDIP	35	0	0	0	
MAX232	9036	16 PDIP	45	0	0	1	OXIDE DEFECT
MAX232	9036	16 WSO	45	0	0	0	
MAX690	9041	8 PDIP	39	0	0	0	
MAX690	9043	8 PDIP	77	0	0	0	
MAX238	9043	24 PDIP	72	0	0	0	
ICM7212	9043	40 PDIP	77	0	0	0	
MAX154	9044	24 PDIP	69	0	0	0	
MAX232	9045	16 PDIP	44	0	0	0	
MAX232	9046	16 PDIP	44	0	0	0	
REF02	9049	8 PDIP	76	0	0	0	
MAX400	9049	8 PDIP	76	0	0	0	
MAX400	9049	8 PDIP	76	0	0	0	
ICL7664	9049	8 PDIP	76	0	0	0	
MX7541	9050	18 PDIP	72	0	0	0	
DG212	9052	16 PDIP	76	0	0	1	MARG. LEAKAGE
DG211	9052	16 NSO	45	0	0	0	
MAX7231	9105	40 PDIP	80	0	0	0	
MX7245	9106	24 PDIP	45	0	0	0	
MX7824	9106	24 PDIP	58	0	0	0	
DG211	9108	16 NSO	45	0	0	0	
MX7845	9108	24 PDIP	68	0	0	0	
MAX8211	9108	8 SO	77	0	0	0	
MAX8211	9108	8 SO	77	0	2	1	2 DIE SCRATCH, 1 SHORT
DG211	9109	16 NSO	45	0	0	0	
MAX231	9109	14 PDIP	80	0	0	0	
MAX275	9110	20 PDIP	41	0	0	0	
MAX732	9110	8 PDIP	77	0	0	0	
MAX232	9110	16 PDIP	80	0	0	0	
DG509	9112	16 PDIP	80	0	0	0	
MAX902	9112	14 PDIP	48	0	0	0	
ICM7212	9115	40 PDIP	45	0	0	0	
MX7845	9117	24 PDIP	58	0	0	0	
OP07	9118	8 PDIP	77	0	0	0	
MAX1000	9119	24 WSO	77	1	0	0	MARG. LEAKAGE
MAX730	9119	8 PDIP	76	0	0	0	
DG508	9122	16 PDIP	77	0	0	1	MARG. LEAKAGE
MX7582	9122	28 PDIP	45	0	0	0	
MAX232A	9123	16 PDIP	77	0	0	0	
ICL7106	9125	44 PLCC	30	0	0	0	
MAX292	9125	8 PDIP	77	0	0	0	
MAX232	9125	16 WSO	56	0	0	0	
OP07	9130	8 PDIP	77	0	0	1	MASKING DEFECT
MX7245	9133	24 PDIP	72	0	0	0	
MAX690	9138	8 PDIP	77	0	0	0	
MX7245	9138	24 PDIP	76	0	0	0	
DG211	9138	16 PDIP	77	0	0	1	MARG. LEAKAGE
MAX232	9140	16 WSO	75	0	0	0	
MAX730	9140	8 PDIP	77	0	1	0	PARAMETRIC
DG211	9141	16 PDIP	77	0	0	0	
DG411	9144	16 PDIP	77	0	1	1	2 MARG. LEAKAGE
DG413	9145	16 PDIP	77	0	0	0	
MAX690	9147	8 PDIP	100	0	0	0	
DG455	9149	16 PDIP	72	0	0	0	
OP07	9152	8 PDIP	77	0	0	0	
MAX232	9201	16 WSO	77	0	0	0	

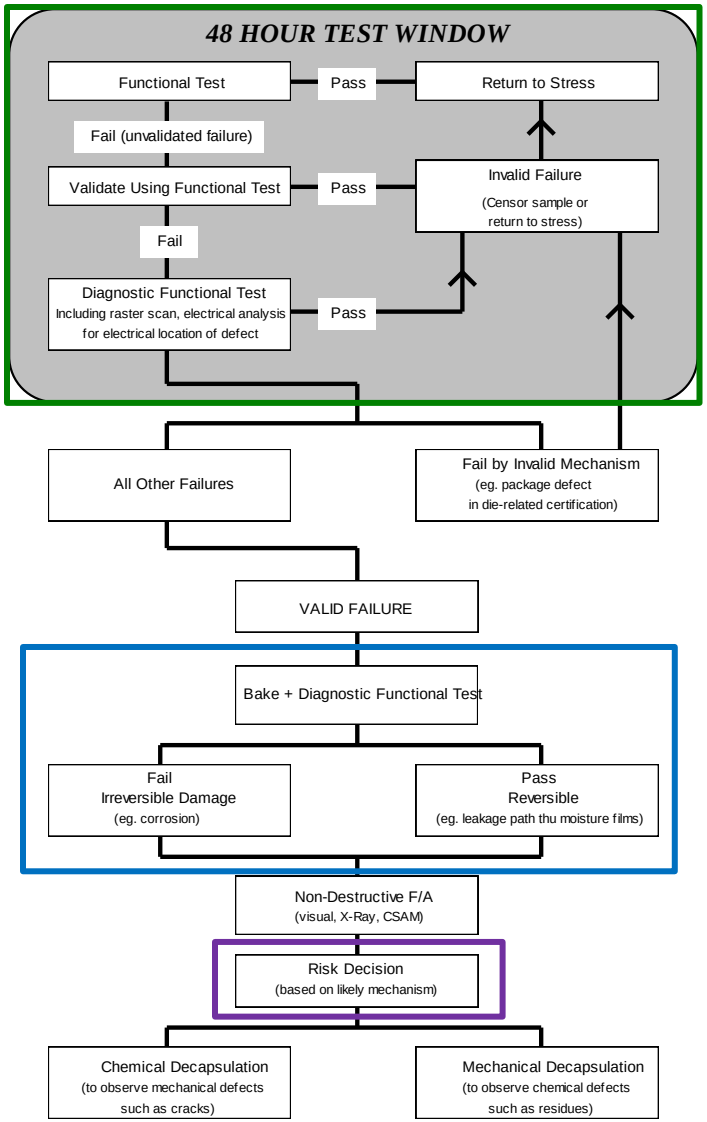
TABLE 11 *(continued)*

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS.) 192	500	1000	NOTE
MAX232	9203	16 PDIP	76	0	0	0	
MX7245	9202	24 PDIP	72	0	0	0	
REF01	9204	8 NSO	77	0	0	0	
MAX232	9206	16 PDIP	77	0	0	0	
MAX690	9206	8 PDIP	77	0	0	0	
ICL7109	9206	40 PDIP	77	0	0	0	
ICL7109	9207	40 PDIP	56	0	0	0	
MAX690	9207	8 PDIP	77	0	0	0	
ICL7106	9208	40 PDIP	28	0	0	0	
ICM7211	9208	40 PDIP	28	0	0	0	
ICL7109	9208	40 PDIP	56	0	0	0	
DG444	9210	16 PDIP	77	0	1	0	MARG. LEAKAGE
DG412	9210	16 PDIP	75	0	0	0	
MAX241	9211	28 SSOP	30	0	0	0	
DG211	9212	16 PDIP	77	0	1	0	MARG. LEAKAGE
MAX707	9212	8 PDIP	76	0	0	0	
MAX232	9214	16 WSO	56	0	0	0	
MAX232	9215	16 WSO	45	0	0	0	
MAX232	9215	16 PDIP	77	0	0	0	
MAX241	9220	28 SSOP	30	0	0	0	
MAX406	9221	8 PDIP	73	0	0	0	
MAX232	9221	16 PDIP	76	0	0	0	
MAX232	9222	16 WSO	56	0	0	0	
MAX626	9222	8 PDIP	76	0	0	0	
REF01	9224	8 PDIP	76	0	0	0	
MAX667	9226	8 PDIP	45	0	0	0	
MAX735	9227	8 PDIP	77	0	0	0	
MAX4420	9232	8 PDIP	77	0	0	0	
DG411	9234	16 PDIP	76	0	0	0	
MAX626	9235	8 PDIP	77	0	0	0	
DG211	9236	16 PDIP	77	0	1	0	MARG. LEAKAGE
MAX232	9237	16 PDIP	77	0	0	0	
MAX480	9237	8 PDIP	77	0	0	0	
MAX663	9238	8 NSO	77	0	1	0	FUNCTIONAL
MAX661	9238	8 PDIP	45	0	0	0	
MAX1074	9240	TO220	25	0	0	0	
DG411	9240	16 PDIP	77	0	0	0	
MX7524	9242	16 PDIP	77	0	0	0	
MAX623	9246	16 PDIP	36	0	0	0	
OP07	9246	8 PDIP	77	0	0	0	
MAX730	9248	8 PDIP	77	0	0	0	
LT1074	9248	TO220	25	0	1	0	PARAMETRIC
MAX232	9249	16 PDIP	77	0	0	1	OXIDE DEFECT
DG211	9249	16 PDIP	77	0	0	0	
MAX662	9249	8 PDIP	45	0	0	0	
MAX8212	9251	8 NSO	77	0	0	0	
MAX903	9252	8 NSO	77	0	0	0	
MAX412	9252	8 PDIP	36	0	0	0	
MAX8212	9301	8 NSO	77	0	0	0	
DG405	9302	16 PDIP	77	0	0	1	PARAMETRIC
MAX412	9302	8 PDIP	36	0	0	0	
MAX410	9302	8 PDIP	36	0	0	0	
MAX708	9303	8 PDIP	77	0	0	0	
MX7524	9306	16 PDIP	77	0	0	0	
REF02	9308	8 PDIP	77	0	1	0	PARAMETRIC
MAX662	9308	8 PDIP	45	0	0	0	
DG508	9309	16 PDIP	77	0	2	0	1 CORROSION; 1 MARG. LEAKAGE
MAX232	9311	16 PDIP	77	0	0	0	
MAX232	9314	16 WSO	45	0	0	0	
MAX8212	9314	8 NSO	77	0	0	0	
MAX232	9315	16 WSO	45	0	0	0	
MAX8212	9315	8 NSO	77	0	0	0	



Test and Failure Analysis

- Moisture-related tests (85/85, HAST, Steam) have specific test/FA reqt's.
  - Test must be done while unit contains moisture.
    - Within 48 hr.
  - Units must not be "wet".
    - Wet = liquid water.
- Diagnostic Bake.
- Risk decision before destructive analysis.



HAST versus 85/85

- Moisture MUST be non-condensing. (RH < 100%).
- Both require about < 1% fail. Typical SS ~ 100.
- 130/85 HAST duration is 10x less than 85/85 duration. We'll see how this was justified.
- 85/85 (**JESD22-A101**)

6 week bottleneck in information turns.

3.1 Temperature, Relative Humidity and Duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
85 ± 2	85 ± 5	81.0	7.12/49.1	1000(-24,+168)

- HAST (**JESD22-A110**)

3.1 Temperature, relative humidity and duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
130 ± 2	85 ± 5	124.7	33.3/230	96 (-0, +2)
110 ± 2	85 ± 5	105.2	17.7/122	264 (-0, +2)

10x less time

1 atm = 14.2 psi

$$\frac{33.3-14.2}{14.2} = 1.34 \text{ atmospheres} \Rightarrow \text{ Pressure vessel required.}$$

Example: Comparison of HAST Stds

Table 4-9 Reliability Test Standards Comparison Table

4/5

	Sony	EIAJ	IEC	JEDEC
Unsaturated Pressure Cooker Test	130±2℃ 85±5%RH 2.3×10^5 Pa • Continue and perform the soldering heat resistance test. • Voltage application (prescribed individually) • Test time: 200 h	EIAJ ED-4701-3 (1997) Test method B-123A • Condition selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa B 120±2℃, 85±5%RH, 1.7×10^5 Pa C 130±2℃, 85±5%RH, 2.3×10^5 Pa • Voltage application if prescribed • Test time prescribed individually	IEC 60749 (1996-10) CHAPTER 3 4C • Condition selection Severity selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa — 408h, 192h, 96h B 120±2℃, 85±5%RH, 1.7×10^5 Pa — 192h, 96h, 48h C 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96h, 48h, 24h • Voltage application if prescribed	JESD22-A110-B (1999) Highly-Accelerated Temperature and Humidity Stress Test (HAST) • Condition selection 110±2℃, 85±5%RH, 1.2×10^5 Pa — 264 $^{+2}_{-0}$ h 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96 $^{+2}_{-0}$ h • Power-on guidelines - Minimum power consumption - Apply to alternating pins as much as possible. - Apply a potential difference to the entire metal wiring. - Apply the maximum allowable voltage. - Continuous power-on when the thermal loss is 200 mW or less or when the die pad temperature rise is 10℃ or less. - Intermittent cycles at 50% duty (Power-on:Power-off = 1:1) - 1 cycle period t ≥ 2 mm: 2 h or less t < 2 mm: 30 minutes or less (t: package thickness) • The temperature and humidity until arrival at the test conditions are prescribed. • Measure within 48 h after placing in and removing from the chamber, and reapply stress within 96 h. The time provision is relaxed to 3 times for storage using bags to prevent the escape of humidity.

Intermittent Bias

Test and Failure Analysis Window

From Sony Quality and Reliability Handbook http://www.sony.net/Products/SC-HP/tec/catalog/qr.html

HAST System

- Large vessel (24” dia) requires forced convection.

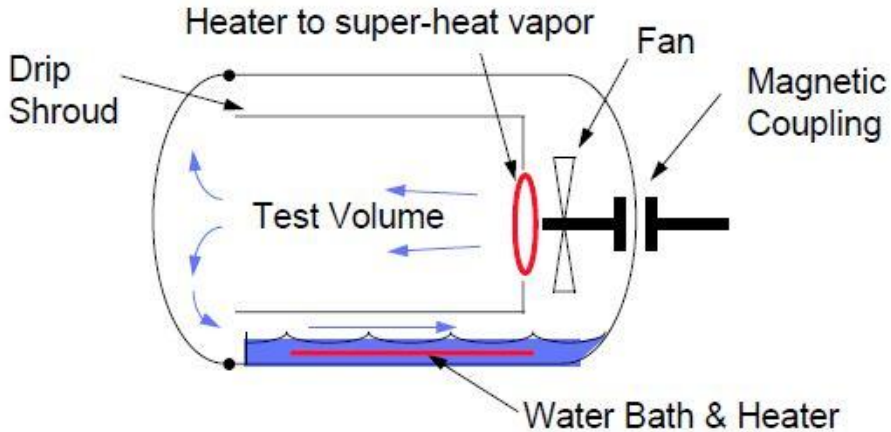
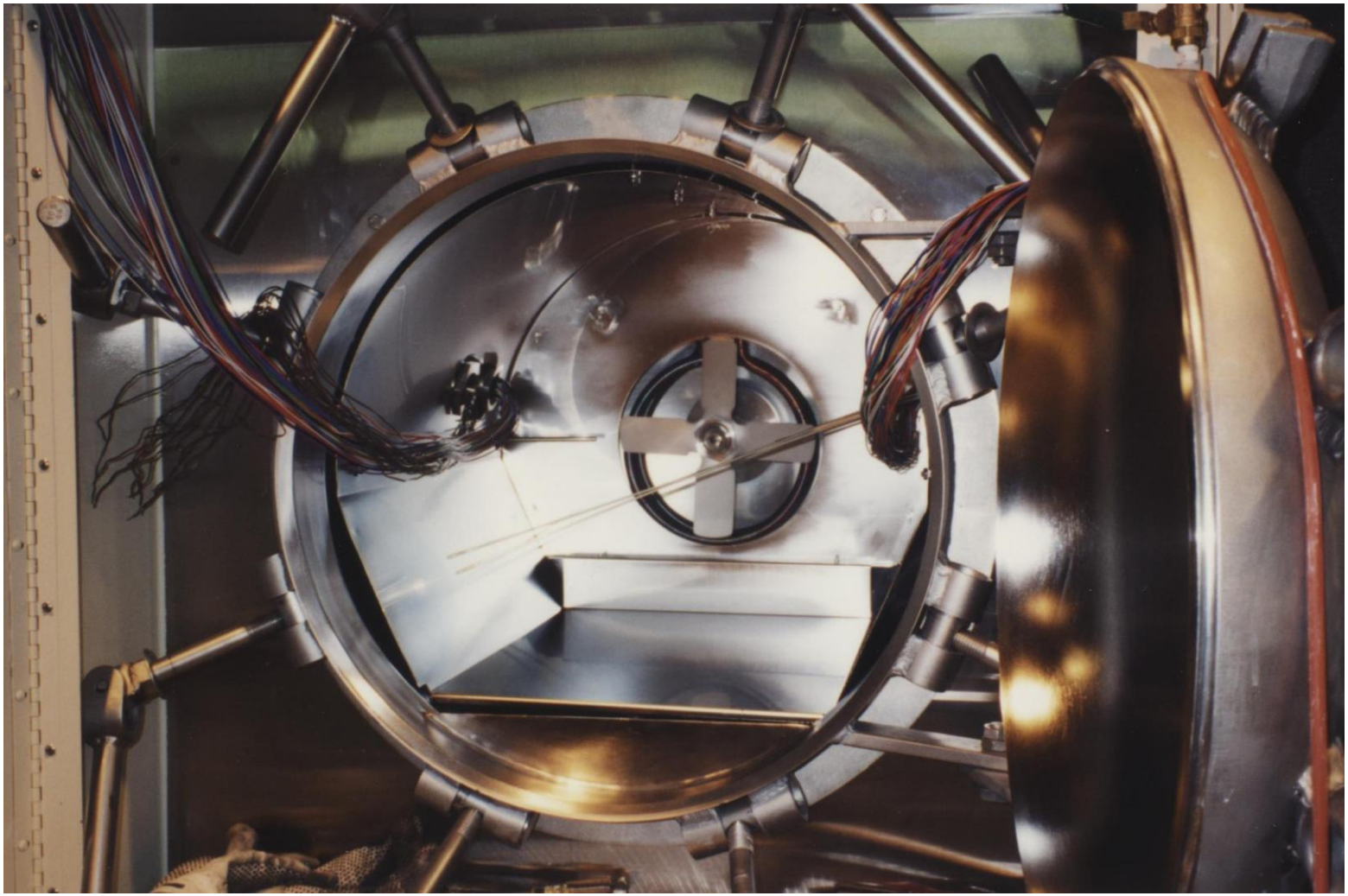


Fig. 3 The NG HAST chamber operates on the principle of forced convection. This ensures efficient mixing, minimizing temperature gradients across the test volume. Reliability of the fan drive is ensured by a proven design of magnetic coupling feed through.

C. G. Shirley, “A New Generation HAST System”, Non-proprietary Report to Intel, Despatch Industries, and Micro-Instrument Corp. describing learnings during development of NG HAST. December, 1994.

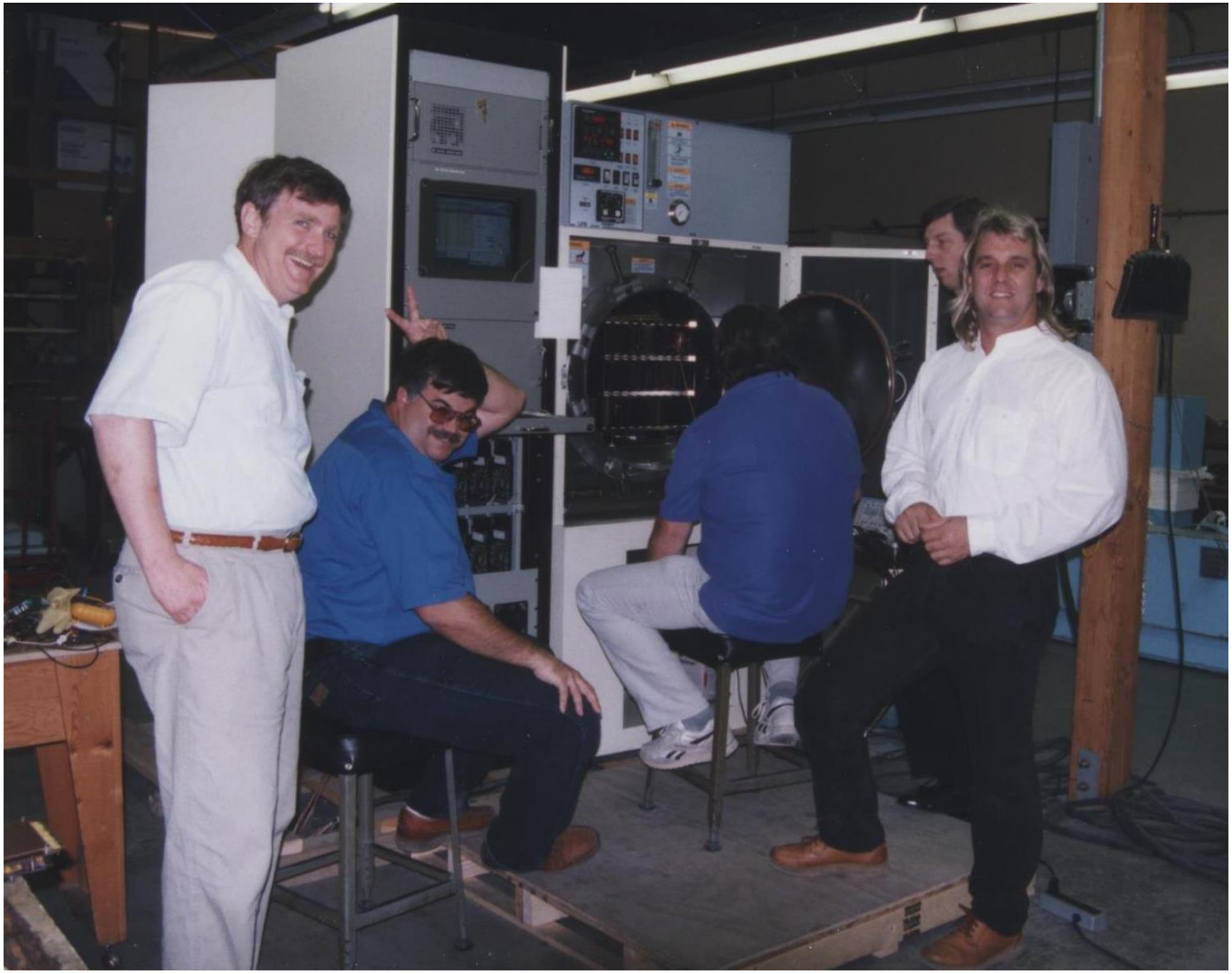
HAST System



HAST System


WARNING
HIGH VOLTAGE
LPB series
WARNING
HIGH TEMPERATURES MAY BE PRESENT INSIDE. DO NOT TOUCH HOT SURFACES.

HAST Development Team



HAST Ramp Up Requirements

- Ramp Up: Avoid condensation on load.

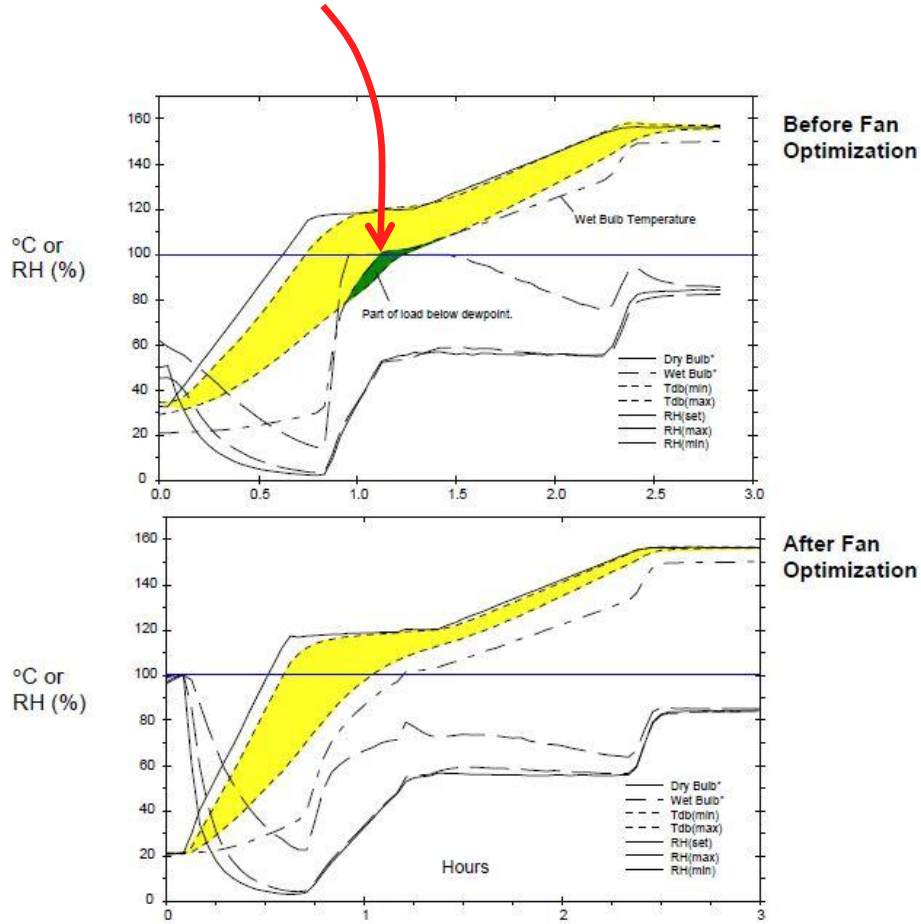
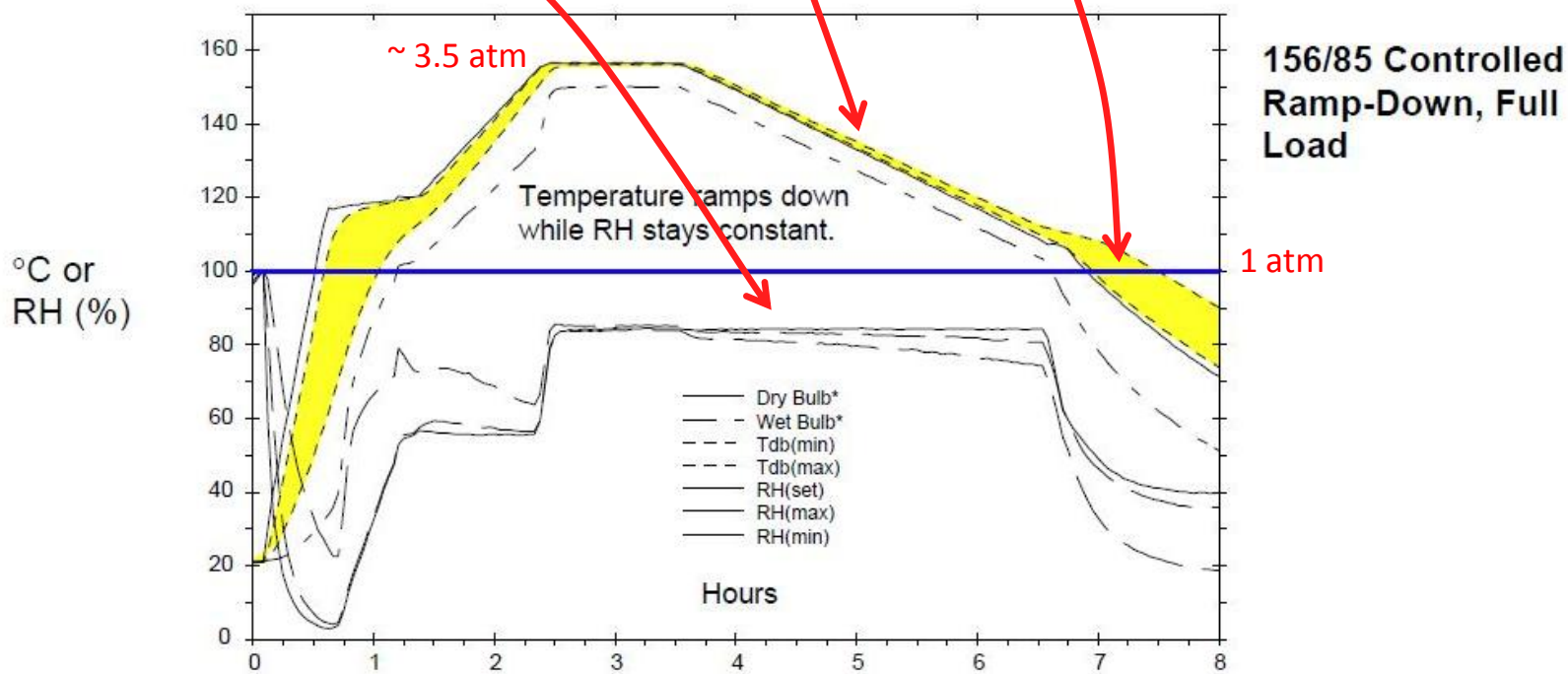


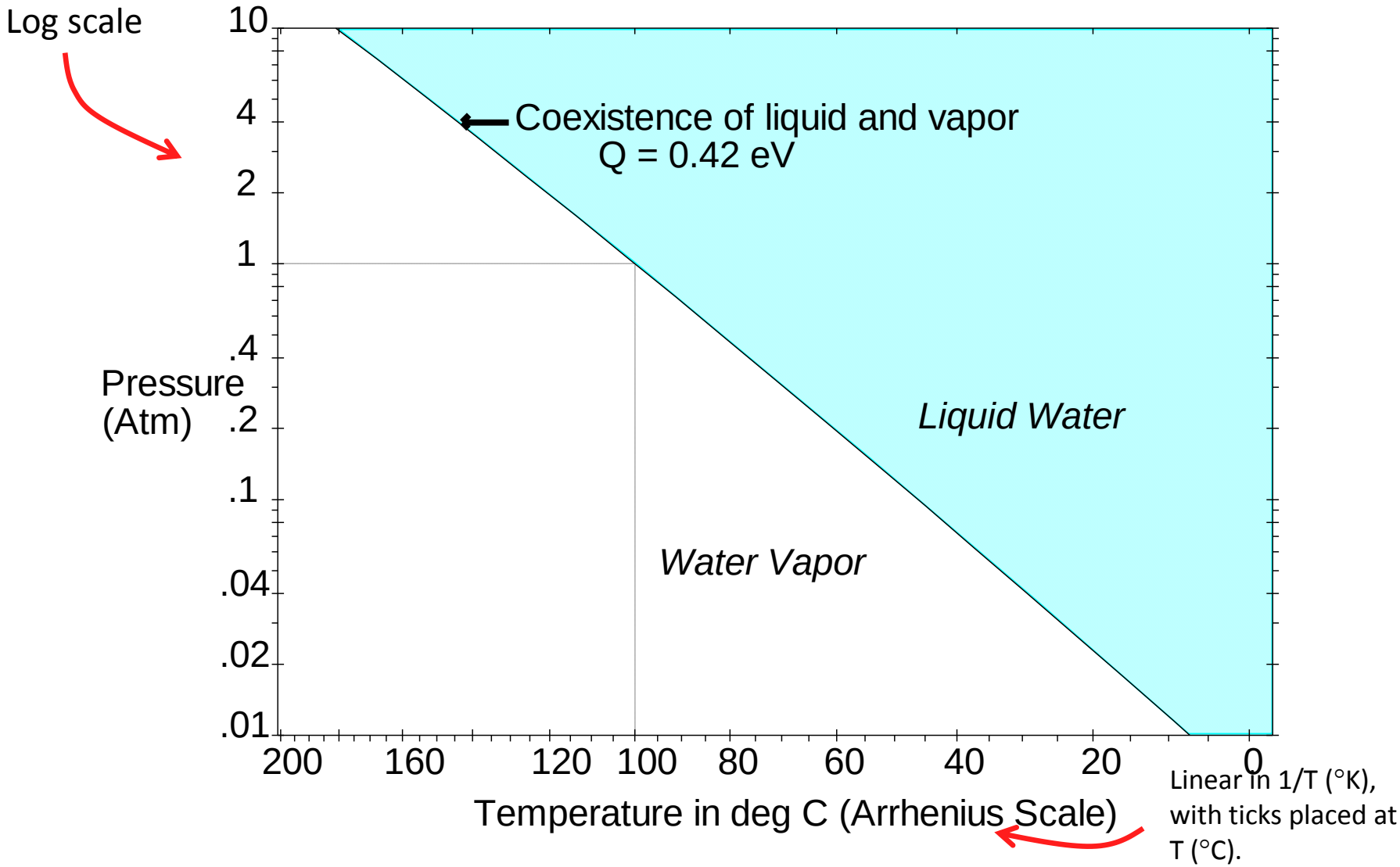
Fig. 4 Full-load ramp-up profile to 156/85 before (top) and after (bottom) optimization of fan. After optimization, the wet-bulb temperature is always below temperature at any point in the load.

HAST Ramp-Down Requirements

- Mechanical pressure relief must be slow (3 h).
- Vent when pressure reaches 1 atm.
- Hold RH at test value.
  - Units must retain moisture acquired during test.



Vapor Pressure and Relative Humidity



Vapor Pressure and Relative Humidity

$$H = \frac{\text{Actual water vapor pressure at temperature } T}{\text{Saturated water vapor pressure at temperature } T}$$

or $$P_{\mathrm{H_2O}} = H \times P_{\mathrm{sat}}(T)$$

Important.

What is P_{sat}?

$$P_{\mathrm{sat}}(T) = P_0 \exp\left(-\frac{\lambda M}{RT}\right) = P_0 \exp\left(-\frac{Q_P}{kT}\right) \quad Q_P = \frac{k\lambda M}{R} = 0.42 \text{ eV}$$

Where

λ = 2262.6 joule/gm (latent heat of vaporization)

M = 18.015 gm/mole, R = 8.32 joules/(mole K), k = 8.617×10^{-5} eV/K

This is a fair approximation. The main benefit is physical insight.

Vapor Pressure and Relative Humidity

An accurate formula for P_{sat} (in Pascals) is

$$P_{sat}(T) = 1000 \times \exp\left(\sum_{n=0}^{3} a_n \times x^n\right), \quad x = \frac{1}{273 + T(^\circ\mathrm{C})}$$

$$a_0 = 16.033225, \quad a_1 = -3.5151386 \times 10^3,$$

$$a_2 = -2.9085058 \times 10^5, \quad a_3 = 5.0972361 \times 10^6$$

which is accurate to better than 0.15% in the range 5 C< T < 240 C.

1 atm = 101325 pascals

This is an accurate formula.

Vapor Pressure and Relative Humidity

- Relative humidity at "hot" die in steady state.
  - Partial pressure of water vapor is the same everywhere:

$$P_{\mathrm{H_2O}}(\mathrm{die}) = P_{\mathrm{H_2O}}(\mathrm{ambient})$$

  - So RH at die is given by:

$$H(\mathrm{die}) \times P_{\mathrm{sat}}(T_{\mathrm{ambient}} + \Delta T_{\mathrm{ja}}) = H(\mathrm{ambient}) \times P_{\mathrm{sat}}(T_{\mathrm{ambient}})$$

  - or

$$H(\mathrm{die}) = H(\mathrm{ambient}) \times \frac{P_{\mathrm{sat}}(T_{\mathrm{ambient}})}{P_{\mathrm{sat}}(T_{\mathrm{ambient}} + \Delta T_{\mathrm{ja}})}$$