ECE 510 Lecture 15
Manufacturing Test Methods

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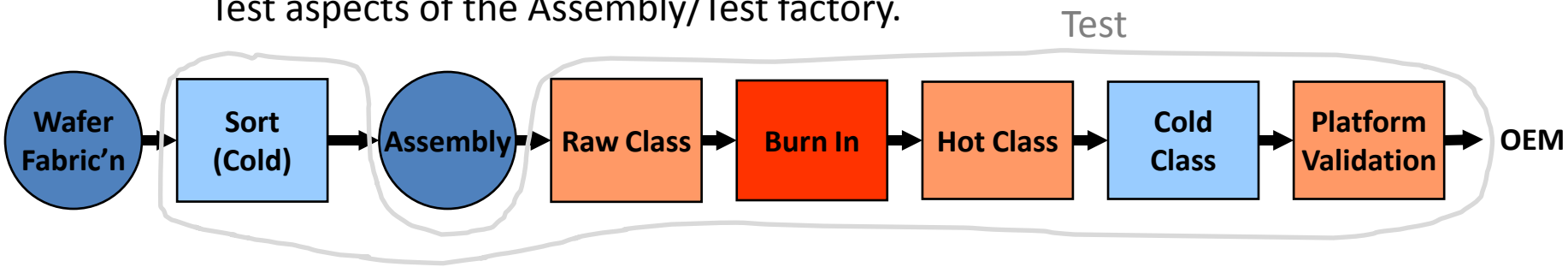
Outline

- Manufacturing Test Flow
  - The “Ramp”.
  - Initial Flow.
  - High-Volume Manufacturing (HVM) Flow.
- Purpose of Various “Test Modules”.
- Monitors: Containing Risk in High-Volume Manufacturing
- What’s Inside a “Test Module”.
- Mutual Coverage of Tests and Patterns.
- Stop-on-Fail (SOF) Figures of Merit from Coverage Metrics
- Measuring Mutual Coverage with Continue-on-Fail (COF) Data

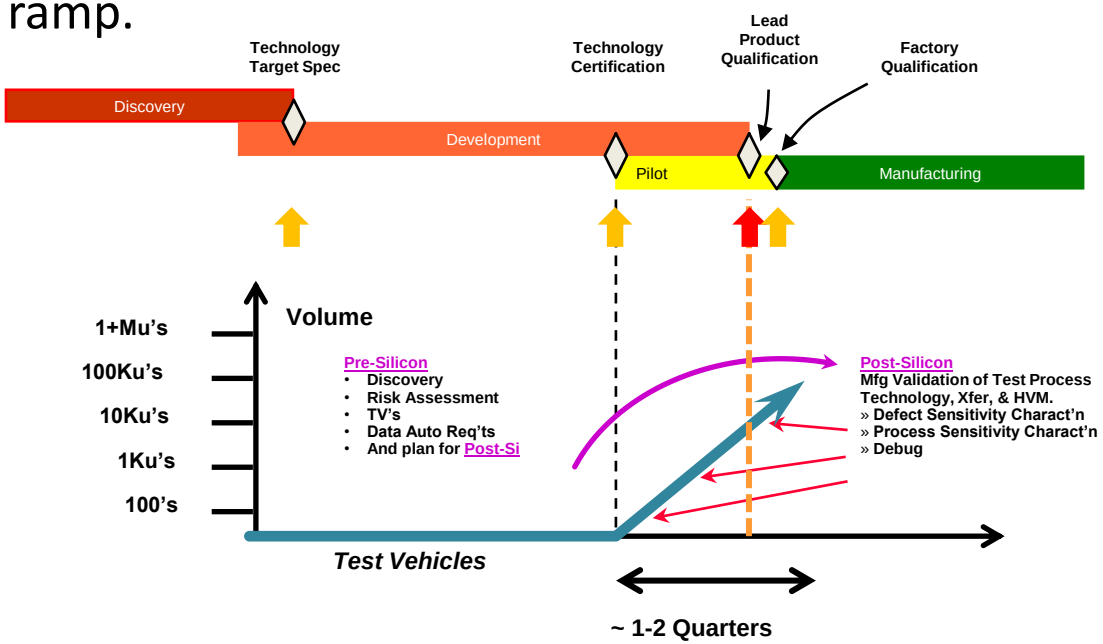
Fab and Assembly/Test

- Fab: Wafer Fabrication
  - Silicon wafers are processed through many steps.
  - The entire process is referred to as wafer fabrication.
  - The factories in which this is done are called “Fabs”.
  - At the end of fabrication, wafers are tested by “e-test” which provides the Fab with feedback at the transistor level.
  - The first product-specific test after fabrication is Sort.
  - Sort is done at the wafer level.
  - The primary measure of success of the Fab is the yield at Sort.
- Assembly/Test
  - Wafers are sent to Assembly factories where they are singulated into individual dies, put into packages and tested.
  - The primary focus of the Test Methodology lectures of the course is on the Test aspects of the Assembly/Test factory.



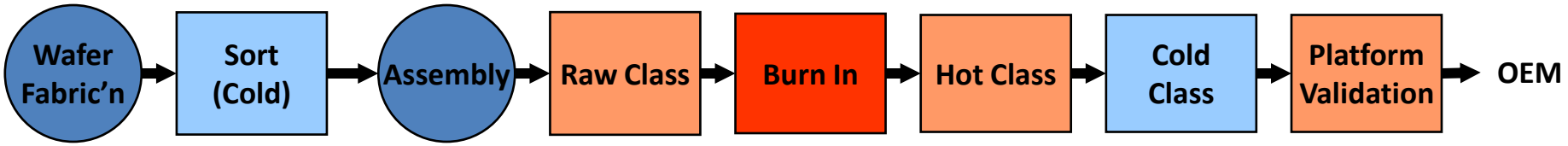
HVM Methods

- Several methods are needed to convert the initial manufacturing process to a high-volume process (HVM) while containing the risks:
  - RCE. Raw Class Elimination.
  - CSE. Cold Socket Elimination.
  - BITR. Burn In Time Reduction.
  - TTR. Test Time Reduction.
  - PVSE. Platform Validation Screen Elimination.
- These all depend on using data acquired during the early stages of the product ramp.

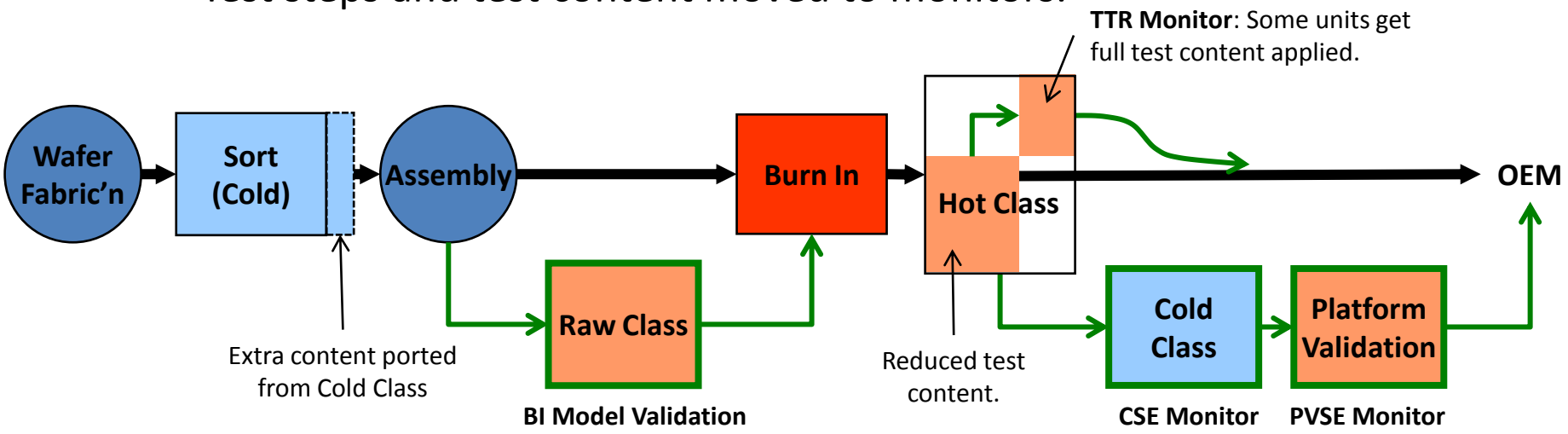


Integrated Circuit Manufacturing Test

- Initial manufacturing process
  - Low volumes, data-intensive.



- High-volume manufacturing process
  - Test steps and test content moved to monitors.

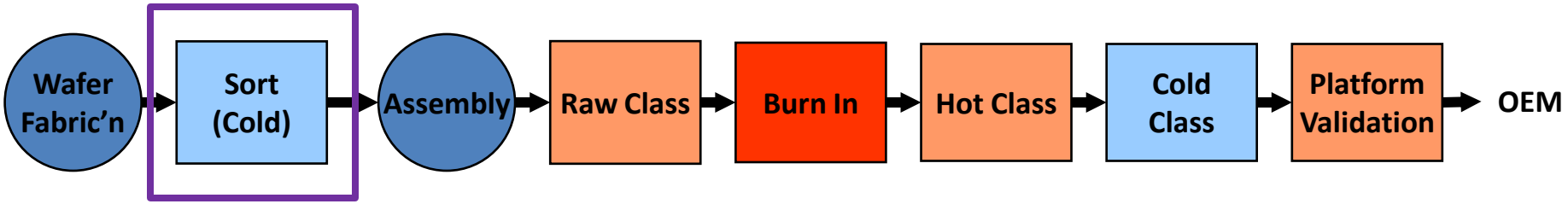


Outline

- Manufacturing Test Flow
- Purpose of Various “Test Modules”.
  - Sort, Class, Burn In, Platform Validation.
- Monitors: Containing Risk in High-Volume Manufacturing
- What’s Inside a “Test Module”.
- Mutual Coverage of Tests and Patterns.
- Stop-on-Fail (SOF) Figures of Merit from Coverage Metrics
- Measuring Mutual Coverage with Continue-on-Fail (COF) Data

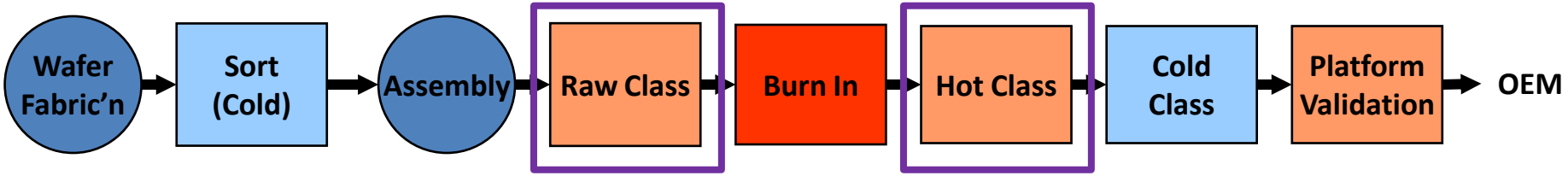
Sort

- Done at wafer level.
  - Signal and power environment non-optimal. So timings are loose, etc.
- Test times are several seconds.
- Gives feedback to Fab on process health.
- Screens for gross manufacturing defects.
- Screens and classifies dies for downstream manufacturing.
  - Screen: Greatly reduces number of defective dies packaged.
  - Classify: eg. Low Isb dies get mobile packages. High Isb dies have different burn in settings.
- The only cold temperature test socket remaining in the HVM test flow.
  - Cold Class removal is enabled by making Sort more effective at screening cold defects.



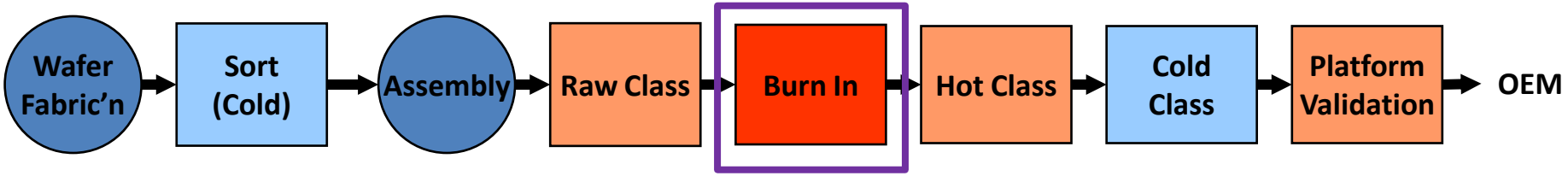
Hot Class and Raw Class

- Guarantees product timing, voltage & thermal specifications at hot corner.
  - Dies passing at worst corner (hot, low Vcc) pass at all lower temperatures and higher voltages – except for some specific kinds of “cold” defects.
- Test times are several seconds.
- Classifies units by speed (speed binning).
- Screens defects including: assembly, hot temperature sensitive, latent reliability defects activated by B/I.
- Gives feedback to Assembly on Assembly Factory process health.
- Pre-Burn-In Class separates Assembly and Fab latent reliability defects.
- Raw Class Elimination (RCE) occurs when product has been validated to match burn in models.
  - Thereafter, defect density measured at Sort suffices.
  - ATE testers used for Raw Class are released to serve as Hot Class testers.



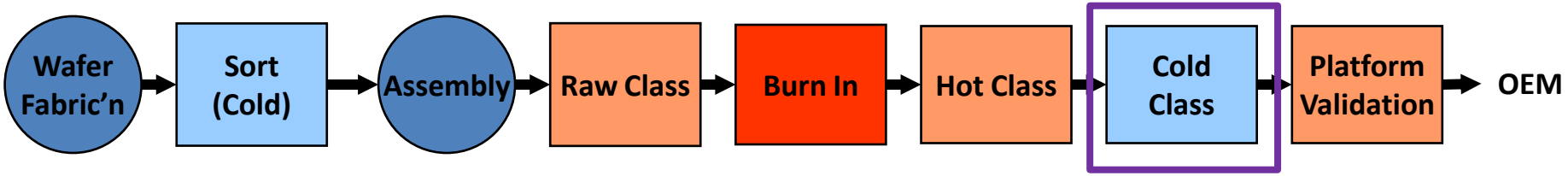
Burn In

- Operates units at high voltage and temperature so that latent reliability defects may be “activated” and so screened by subsequent Class tests.
- Burn in times range from about an hour to several hours.
- Many (100’s) of units are stressed in parallel in burn in ovens.
- Load/unload times are key factors in the efficiency of the process.
- Validation of the stress is important – for example ensuring that the voltage is really being applied.
- Burn-In time reduction (BITR) is driven by
  - Fab process killer defect density reduction, which also reduces LRD density.
  - Carefully(!) putting brief high voltage stresses into Sort and Class.
- Test-during-burn-in (TDBI) is a perennial idea that never works.



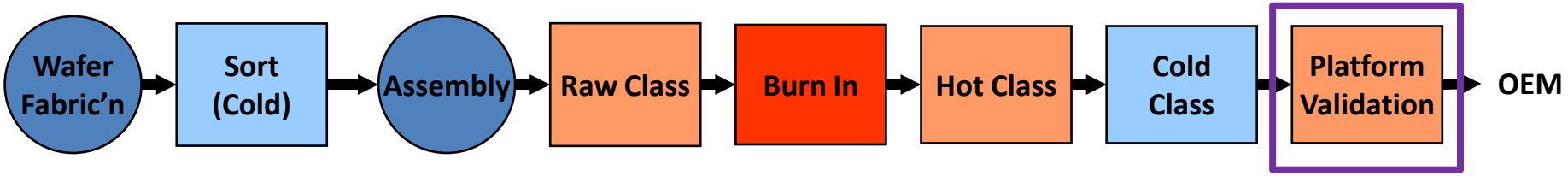
Cold Class

- Guarantees product timing, voltage & thermal specs at cold corner.
- Some Fab defects fail at the cold corner, rather than at the hot corner.
  - Caused by specific kinds of defects ("salicide").
- Uses expensive ATE equipment. Test times are several seconds.
- Provides two kinds of feedback:
  - Isolates cold defects for Fab, so that Fab can can eliminate them.
  - Identifies tests that can be moved to Sort to screen cold defects there.
- Cold Socket Elimination (CSE) must occur before the ramp reaches half the planned volume so testers used for Cold Class can be used for Hot Class.



Platform Validation

- Closely matches end-use conditions. It is an end-use platform (eg. PC) with user-like software running.
  - Heavily engineered to work in a factory. Robot handling, make/break contact sockets, etc.
- Test times are 10's of minutes.
- An in-factory measure of expected customer production-line failure rates.
- Finds failing patterns missing in upstream test programs.
- Provides an initial use-like screen, but test times are long (10's of minutes) so must be quickly moved to monitor status.

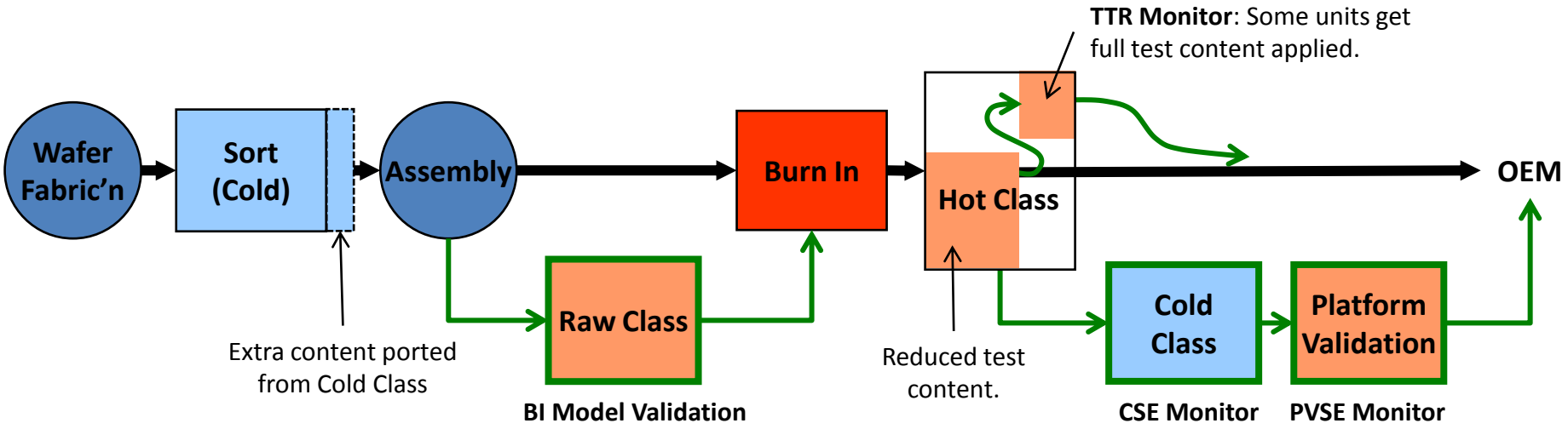


Outline

- Manufacturing Test Flow
- Purpose of Various “Test Modules”.
- Monitors: Containing Risk in High-Volume Manufacturing
  - Statistical Design of Monitors.
- What’s Inside a “Test Module”.
- Mutual Coverage of Tests and Patterns.
- Stop-on-Fail (SOF) Figures of Merit from Coverage Metrics
- Measuring Mutual Coverage with Continue-on-Fail (COF) Data

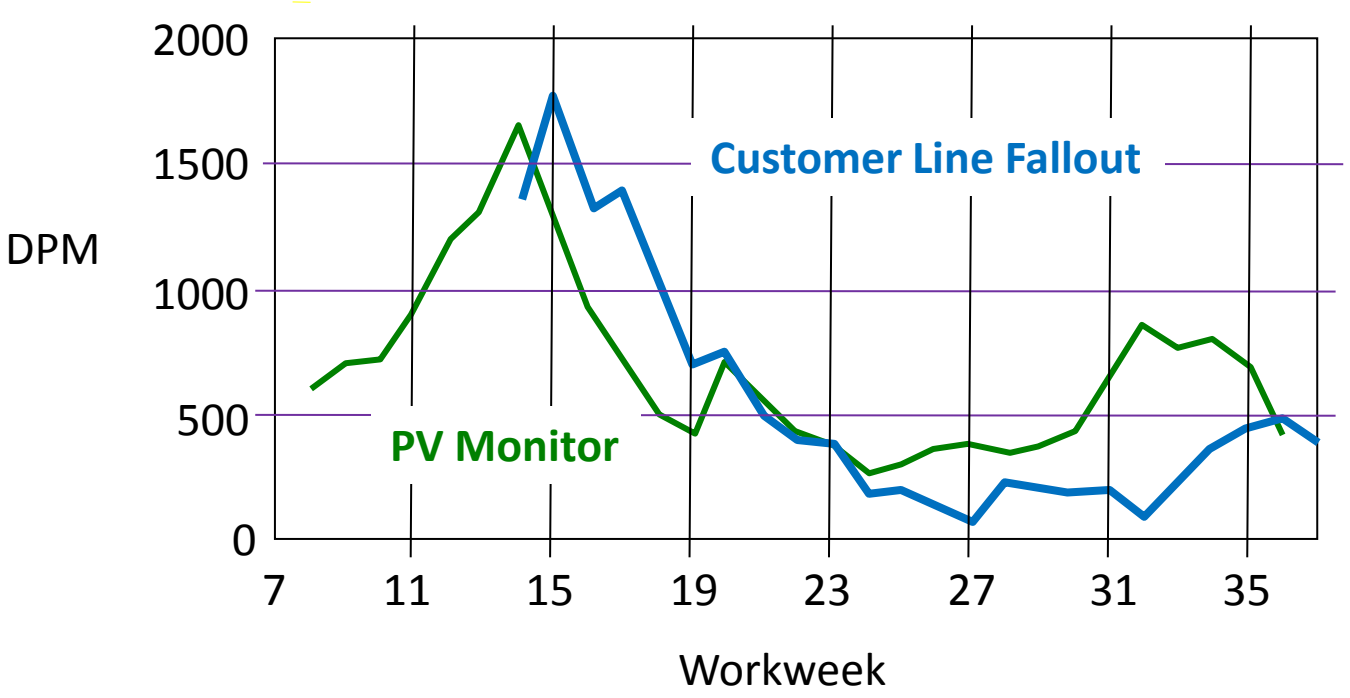
Monitors

- The HVM process requires monitors which sample the volume.
- Benefit: Greatly increased efficiency.
- Risk: Whenever a screen is replaced by a monitor there are producer and customer risks.
- Sampling plans for monitors must be designed to meet specific producer and customer risk parameters.
  - Example: What is the escape risk for a sudden increase in proportion defective?

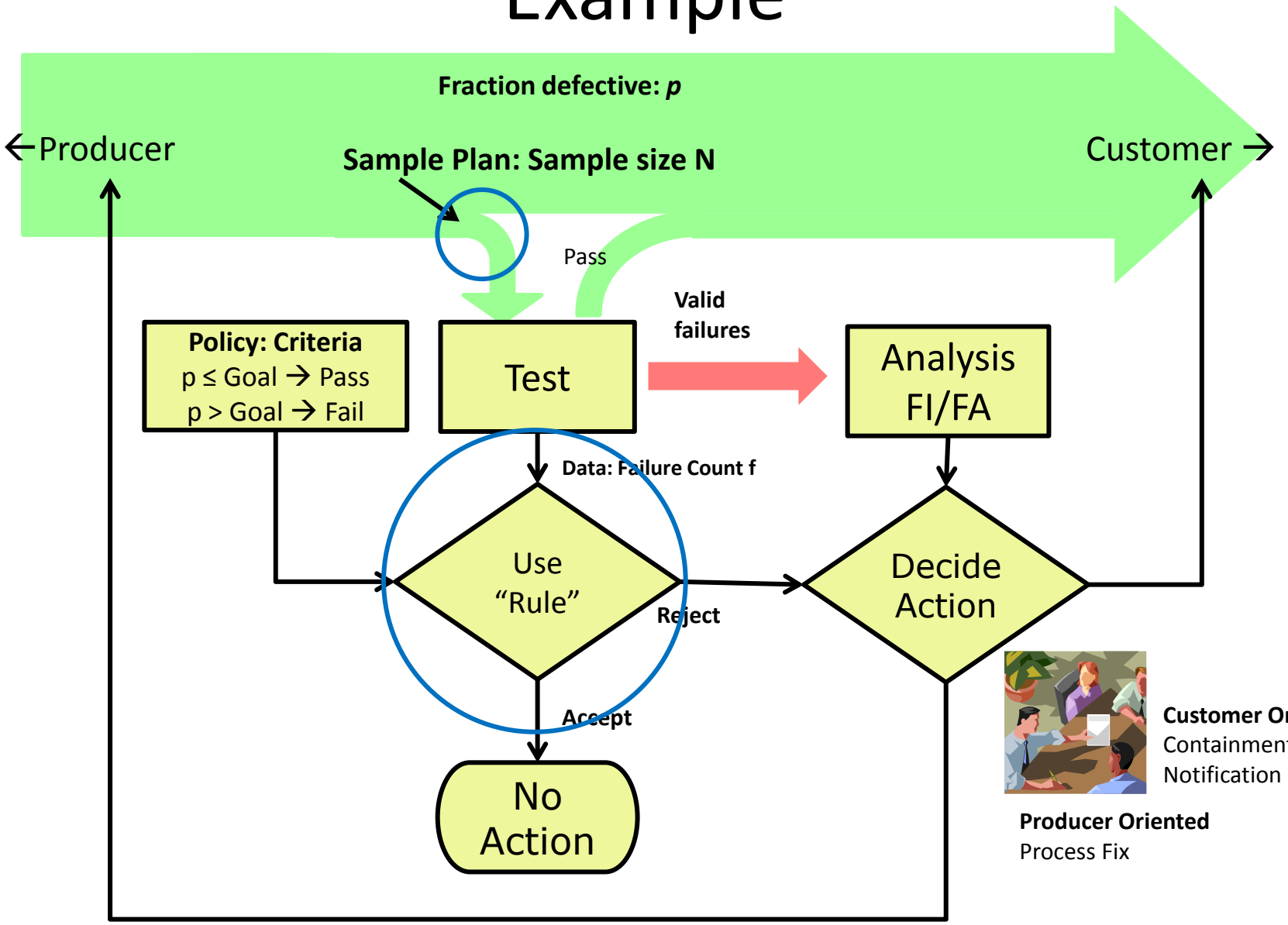


PV Monitor to CLF Correlation

- The PV monitor provides an in-factory indicator of customer-perceived failure rates; “customer line fallout (CLF)”.
- The signal is seen about 1 week before the customer sees it.



Example


Fraction defective: p
←Producer
Sample Plan: Sample size N
Customer →
Pass
Valid failures
Policy: Criteria
p ≤ Goal → Pass
p > Goal → Fail
Test
Analysis FI/FA
Data: Failure Count f
Use "Rule"
Reject
Decide Action
Accept
No Action
Customer Oriented
Containment, Notification
Producer Oriented
Process Fix

Risk Matrix

For a specific hypothetical value of *p* (percent defective).

		The Truth (Known only to God)	
		***p* ≤ Goal**	***p* > Goal**
Decision by Rule	**Accept**	**Correct** Probability = $(1 - \alpha)$	**Customer Risk** Beta Risk Type II Error Probability = β
	Reject	**Producer Risk** Alpha Risk Type I Error Probability = α	**Correct** Probability = $(1-\beta)$

Operating Characteristic (OC)

- Every “rule” with an “Accept” or “Reject” result has an operating characteristic (OC) curve.
- The OC curve is the probability of an “Accept” result as a function of the fraction of the population, *p*, that is defective.
- No matter how complicated the “rule” is, an OC curve exists.
- The OC curves for simple rules can be calculated analytically.
- More complicated rules may require Monte-Carlo simulation.
  - Calculation is simplified because the OC curve is only needed at two particular values of *p* (AQL and RQL, see below.)

Example Rules 1

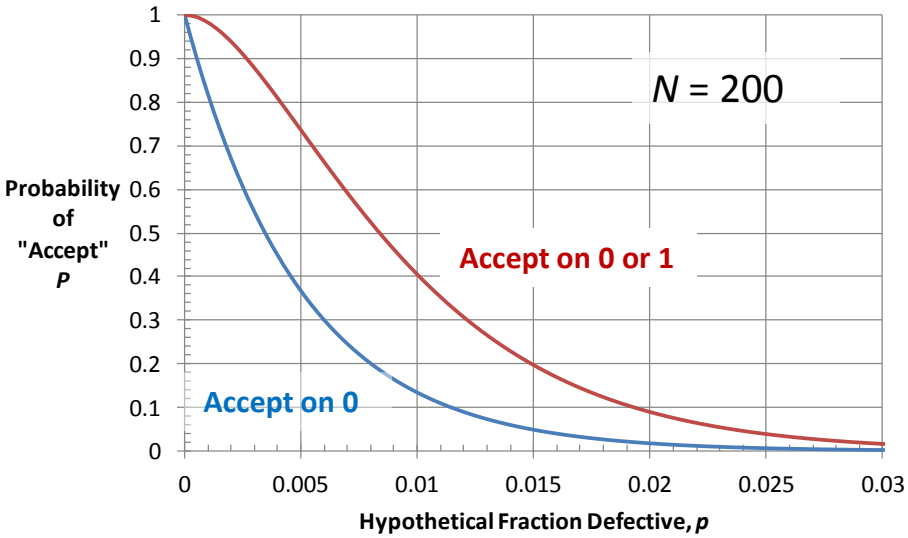
- Minimum and "Nearly Minimum" Sample Size Rules
- A sample of size N is taken.
- Assumptions
  - Sample is small compared to total population sampled.
  - Population defect density is uniform.
- Rule 1a: Accept on 0, Reject on 1 or more.
  - Probability of the "Accept" decision is the probability of no defects

$$P_{\text{accept}} = (1-p)^N$$

- Rule 1b: Accept on 0 or 1, Reject on 2 or more
  - Probability of the "Accept" decision is the probability of 0 or 1 defects

$$P_{\text{accept}} = (1-p)^N + N \times p \times (1-p)^N$$

OC Curves



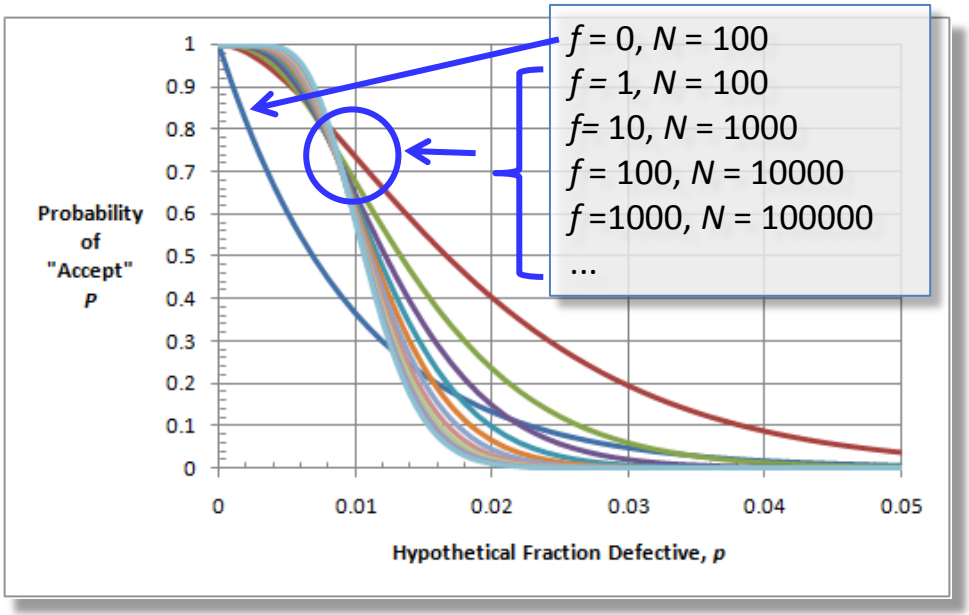
Example Rule 2

- Rule for any sample size.
- A sample of size *N* is taken.
- Assumptions
  - Sample is small compared to total population sampled.
  - Population defect density is uniform.
- Rule
  - For 0, 1, 2,..,*f* failures in the sample, the decision is “Accept”.
  - For *f* + 1or more failures in the sample, the decision is “Reject”.
- Probability of no failures in the sample, that is, of the “Accept” decision is

$$P_{\text{accept}} = \sum_{n=0}^{f} \frac{N!}{f!(n-f)!}(1-p)^{N-f}\, p^{f}$$
$$= \text{BINOMIAL}(f, N, p, \text{TRUE})$$

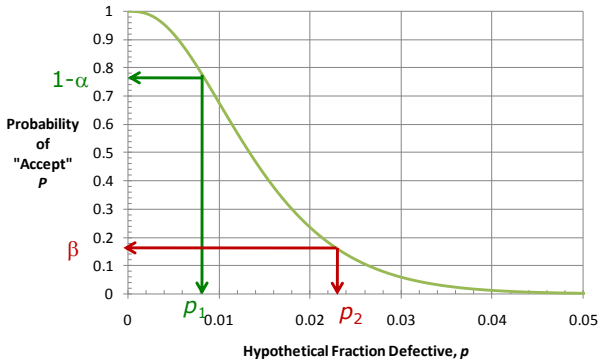
Notes:

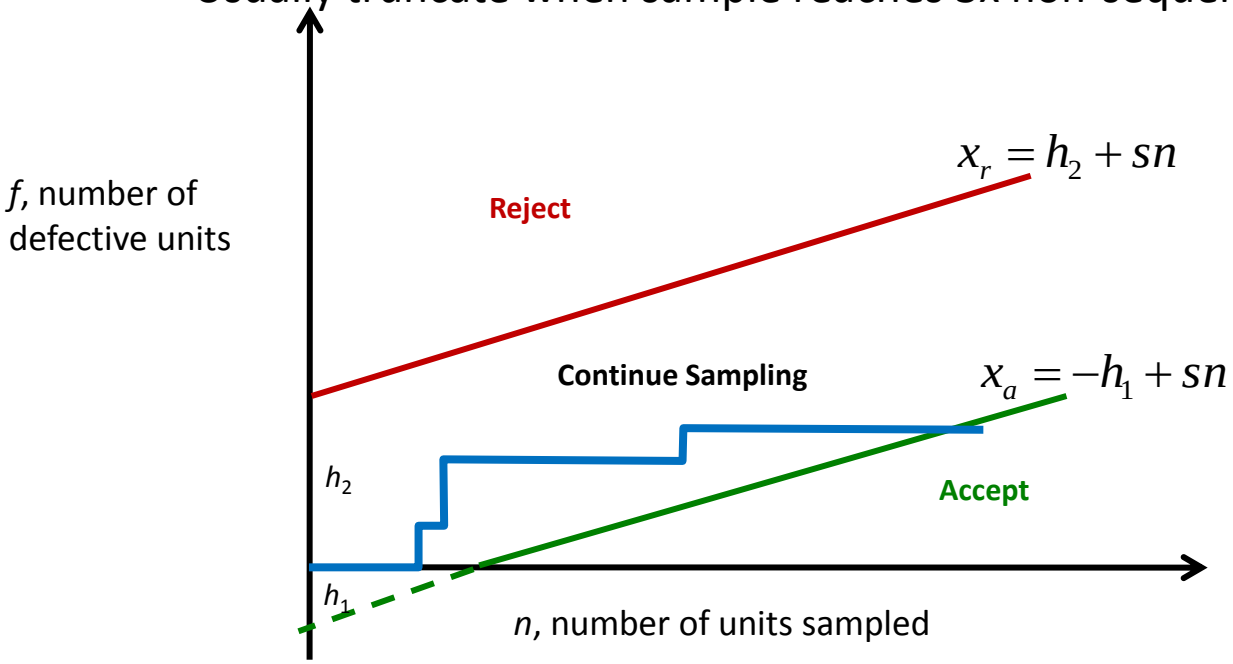
- This rule generalizes Rules 1.
- The OC Picker Tool” tab on the Rel Calculator Excel tool may be used to implement this rule.



Example Rule 3

- Sequential Sampling
  - Benefit: Sample size "adapts" to defectivity.
  - Risk: Can lead to 100% sampling.
- Assumptions (for this example)
  - Sample is small compared to total population.
- Rule
  - See diagram and equations.
  - Usually truncate when sample reaches 3x non-sequential plan.





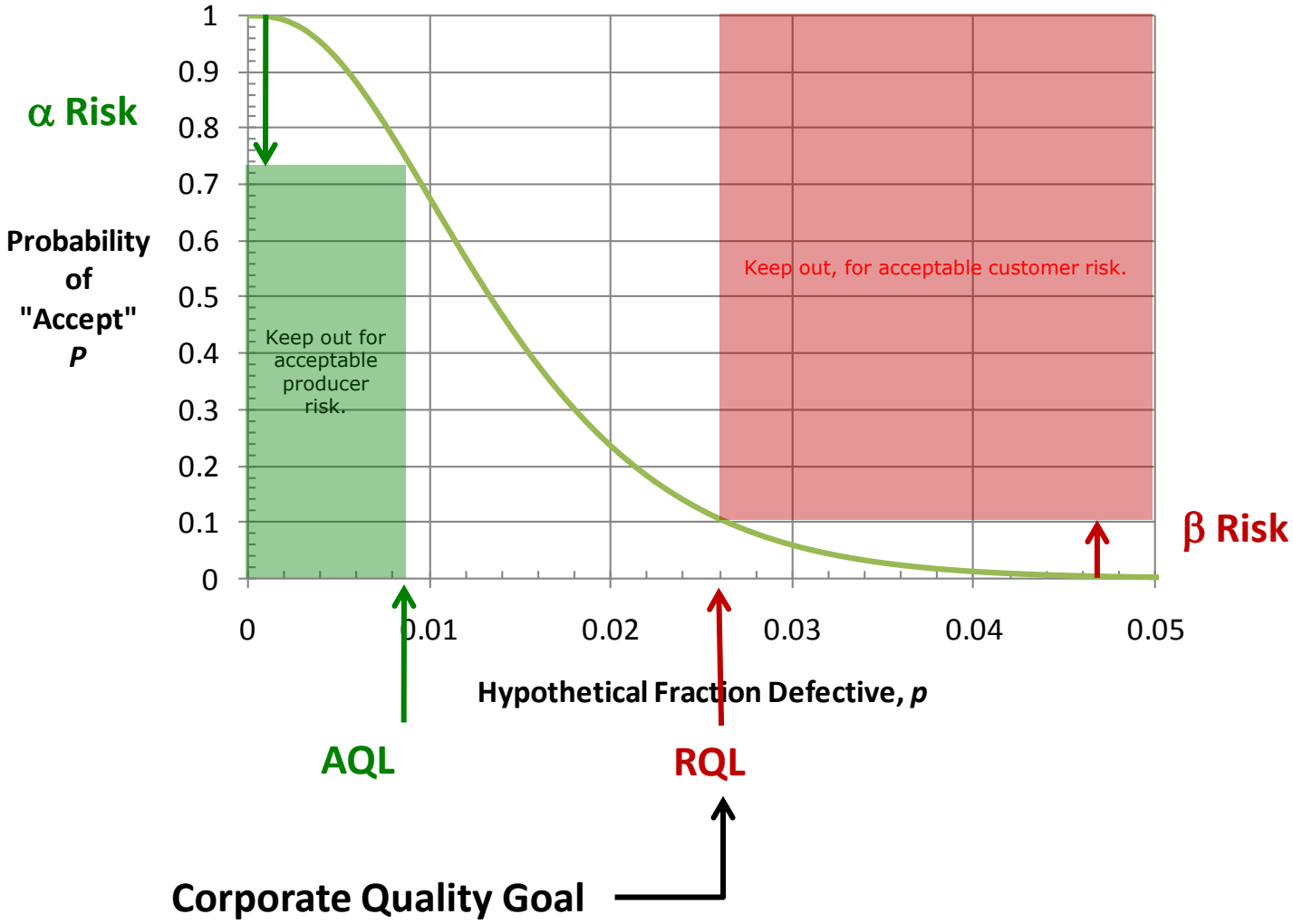
$$k = \ln \frac{p_2(1-p_1)}{p_1(1-p_2)}$$

$$h_1 = \left(\ln \frac{1-\alpha}{\beta} \right) \Big/ k$$

$$h_2 = \left(\ln \frac{1-\beta}{\alpha} \right) \Big/ k$$

$$s = \ln \left(\frac{1-p_1}{1-p_2} \right) \Big/ k$$

Producer and Customer Risks



Producer and Customer Risks

- Producer requires..
  - Low risk α of rejecting a lot with less than some percent defective, called AQL (Acceptable Quality Level).
    - OC curve outside the green zone meets producer requirements.
- Customer requires..
  - Low risk β of accepting a lot with more than some percent defective, RQL (Rejectable Quality Level).
    - OC curve outside in the red zone meets customer requirements.
- Notes
  - AQL < RQL, unless everything is tested.
  - Lot Tolerance Percent Defective (LTPD) is RQL when $\beta = 0.1$

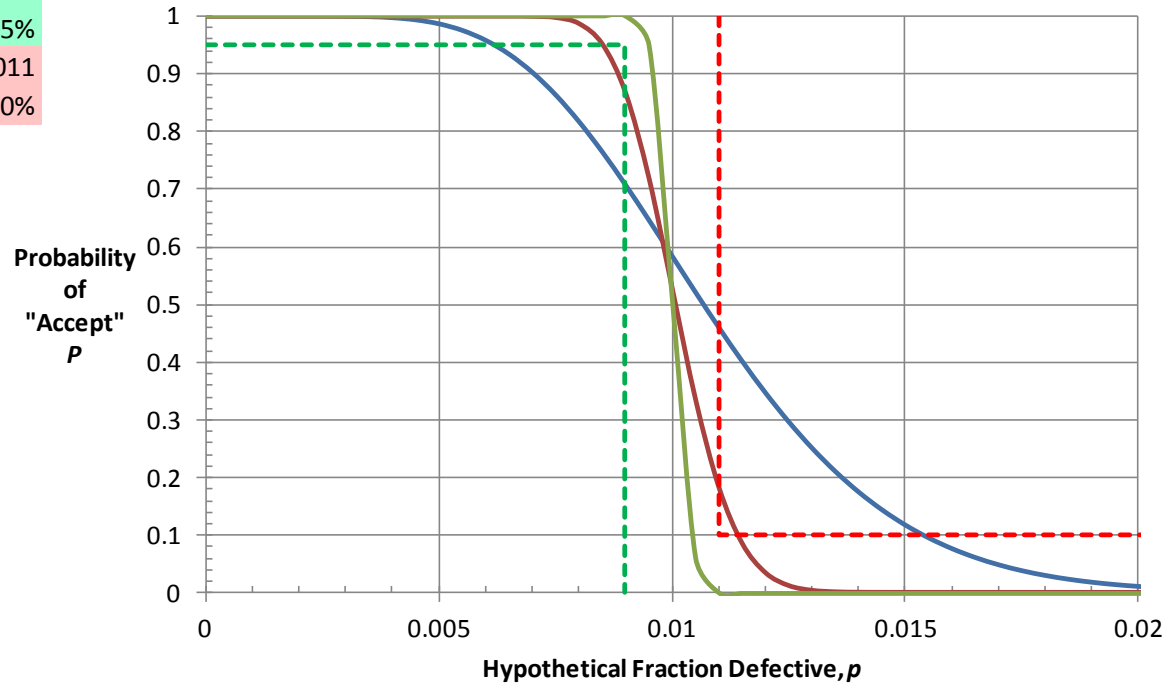
Recipe

- Determine Customer Risk
  - Policy owned by Q&R and Marketing.
  - Assign RQL = Corporate Quality Goal
  - Choose Beta risk = Standard value, 10%.
- Determine Producer Risk
  - Policy owned by Manufacturing.
  - Assign AQL (< RQL) = Some fraction, < 1, of RQL.
  - Choose Alpha risk = Standard value, 5%.
- Choose sampling plan that will
  - Avoid green and red zones in the OC Picker tool, but...
  - Minimizes cost by just “grazing” the red/green zones.

Example

- Only if <u>everything</u> is screened, can AQL=RQL.
  - OC curve becomes a step function as $N \to \infty$.

AQL	0.009
Alpha	5%
RQL	0.011
Beta	10%



10	100	1000	←Accept, f (Reject on f + 1).
1000	10000	100000	←SS

Homework 15.1

- Use the “OC Picker Tool” tab on the Rel Calculator Excel tool.
- Find the sample size for RQL = 1% and Beta risk of 10% when the producer risk is “don’t care”. This will be the minimum sample size.
- Find a sampling plan which meets RCL/Beta = 1%/10% and AQL/Alpha = 0.5%/5% requirements.
- What is the probability of a “Reject” decision if the population is 1.5% defective and the rule is: Sample 7000 units, accept on 95, reject on 96.

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- Manufacturing Test Flow
- Purpose of Various “Test Modules”.
- Monitors: Containing Risk in High-Volume Manufacturing
- What’s Inside a “Test Module”.
  - Modules → Tests → Patterns
- Mutual Coverage of Tests and Patterns.
- Stop-on-Fail (SOF) Figures of Merit from Coverage Metrics
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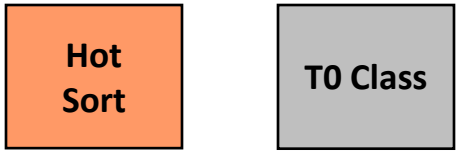
Contents of a Test Module

- Each manufacturing test module (Sort, Class, PV) contains a sequence of tests of different kinds.
- The initial tests check for basic electrical continuity and leakage before tests that exercise logic are applied.

What's inside these?



- Logical tests are executed by patterns which are sequences of vectors.
  - Patterns exercise the logic so that faults can be found by unexpected outputs.
  - The Sematech data describes only vectors.
- There are several kinds of logical tests
  - Stuck-At, Functional, Delay, Iddq
  - A failure occurs at a specific vector.
- Scan is a Design-for-Test feature for Stuck-At, Delay, and Iddq tests.
  - The IBM ASIC in the Sematech study has a scan DFT feature.
- Logical tests are done at several environmental conditions
  - Voltage: Nominal/Low/High (Sematech does all 3).
  - Temperature: Cold/Room/Hot (Sematech does hot Sort, RT Class).

Test Hierarchy