Plastic Package Reliability

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Outline

- Plastic Package Technology
- Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - Moisture
  - Thermal
  - Thermo-mechanical
Plastic-Encapsulated Microcircuits

- Molding compound (MC) in PEMs comes in direct contact with the die and chip connections.
Plastic-Encapsulated Microcircuits

- Die is mounted on a lead frame (A42 or Cu).
- Bonds are made by:
  - Wirebond: Au, moving to Cu in early 2000’s.
  - TAB: Tape-Automated Bonding.
  - C4: Controlled Collapse Chip Connect.
- Assembly is encapsulated in molding compound.
  - Molding compound is in direct contact with die, wire bonds, etc.
- External leads are trimmed and solder plated.

Alloy 42
Fe 58% Ni 42% alloy with CTE matching Si.
Molding Compounds

• MC is thermoset (curing) epoxy, typically novolac.
  – Cures at ~ 170-180°C.
  – Silica “filler” controls CTE and increases thermal conductivity.
  – MCs are (now) free of ionic contaminants.

• Glass Transition ~ 140°C.

• Moisture properties of MC:
  – Permeable to moisture.
  – Absorbs moisture. “Hygroscopic.”

Note distinction between thermoset and thermoplastic.
Molding Compound Properties

- At the glass transition (> 140 °C)...

MC strength decreases

CTE increases

FIGURE 4-16 Shear modulus versus temperature data for an epoxy molding compound. Data show the effect of postcure on the thermomechanical properties. Frequency is 1 rad/sec.

FIGURE 4-1 A plot of expansion versus temperature for an epoxy molding compound. The dashed line is the temperature derivative of expansion, which is defined as the coefficient of thermal expansion. Note the higher CTE above the glass transition temperature.

Molding Compound Properties, ct’d

- Molding compound strongly absorbs water.
  - *Saturation* uptake is proportional to RH, and *independent of temperature*.
  - *Rate* of uptake *depends strongly on temperature*.

### Key Material Properties

- Material properties which drive temperature cycling-induced failure mechanisms.

| Material                     | Thermal Coeffic’
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Material properties</td>
<td>of Expansion</td>
</tr>
<tr>
<td>(ppm/°C) “TCE”</td>
<td>Young's Modulus</td>
</tr>
<tr>
<td>Material properties</td>
<td>(GPa)</td>
</tr>
<tr>
<td>Material properties</td>
<td>Thermal</td>
</tr>
<tr>
<td>Material properties</td>
<td>Conductivity</td>
</tr>
<tr>
<td>Material properties</td>
<td>(W/m °C)</td>
</tr>
<tr>
<td>Copper</td>
<td>17</td>
</tr>
<tr>
<td>Alloy 42</td>
<td>5 Match!</td>
</tr>
<tr>
<td>Silicon</td>
<td>3</td>
</tr>
<tr>
<td>Molding Compound</td>
<td>21</td>
</tr>
<tr>
<td>Alumina</td>
<td>6.5</td>
</tr>
<tr>
<td>PC Board</td>
<td>15-17</td>
</tr>
</tbody>
</table>
Outline

• Plastic Package Technology

● Stress and Test Flows

• Mechanisms
  – Moisture-mechanical
  – Moisture
  – Thermal
  – Thermo-mechanical
Life of an Integrated Circuit

Assembly → Shipping → Storage → OEM/ODM Assembly → End-user Environment

Desktop

Mobile PC

Handheld

Slide by Scott C. Johnson.
Stress/Test Flow

From: JEP150 “Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components” (JEDEC)

Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Simulate shipping, storing, and OEM board mounting process.

Simulate in-service end use conditions.

Determine pass/fail. Diagnose failures.

Figure 1 — Levels of Assembly - Interaction of packaging technical concerns
Industry Reliability Standards

- International
  - ISO International Standard Organization
  - IEC International Electrotechnical Commission
- Europe
  - CEN, CENELEC Comité Européen de Normalisation Électrotechnique
- Japan
  - JIS Japanese Industrial Standard, EIAJ
- US
  - MIL (US Department of Defense), EIA/JEDEC

For US commercial products JEDEC standards have mostly superseded MIL standards.
Preconditioning

• Preconditioning simulates board assembly.

• Specified by

http://www.jedec.org/

Free downloads, registration required.
Preconditioning Flow

JESD22-A113F

Annex A Typical Preconditioning Sequence Flow

<table>
<thead>
<tr>
<th>Step</th>
<th>Item</th>
<th>Details</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initial Electrical Test</td>
<td>- Replace any failing devices - Optional for testing by Supplier</td>
<td>4.1</td>
</tr>
<tr>
<td>2</td>
<td>Visual Inspection</td>
<td>- Replace any failing devices - Optional for testing by Supplier</td>
<td>4.2</td>
</tr>
<tr>
<td>3</td>
<td>Temperature Cycling</td>
<td>- 5 cycles -40 °C to 60 °C - Optional shipping simulation based on product requirements</td>
<td>4.3</td>
</tr>
<tr>
<td>4</td>
<td>Bake</td>
<td>- 240 °C, 120 °C - Optional for testing by Supplier</td>
<td>4.4</td>
</tr>
<tr>
<td>5</td>
<td>Moisture Soak</td>
<td>- Soak time and conditions per IPC/JEDEC J-STD-020 based on device MSL level</td>
<td>4.5</td>
</tr>
<tr>
<td>6</td>
<td>Reflow</td>
<td>- 9-reflow cycles using profiles per IPC-JEDEC J-STD-020, document rev of J-STD-020 used - SnPb or Pb-free profile based on device end-use process</td>
<td>4.6</td>
</tr>
<tr>
<td>7</td>
<td>Flux Application</td>
<td>- 10-s full immersion dip in activated water soluble flux - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages</td>
<td>4.7</td>
</tr>
<tr>
<td>8</td>
<td>Cleaning</td>
<td>- DI water rinse - Remove all flux residual - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages</td>
<td>4.8</td>
</tr>
<tr>
<td>9</td>
<td>Drying</td>
<td>- Room ambient drying - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages</td>
<td>4.9</td>
</tr>
<tr>
<td>10</td>
<td>Final Electrical Test</td>
<td>- If all devices pass then ready for Reliability Testing - If valid failures are found then devices may have been tested to the wrong MSL level or something is substandard with the devices - Optional for testing by Supplier</td>
<td>4.10</td>
</tr>
</tbody>
</table>

IPC/JEDEC J-STD-020D.01

Table 5.1 Moisture Sensitivity Levels

Table 5.2 Classification Reflow Profiles

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Environmental Test

• Stress-based testing (traditional).
  – Pro:
    • Well-established standards. Lots of historical data. Good for comparisons.
    • Little information about mechanism or use is required.
  – Con:
    • Overstress: May foreclose a technology.
    • Understress: Misses a mechanism.
      – May not accurately reflect a use environment.

• Knowledge-based testing.
  – Risk assessment of Use and Mechanism guides test.

To keep things simple, we’ll follow this approach.
### 5.5 Device qualification requirements

#### Table 1 — Device qualification tests

<table>
<thead>
<tr>
<th>Stress</th>
<th>Ref.</th>
<th>Abbv.</th>
<th>Conditions</th>
<th># Lots / SS per lot</th>
<th>Duration / Accept</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Temperature Operating Life</td>
<td>JESD22-A108, JESD22-A109</td>
<td>HTOL</td>
<td>$T_J \geq 125^\circ C$ $V_{cc} \geq V_{max}$</td>
<td>3 Lots / 77 units</td>
<td>1000 hrs / 0 Fail</td>
</tr>
<tr>
<td>Early Life Failure Rate</td>
<td>JESD22-A108, JESD22-A109</td>
<td>ELFR</td>
<td>$T_J \geq 125^\circ C$ $V_{cc} \geq V_{max}$</td>
<td>See ELFR Table</td>
<td>48 $\pm 6$ hrs / 0 Fail</td>
</tr>
<tr>
<td>Low Temperature Operating Life</td>
<td>JESD22-A108, JESD22-A109</td>
<td>LTOL</td>
<td>$T_J \leq 50^\circ C$ $V_{cc} \geq V_{max}$</td>
<td>1 Lot / 32 units</td>
<td>1000 hrs / 0 Fail</td>
</tr>
<tr>
<td>High Temperature Storage Life</td>
<td>JESD22-A103</td>
<td>HTSL</td>
<td>$T_a \geq 150^\circ C$</td>
<td>3 Lots / 25 units</td>
<td>1000 hrs / 0 Fail</td>
</tr>
<tr>
<td>Non-Volatile Memory Cycling Endurance</td>
<td>JESD22-A117</td>
<td>NVCE</td>
<td>$25^\circ C$ and $85^\circ C$ $T_J \geq 55^\circ C$</td>
<td>3 Lots / 77 units</td>
<td>Up to Spec. Max Cycles per note (e) / 0 Fail</td>
</tr>
<tr>
<td>Data Retention for Non-Volatile Memory, High Temperature</td>
<td>JESD22-A117</td>
<td>HTDR</td>
<td>Option 1: $T_J = 100^\circ C$</td>
<td>3 Lots / 39 units</td>
<td>Cycles per NVCE ($25^\circ C$ / 56 hours / 0 Fail / note (f))</td>
</tr>
<tr>
<td>Option 2: $T_J \geq 125^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Non-Volatile Memory Low Temperature Retention and Read Disturb:</td>
<td>JESD22-A117</td>
<td>LTDR</td>
<td>$T_a = 25^\circ C$</td>
<td>3 Lots / 38 units</td>
<td>Cycles per NVCE ($25^\circ C$ / 300 hrs / 0 Fail / note (g))</td>
</tr>
<tr>
<td>Latch-Up</td>
<td>JESD78</td>
<td>LU</td>
<td>Class I or Class II</td>
<td>1 Lot / 3 units</td>
<td>0 Fail</td>
</tr>
<tr>
<td>Electrical Parameter Assessment</td>
<td>JESD86</td>
<td>ED</td>
<td>Datasheet</td>
<td>3 Lots / 10 units</td>
<td>$T_a$ per datasheet</td>
</tr>
<tr>
<td>Human Body Model ESD</td>
<td>JES-001</td>
<td>ESD-HBM</td>
<td>$T_a = 25^\circ C$</td>
<td>3 units</td>
<td>Classification</td>
</tr>
<tr>
<td>Changed Device Model ESD</td>
<td>JESD22-C01</td>
<td>ESD-CDM</td>
<td>$T_a = 25^\circ C$</td>
<td>3 units</td>
<td>Classification</td>
</tr>
<tr>
<td>Accelerated Soft Error Testing</td>
<td>JESD98-2, JESD98-3</td>
<td>ASER</td>
<td>$T_a = 25^\circ C$</td>
<td>3 units</td>
<td>Classification</td>
</tr>
<tr>
<td>“OK” or System Soft Error</td>
<td>JESD99-1</td>
<td>SSER</td>
<td>$T_a = 25^\circ C$</td>
<td>Minimum of 16-66 Device Hrs or 10 fails</td>
<td>Classification</td>
</tr>
</tbody>
</table>

#### Note:
- TS (JESD22-A106) and AC (Steam) (JESD22-A102) are not recommended. Very different from use.

### 5.6 Nonhermetic package qualification test requirements

#### Table 2 — Qualification tests for components in nonhermetic packages

<table>
<thead>
<tr>
<th>Stress</th>
<th>Ref.</th>
<th>Abbv.</th>
<th>Conditions</th>
<th># Lots / SS per lot</th>
<th>Duration / Accept</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL Preconditioning</td>
<td>JESD22-A113</td>
<td>PC</td>
<td>Per appropriate MSL level per J-STD-020</td>
<td>Electrical Test (optional)</td>
<td></td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>JESD22-A103, JESD22-A109</td>
<td>HTSL</td>
<td>$T_a = 150^\circ C$ $T_J$</td>
<td>3 Lots / 25 units</td>
<td>1000 hrs / 0 Fail</td>
</tr>
<tr>
<td>Temperature Humidity Bias (Steam)</td>
<td>JESD22-A101</td>
<td>THB</td>
<td>$85^\circ C$, $85%$ RH, $V_{max}$</td>
<td>3 Lots / 25 units</td>
<td>1000 hrs / 0 Fail</td>
</tr>
<tr>
<td>Temperature Humidity Bias (High Accelerated Temperature and Humidity Stress)</td>
<td>JESD22-A110</td>
<td>HAST</td>
<td>$130^\circ C$, $110^\circ C$, $85%$ RH, $V_{max}$</td>
<td>3 Lots / 25 units</td>
<td>90/264 hours or equivalent per package construction / 6 Fail</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>JESD22-A104</td>
<td>TC</td>
<td>$8^\circ C$ $T_J$ to $+125^\circ C$</td>
<td>3 Lots / 25 units</td>
<td>700 cycles / 0 Fail</td>
</tr>
<tr>
<td>Unbiased Temperature-Humidity Autoclave</td>
<td>JESD22-A102</td>
<td>AC</td>
<td>$121^\circ C$ or $100%$ RH</td>
<td>3 Lots / 25 units</td>
<td>90 hrs / 0 Fail</td>
</tr>
<tr>
<td>Soldier Ball Shear</td>
<td>JESD22-B117</td>
<td>SBBS</td>
<td>Characterization</td>
<td>30 balls / 2 units</td>
<td>Pyrex 66</td>
</tr>
<tr>
<td>Bond Pull Strength</td>
<td>MD011</td>
<td>BPS</td>
<td>Characterization, Pre Encapsulation</td>
<td>30 bonds / 5 units</td>
<td>Pyrex 66 (note 6)</td>
</tr>
<tr>
<td>Bond Shear</td>
<td>JESD22-B116</td>
<td>BS</td>
<td>Characterization, Pre Encapsulation</td>
<td>30 bonds / 5 units</td>
<td>Pyrex 66 (note 6)</td>
</tr>
<tr>
<td>Solderability</td>
<td>MD003</td>
<td>SD</td>
<td>Characterization</td>
<td>3 lots / 22 leads</td>
<td>6 Fail</td>
</tr>
<tr>
<td>Tin Whisker Acceptance</td>
<td>JESD22-A111, JESD22-A112</td>
<td>WSIR</td>
<td>Characterization per JESD 201</td>
<td>See JESD 201</td>
<td></td>
</tr>
</tbody>
</table>

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Knowledge-Based Test

- Knowledge-Based Testing
  - Stress depends on knowledge of use conditions and mechanisms.
  - Risk assessment, using methods
    - JEDEC: JESD94, JEP143, JEP148
    - Sematech: “Understanding and Developing Knowledge-based Qualifications of Silicon Devices” #04024492A-TR

- Pro:
  - Stresses fit the product and its use. May make a product feasible.

- Con:
  - Easy to miss mechanisms in new technologies and overlook use conditions in new applications.
  - Tempting to misapply to “uprate” devices, relax requirements.
Example Stress Flow

Focus of this talk.

- **ELFR**
  - Early life failure rate.
  - 168 hrs
  - JESD22-A108

- **HTOL**
  - High temperature operating life.
  - 168 -1000 hrs
  - JESD22-A108

- **HTSL (Bake)**
  - 1000 hrs
  - JESD22-A103

- **TC**
  - 700 cycles
  - 3 cycles/hr
  - 233 hrs
  - JESD22-A104

- **THB or HAST**
  - 1000 hrs (85/85)
  - JESD22-A101
  - 96 hrs (130/85)
  - JESD22-A110

Assumptions

- 168 h is equivalent to early life requirement
- SS computed from goal. eg. $3 \times 611 = 1833$

Preconditioning.

- JESD22-A113

(Lots x Units)

- 3 x 77

- 3 x 25

December 3, 2015
Outline

• Plastic Package Technology
• Stress and Test Flows
• Mechanisms
  • Moisture-mechanical
    – Moisture
    – Thermal
    – Thermo-mechanical
Popcorn Mechanism

ELFR

Early life failure rate.
168 hrs
**JESD22-A108**

HTOL

High temperature operating life.
168 -1000 hrs
**JESD22-A108**

HTSL (Bake)

1000 hrs
**JESD22-A103**

TC

700 cycles
3 cycles/hr
233 hrs
**JESD22-A104**

Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
**JESD22-A101**
96 hrs (130/85)
**JESD22-A110**

Preconditioning.
**JESD22-A113**

December 3, 2015
Plastic package cracking due to “popcorn” effect during solder reflow
Plastic package cracking due to “popcorn” effect during solder reflow
Popcorn Damage

Pulse-echo acoustic image through back of 68PLCC that developed popcorn cracks during solder reflow

Popcorn Damage

Pulse-echo acoustic image through top (delamination in black)

Acoustic time-of-flight image indicating package crack

Real-time x-ray image showing deformation in wires where they intersect the crack

132 lead PQFP which was damaged during solder reflow.

Factors Affecting Popcorning

• Molding compound moisture content
  – Temperature/humidity/time exposure before solder.

• Package geometry
  – Dimensions of die paddle.
  – Thickness of molding compound under paddle.

• Peak temperature reached during soldering.

• Adhesion of molding compound to die and/or lead frame.

Not on this list: Pre-existing voids in the plastic package.
H₂O Diffusion/Absorption in MC

Diffusion Coefficient:

\[ D = D_0 \exp\left(-\frac{Q_d}{kT}\right) \]

\( D_0 = 4.7 \times 10^{-5} \text{ m}^2 / \text{sec} \) \( Q_d = 0.50 \text{ eV} \)

Saturation Coefficient:

\[ S = S_0 \exp\left(\frac{Q_s}{kT}\right) \]

\( S_0 = 2.76 \times 10^4 \text{ mole/m}^3\text{Pa} \) \( Q_s = 0.40 \text{ eV} \)

Henry’s Law:

\[ M_{\text{sat}} = PS = H P_{\text{sat}} S \]

H₂O vapor pressure.

Clausius-Clapeyron (approximate):

\[ P_{\text{sat}} \approx P_{\infty} \exp\left(-\frac{Q_p}{kT}\right) \]

\( P_{\infty} = 4.58 \times 10^5 \text{ Atm} \) \( Q_p = 0.42 \text{ eV} \)

Key Observation: Saturated moisture content of molding compound is nearly independent of temperature, and is proportional to RH.

\[ M_{\text{sat}} = HP_{\infty} S_0 \exp\left[\frac{(Q_s - Q_p)}{kT}\right] \]

\( Q_s - Q_p = -0.02 \text{ eV} \)

Nearly zero!
H$_2$O Diffusion/Absorption in MC

**MODEL**

Surface exposed to ambient.

Zero flux or "die" surface

$2L$

**ACTUAL**

Plastic Molding Compound (MC)
H₂O Diffusion/Absorption in MC

Fourier Number = Dt/L^2

Concentration at Die Surface (C)
Total Weight Gain (M)

\[
\frac{(C-C_{\text{init}})}{(C_{\text{eq}}-C_{\text{init}})} \quad \text{or} \quad \frac{(M-M_{\text{init}})}{(M_{\text{eq}}-M_{\text{init}})}
\]

0.8481
Time to 90% Saturation After Humidity Step

Typical Use Saturation Times

Package Moisture Time Constant
(time to 90% saturation)

\[ t(\text{sat}) = 0.8481 \frac{L^2}{D_0} \exp \left( \frac{Q_d}{kT_{mc}} \right) \]

Typical 130/85 HAST Saturation Times

Normal Operating Range

December 3, 2015

Plastic Package Reliability

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Popcorn Model

• A crack propagates to the surface when maximum bending stress $\sigma_{\text{max}}$ exceeds a fracture stress characteristic of the molding compound

$$\sigma_{\text{max}} > \sigma_{\text{crit}} (T_{\text{reflow}})$$

• $\sigma_{\text{crit}}$ depends on MC formulation, and on temperature (see next slide).

Popcorn Model, $\sigma_{\text{crit}}$

$\sigma_{\text{crit}}$ is proportional to molding compound strength.

Source: Kitano, et al. IRPS, 1988
Popcorn Model, $\sigma_{\text{max}}$

- Maximum bending stress occurs at center of long edge of die and is given by:

$$\sigma_{\text{max}} = 6 \times K \times \left( \frac{a}{t} \right)^2 P$$

- $a$ is the length of the die edge.
- $t$ is the thickness of the molding compound over the die.
- $K$ is a geometrical factor ($K = 0.05$ for square pad).
- $P$ is the internal pressure. Depends on
  - Moisture content of molding compound.
    - Depends in turn on RH and T of previous soak ambient.
  - Peak temperature during reflow.
\( \mu(x,t) \equiv \text{Concentration Profile in Molding Cpd.} \)

\( \rho_{\text{cav}}(t) \equiv \text{Moisture Concentration in Cavity} \)

\( P_{\text{cav}}(t) = R \times T_1 \times \rho_{\text{cav}}(t) = \text{Cavity Pressure} \)

\( \mu_0 = H_0 \times P_{\text{sat}}(T_0) \times S(T_0) \equiv \text{Initial Moisture Conc. In Mold. Cpd.} \)

For \( t > 0 \) the boundary condition at \( x = 0 \) is:

\[
P_{\text{cav}}(t) = \frac{\mu(0,t)}{S(T_1)}
\]

Henry’s Law
Popcorn Model, Internal Pressure

Moisture conc. in MC >> (~ 30x) Moisture conc. in cavity.


Inputs

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>T_0</td>
<td>25 C</td>
<td></td>
</tr>
<tr>
<td>H_0</td>
<td>85 % RH</td>
<td></td>
</tr>
<tr>
<td>T_1</td>
<td>215 C</td>
<td></td>
</tr>
<tr>
<td>W_</td>
<td>0.2 cm</td>
<td></td>
</tr>
<tr>
<td>L_</td>
<td>0.01 cm</td>
<td></td>
</tr>
</tbody>
</table>

December 3, 2015
Popcorn Model, Internal Pressure

\[ P_{\text{cav}} \xrightarrow{1 \to 0; \nu \to \infty \ (\text{or} \ t \to 0)} H_0 \times P_{\text{sat}}(T_0) \times \frac{S(T_0)}{S(T_1)} \]

Delamination pressure exists even with no physical void.

Example:

- Unit preconditioned in 85/85 for a long time, then subjected to 215 C solder shock.
- Saturation coefficient has activation energy of 0.4 eV. (eg. Kitano et. al.)
- Steam table pressure at 85 C is 0.57 atm.

\[
P_{\text{cav}} = 0.85 \times 0.57 \times \exp \left( \frac{0.40 \text{ eV}}{8.62 \times 10^{-5} \text{ eV/}^{\circ} \text{K}} \left( \frac{1}{273 + 85} - \frac{1}{273 + 215} \right) \right)
\]

\[= 15.3 \text{ Atmospheres} \quad \text{Wow!!} \]
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  – Moisture-mechanical
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  - Condition B or G
  - (C is too severe)

THB or HAST
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  - JESD22-A101
  - 96 hrs (130/85)
  - JESD22-A110

Preconditioning.
- JESD22-A113

Plastic Package Reliability
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HAST System

• Large vessel (24” dia) requires forced convection.

![Diagram of HAST System]

Fig. 3 The NG HAST chamber operates on the principle of forced convection. This ensures efficient mixing, minimizing temperature gradients across the test volume. Reliability of the fan drive is ensured by a proven design of magnetic coupling feed through.

HAST System
HAST System
HAST Ramp Up Requirements

- Ramp Up: Avoid condensation on load.

Fig. 4 Full-load ramp-up profile to 150/85 before (top) and after (bottom) optimization of fan. After optimization, the wet-bulb temperature is always below temperature at any point in the load.
HAST Ramp-Down Requirements

• Mechanical pressure relief must be slow (3 h).
• Vent when pressure reaches 1 atm.
• Hold RH at test value.
  – Units must retain moisture acquired during test.

~ 3.5 atm

Temperature ramps down while RH stays constant.

1 atm

°C or RH (%)

156/85 Controlled Ramp-Down, Full Load

Dry Bulb*
Wet Bulb*
Tdb(min)
Tdb(max)
RH(set)
RH(max)
RH(min)

Plastic Package Reliability

Hours

December 3, 2015
Peck’s Acceleration Model

- Fundamental environmental parameters are $T$, $H$ and $V$, at the site of the failure mechanism.
  - If the die is the site, this is denoted by “$j$”.
- A frequently used acceleration model is due to Peck
  
  $$AF = (a + b \times V) \times H_j^m \times \exp\left(-\frac{Q}{kT_j}\right)$$

- Find $a$, $b$, $m$, $Q$ from experiments with steady-state stress and negligible power dissipation.
- Typically $a$ is small or zero: Bias is required.
- Requires $H > 0$ for acceleration: Moisture is required.
Moisture: MM Tape Leakage

- Leadframe
- Power Plane
- Ground Plane
Moisture: MM Tape Leakage

Experimental Tape Data:

Tape | m  | Q (eV)
--- | --- | ---
"A" | >12 | 0.74
"B" | 5   | 0.77

Source: C. Hong, Intel, 1991

Acceleration factor is proportional to bias.

\[ AF = \text{Constant} \times V \times H^m \exp\left(-\frac{Q}{kT}\right) \]

December 3, 2015

Plastic Package Reliability

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Moisture: Internal Metal Migration

• TAB Inter-lead Leakage/Shorts
  – Accelerated by voltage, temperature and humidity
  – Seen as early as 20 hrs 156/85 HAST
  – Highly dependent on materials & process

Copper dendrites after 40 hours of biased 156/85 HAST

December 3, 2015
Lead-Stabilizing Tape Leakage

- A vendor process excursion.
- Leakage observed after 336 hours of steam.
- Re-activated by 48 hours at 70C/100% RH
- No leakage seen between leads not crossed by tape
- Rapid decay for leads crossing end of tape
  - Tape dries from exterior inwards

Die
Lead Stabilizing Tape

Tape provides mechanical stability to long leads during wirebond.
Lead-Stabilizing Tape Leakage

Leakage Current (A) vs Recovery Time (Minutes)

- Pins Crossed by Tape
  - Pin 2-3
  - Pin 3-4
- Pins NOT crossed by tape

Source: S. Maston, Intel
Aluminum Bond Pad Corrosion

\[ AF = \text{Constant} \times V \times H^m \exp(-Q / kT) \]

<table>
<thead>
<tr>
<th>Source</th>
<th>(m)</th>
<th>(Q) (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peck (a)</td>
<td>2.66</td>
<td>0.79</td>
</tr>
<tr>
<td>Hallberg &amp; Peck (b)</td>
<td>3.0</td>
<td>0.9</td>
</tr>
</tbody>
</table>

(a) IRPS, 1986; (b) IRPS, 1991.


Shortest path has highest failure rate.

Source: © C. Glenn Shirley
Passivation in Plastic Packages

• Passivation is the final layer on the die.

• Passivation has two main functions:
  – Moisture Barrier
    • Molding compound is not a moisture barrier.
    • Silicon oxides are not good moisture barriers.
    • PECVD silicon nitride or silicon oxynitride film is a good barrier.
    • Film must be thick enough to avoid pinholes, coverage defects.
  – Mechanical Protection
    • Silicon nitride films are brittle.
    • Polyimide compliant film protects silicon nitride.
    • Polyimide can react with moisture (depending on formulation).
Polyimide/Au Bond Failure

- Bonds overlapping passivation don’t necessarily violate design rules.
- But can activate polyimide-related “purple plague” failure mechanisms in combination with moisture.
- Acceleration modeling showed no field jeopardy.
Moisture-Related Gold Bond Degrad’n

Effect of 80 hours of 156/85 HAST vs 156/0 Bake and Centered vs Off-Centered Bonds on Wire Pull Test Data

Source: G. Shirley and M. Shell, IRPS, 1993
Moisture-Related Gold Bond Degrad’n

Wire Pull Strength of Polyimide vs No Polyimide and Centered vs Off-Centered Bonds after 40 hours of 156/85 HAST

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993
Moisture-Related Purple Plague

Cross-section of gold ball bond on aluminum pad after 80 hours at 156C/85%RH
Moisture-Related Gold Bond Degrad’n

\[ b = 112.7 \text{ gm} \]
\[ a_0 = 1.13 \times 10^{10} \text{ (gm - hrs)}^{-1} \]
\[ m = 0.98; \quad Q = 1.15 \text{ eV} \]

\[ F_{50} = \frac{1}{\sqrt{(at)^2 + 1/b^2}} \]
\[ a = a_0 \times h^m \times \exp(-Q/kT) \]
\[ F_p = F_{50} \times \exp(-\sigma \times Z_p) \]
\[ \sigma = 0.17 \]

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993

December 3, 2015
Circuit Failure Due to Passiv’n Defects

Site of failing bit. SRAM after HAST stress.
Courtesy M. Shew, Intel
Circuit Failure Due to Passiv’n Defects

Etch-decorated cross-section of passivation. Note growth seams.
Circuit Failure Due to Passiv’n Defects

SRAM VOLTAGE THRESHOLD MAP FOR CELL PULLUP TRANSISTOR
(Baseline threshold is 0.89 V. Passivation is 0.6 µ nitride, no polyimide.)

After 120 h 156/85. 4 failed bits with Vt > 2.5 V

2 bits recover after further 2 hr bake at 150 C

Source: C. Hong, Intel

December 3, 2015
Acceleration Model Fit of HAST Data

SRAM HAST and 85/85 Bit Failures (No Polyimide)

\[ AF = \text{Constant} \times (a + bV) \times H^m \times \exp(-Q / kT) \]

\[ a = 0.24 \quad b = 0.14 \quad m = 4.64 \quad Q = 0.79 \quad \text{eV} \]

Notes:
- “Standby” = 5.5V bias, low power
- “Active” = 5.5V bias, high power
- 156/85: non-standard, limit of pressure vessel.
- Source: C. G. Shirley, C. Hong. Intel

December 3, 2015
Peck Model Parameters

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Q(eV)</th>
<th>m</th>
<th>Q/m</th>
<th>Q/m &lt; 0.42eV?</th>
<th>Hours of 130/85</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>MM Tape A</td>
<td>0.74</td>
<td>12</td>
<td>0.06</td>
<td>Yes</td>
<td>69</td>
<td>2</td>
</tr>
<tr>
<td>MM Tape B</td>
<td>0.77</td>
<td>5</td>
<td>0.15</td>
<td>Yes</td>
<td>62</td>
<td>2</td>
</tr>
<tr>
<td>Single Bit SRAM</td>
<td>0.79</td>
<td>4.6</td>
<td>0.17</td>
<td>Yes</td>
<td>57</td>
<td>3</td>
</tr>
<tr>
<td>Corrosion, THB (early Peck)</td>
<td>0.79</td>
<td>2.66</td>
<td>0.30</td>
<td>Yes</td>
<td>57</td>
<td>4</td>
</tr>
<tr>
<td>Corrosion, THB (later Peck)</td>
<td>0.90</td>
<td>3</td>
<td>0.30</td>
<td>Yes</td>
<td>39</td>
<td>5</td>
</tr>
<tr>
<td>Bond Shear</td>
<td>1.15</td>
<td>0.98</td>
<td>1.17</td>
<td>No</td>
<td>16</td>
<td>6</td>
</tr>
</tbody>
</table>

Yes/No: Increasing power dissipation at die, slows/accelerates the moisture mechanism.

HAST versus 85/85, ct’d

- For all mechanisms surveyed, 1000 hours of 85/85 is equivalent to < 96 hr of 130/85.
- For packages < 10 mils covering die, moisture saturation occurs within 10 h at 130/85.
- For $T_j-T_a > 10^\circ$C, most mechanisms (with $Q/m < 0.42$ eV) can be more accelerated with cyclical bias.
- 85/85
  - JESD22-A101
- HAST
  - JESD22-A110
Outline

• Plastic Package Technology
• Stress and Test Flows
• Mechanisms
  – Moisture-mechanical
  – Moisture
  ● Thermal
  – Thermo-mechanical
Focus Topic: Acceleration

• Acceleration between two stresses is the ratio of times (or cycles) to achieve the same effect.
• The “same effect” could be the same fraction failing.
  – eg. The ratio of median (not mean!) times to failure in different stresses is the Acceleration Factor (AF).
  • AF is proportional to 1/MTTF

\[
AF(2 \mid 1) = \frac{MTTF_1}{MTTF_2} = \exp \left[ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right]
\]

Thermal ("Arrhenius")

\[
AF(2 \mid 1) = \frac{MTTF_1}{MTTF_2} = \exp \left[ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right] \exp \{ C(V_2 - V_1) \}
\]

Thermal and Voltage

\[
AF(2 \mid 1) = \frac{MTTF_1}{MTTF_2} = \left\{ \frac{a + bV_2}{a + bV_1} \right\} \left\{ \frac{RH_2}{RH_1} \right\} \exp \left[ \frac{Q}{k_B} \left( \frac{1}{T_1} - \frac{1}{T_2} \right) \right]
\]

Moisture ("Peck")

\[
AF(2 \mid 1) = \frac{MCTF_1}{MCTF_2} = \left( \frac{\Delta T_2}{\Delta T_1} \right)^m
\]

Thermal Cycle ("Coffin-Manson")
Thermal Mechanisms

ELFR
- Early life failure rate.
- 168 hrs
  - JESD22-A108

HTOL
- High temperature operating life.
- 168 - 1000 hrs
  - JESD22-A108

HTSL (Bake)
- 1000 hrs
  - JESD22-A103

PC

TC
- 700 cycles
- 3 cycles/hr
- 233 hrs
  - JESD22-A104

THB or HAST
- 1000 hrs (85/85)
  - JESD22-A101
- 96 hrs (130/85)
  - JESD22-A110

Preconditioning.
  - JESD22-A113
Gold-Aluminum Bond Failure

- Gold and Aluminum interdiffuse.
  - Intermetallic phases such as AuAl$_2$ (“Purple Plague”) form.
  - Imbalance in atomic flux causes Kirkendall voiding.
  - Bromine flame retardant is a catalyst.

- Kirkendall voids lead to
  - Bond weakening - detected by wire pull test.
  - Resistance changes in bond - detected by Kelvin measurement of bond resistance.
Thermal (Ordinary) Purple Plague

Cross-section of gold ball bond on aluminum pad after 200 hours at 160°C
Wire Bond Pull Test
Gold-Aluminum Bond Failure

Arrhenius plot of time to 10% of wire pull failure. Activation energy \((Q) = 1.17 \text{ eV}\).

Source: S. Ahmad, Intel

Linear in \(1/T\) \((^\circ \text{K})\), with ticks placed at \(T\) \((^\circ \text{C})\).

1 year (!) (8760h)
Thermal Degradation of Lead Finish

• Only an issue for copper lead frames (not Alloy 42).
• $\text{Cu}_3\text{Sn}$ or $\text{Cu}_6\text{Sn}_5$ inter-metallic phases grow at the interface between solder or tin plating.
• Activation energy ($Q$) for inter-metallic phase growth is 0.74 eV.
• If inter-metallic phase grows to surface of solder or tin plate, solder wetting will not occur.
• Main effect is to limit the number of dry-out bakes of surface mount plastic components.
Thermal Degradation of Lead Finish

Post-plating solder plate

Post burn-in solder plate showing copper-tin intermetallic
Thermal Degradation of Lead Finish

X-section of solder-\textit{plated} lead  \hspace{1cm}  X-section of solder-\textit{coated} lead
Outline

• Plastic Package Technology
• Stress and Test Flows
• Mechanisms
  – Moisture-mechanical
  – Moisture
  – Thermal
  • Thermo-mechanical
Thermomechanical Mechanisms

ELFR
- Early life failure rate.
  - 168 hrs
  - JESD22-A108

HTOL
- High temperature operating life.
  - 168 -1000 hrs
  - JESD22-A108

HTSL (Bake)
- 1000 hrs
  - JESD22-A103

TC
- 700 cycles
  - 3 cycles/hr
  - 233 hrs
  - JESD22-A104
- Condition B or G
  - (C is too severe)

THB or HAST
- 1000 hrs (85/85)
  - JESD22-A101
- 96 hrs (130/85)
  - JESD22-A110

Preconditioning.
  - JESD22-A113

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Plastic Package Reliability

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Cracking Due to Temperature Cycle

Shear Stress

Normal Stress

Void & cracks

Bond and TFC damage

Crack

Die Edge

With crack

Without crack
Crack Propagation in Package

- The rate of crack propagation is also given by

\[
\frac{da}{dN} = Const \times (\Delta K)^m
\]

- But in plastic packages under temperature cycling, the stress concentration factor is

\[
\Delta K = Const \times (\alpha_{moldingcompound} - \alpha_{silicon}) \times (T_{min} - T_{neutral})
\]

- \(\alpha\) is the TCE of MC.

\(\Delta T\) in temperature cycling-driven models is the temperature difference between the neutral (usually cure) temperature, and the minimum temperature of the cycle. \(T_{max}\) is less important.
Package Cracking and Delamination...

..damages Wires, Bonds, and Passivation Films.

Normal (tensile)

Shear

Crack

Wire Shear

Au

Substrate Damage

Silicon

Thin-Film Cracking
Bond Damage: Wires and Ball Bonds

• Cracks can intersect wires, TAB leads.
• Bonds can be sheared at the bond/pad interface
• Shear and tensile normal stress can break wires at their necks.
• Substrate cracks induced during bonding can propagate and cause “cratering” or “chip-out”.
Wire Damage

Wires sheared by wire crack

(Open)
Ball bonds in plastic package after temperature cycle.
Bond Damage

Necking Damage
Bond Damage

Necking fracture
Bond Damage

Delamination induced down bond fail after temperature cycle
Bond Damage and Delamination

Pulse-echo acoustic image of mold compound/die interface in four devices. Delamination is shown in black. White boxes added to show locations of low bond wire pull strength results.

Intermetallic fracture at bond due to shear displacement.

44 PLCC devices that failed after solder reflow and 1000 cycles (-40 to 125°C)

Thin-Film Cracking (TFC)

- Normal (tensile)
- Shear
- Wire Shear
- Substrate Damage
- Crack

Silicon

Thin-Film Cracking
TFC - Plastic Conforms to Die Surface

Die Surface

Replica in Plastic
TFC – Effect on Thin Films

Shear stress applied to passivation

Die Corner

Aluminum

Polysilicon

Die center

Passivation

Crack

PSG

Channel

Polysilicon

PSG

SiO2
Thin-Film Cracking (TFC)

Passivation delamination crack propagates into substrate.

Source: K. Hayes, Intel
Test Chip - Thin Film Cracking

• Thin film cracking (TFC) can be detected electrically by test structures in the corner of the die.
  – Sensitive to opens and to shorts.

• Buss width is varied to determine design rule.

Die edge (saw cut).

TFC sensor

Edge ring

ATC

TFC (20 um bus)

TFC (10 um bus)

BOND PADS

TFC (40 um bus)

TFC (100 um bus)
TFC – Effect of Buss Width

Factors Affecting TFC: Buss Width Effect

Polysilicon meanders under buss edge are vulnerable to crack-induced opens.

Buss Widths

- 21 μ
- 7 μ
- 105 μ

No Contacts

17 μ contacts

3 μ contacts

Narrow buss, or contacts, stabilizes buss, reduces incidence of TFC. Leads to buss width design rules, and buss slotting in die corners.
TFC – Effect of Temperature Cycle

- Drivers: T/C conditions, and number of cycles.
- **Minimum** T/C temperature, not amplitude, is key aspect of stress.
  - Stress depends on difference between cure temperature (neutral stress) and minimum stress temperature.


Same amplitude!
TFC – Effect of Passivation Thickness

- Fraction of PDIP-packaged SRAM failing.
- Post 1K cycle of T/C C.
- No Polyimide die coat.
- Thicker passivation is more robust.

Source: A. Cassens, Intel
## TFC – Effect of Compliant Overcoat

- SRAM in PDIP
- Temperature Cycle Condition C
- Polyimide Overcoat

<table>
<thead>
<tr>
<th></th>
<th>200 cycles</th>
<th>500 cycles</th>
<th>1000 cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Polyimide</td>
<td>0/450</td>
<td>13/450</td>
<td>101/437</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0/450</td>
<td>0/450</td>
<td>0/450</td>
</tr>
</tbody>
</table>
Theory of TFC

- Shear stress applied to die surface by MC
  - Is maximum at die corners
  - Zero at die center.

\[ \sigma(\text{At die Surface}) \]
Theory of TFC, ct’d

- Buss width effect: Okikawa et. al.
- Passivation thickness effect: Edwards et al.
- TFC occurs when and where

$$\sigma(\text{Passivation Surface}) > K \times E \times \left(\frac{t}{L}\right)^2$$

- $K$ = dimensionless constant
- $E$ = Young’s modulus of passivation
- $t$ = Passivation thickness
- $L$ = Buss width

Local strength of passivation.

Thicker passivation, and/or narrower busses implies less TFC.

Thin Film Moisture Delamination

• Saw cut exposes thin film edges to moisture..

• And shear stress tends to peel films.

Substrate (Si)

Thin films

Metal Bond Pad

Polyimide

PECVD Oxynitride/Nitride

Other films

Silicon

Shear stress

Thin film delamination.

Moisture

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Plastic Package Reliability
Test Chip – Thin Film Delamination

- “Edge rings” are lateral moisture barrier.
- Effectiveness of edge rings can be tested electrically by a thin-film delamination (TFD) sensor.

Edge ring

Die edge (saw cut).

Cross section of TFD sensor
Thin-Film Delamination

Delamination at die edge after 168 hours of steam.

Source: C. Hong
Intel
Thin-Film Delamination

Delamination at die edge after 168 hours of steam.

Source: C. Hong
Intel

Crack breaks continuity of TFD sensor

Edge Ring

10 μ
Backup
# Reliability Goals from ITRS 2009

[http://www.itrs.net/reports.html](http://www.itrs.net/reports.html)

## Table PIDS6  Reliability Technology Requirements

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM 1/2 Pitch (mm) (contacted)</td>
<td>52</td>
<td>45</td>
<td>40</td>
<td>36</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) 1/2 Pitch (mm)</td>
<td>54</td>
<td>45</td>
<td>38</td>
<td>32</td>
</tr>
<tr>
<td>MFC Physical Gate Length (nm)</td>
<td>2</td>
<td>24</td>
<td>22</td>
<td>26</td>
</tr>
<tr>
<td>Early failures (ppm) (First 4000 operating hours) [1]</td>
<td>2-2000</td>
<td>2-2000</td>
<td>2-2000</td>
<td>2-2000</td>
</tr>
<tr>
<td>Long term reliability (FITs = failures in 1E9 hours) [2]</td>
<td>1.1000</td>
<td>1.1000</td>
<td>1.1000</td>
<td>1.1000</td>
</tr>
<tr>
<td>SRAM Soft error rate (FITs/MBit) [3]</td>
<td>11,000</td>
<td>11,000</td>
<td>11,000</td>
<td>11,000</td>
</tr>
<tr>
<td>Relative failure rate per transistor (normalized to 2009 value) [4]</td>
<td>1.000</td>
<td>0.71</td>
<td>0.50</td>
<td>0.35</td>
</tr>
<tr>
<td>Relative failure rate per meter of Interconnect (normalized to 2009 value) [5]</td>
<td>1.00</td>
<td>0.50</td>
<td>0.50</td>
<td>0.25</td>
</tr>
</tbody>
</table>

- Infant Mortality
- Wear-out
- Constant fail rate
Sampling

• **JESD47** sample requirements are minimal.
  – Single “snapshot” is a crude validation of the reliability of the product.
  – Small SS does not generate failures to give clues to process weaknesses.

• Risks.
  – Qualification hinges on single failures.
    • Moral hazard to “invalidate” a failure is high.
  – Lot-to-lot variation, excursions.
    • Incoming materials, fab lots, assembly lots, test lots.
Sampling, ct’d

• Number of lots covers risks of machine-to-machine, day-to-day, etc. variation.

• Often minimum SS to validate a goal is chosen.
  – Pro: Saves $, and there are no failures to explain.
  – Con: Pass/fail of the qual is at the mercy of a single failure.
    • Verrry tempting to invalidate a failure.
  – Con: No mechanism learning.

• eg. To validate 500 DPM at ELFR using minimum SS at 60% confidence, 1833 units are required.
  – 500 DPM is a typical goal (see ITRS)
    \[
    SS = \frac{-\ln(1 - cl)}{D}
    \]
    \[
    1833 = \frac{-\ln(1 - 0.6)}{500 \times 10^{-6}}
    \]

Useful “mental furniture” (Accept/Reject \(\Rightarrow 0/1\)}

December 3, 2015
Sampling, ct’d

• For environmental stress, 77 is a typical SS, why?

\[ SS = \frac{-\ln(1-cl)}{D} ; \quad \frac{-\ln(1-0.9)}{3 \times 10^{-2}} = \frac{-\ln(0.1) \times 100}{3} = \frac{230.26}{3} = 76.7 \]

  – So, 0/1 accept/reject validates, to 90% confidence, a failure rate less than 3% at the accelerated condition.

• If the stress corresponds to the lifetime (eg. 7 years) then the average wearout failure rate is

\[ FR = \frac{3 \times 10^{-2}}{7 \times 365 \times 24} \times 10^9 = 489 \text{ Fits} \]

  – This falls into the range of ITRS goals.
Example Data

- Additional attributes enhance value of data.
  - Device type
  - Date code
  - Package type
  - Readouts
  - Failure analysis

Maxim product reliability report RR-1H
Vapor Pressure and Relative Humidity

\[ H = \frac{\text{Actual water vapor pressure at temperature } T}{\text{Saturated water vapor pressure at temperature } T} \]

or \[ P_{\text{H}_2\text{O}} = H \times P_{\text{sat}}(T) \]

What is \( P_{\text{sat}} \)?

\[ P_{\text{sat}}(T) = P_0 \exp\left(-\frac{\lambda M}{RT}\right) = P_0 \exp\left(-\frac{Q_P}{kT}\right) \]

\[ Q_P = \frac{k\lambda M}{R} = 0.42 \text{ eV} \]

Where

\[ \lambda = 2262.6 \text{ joule/gm (latent heat of vaporization)} \]

\[ M = 18.015 \text{ gm/mole, } R = 8.32 \text{ joules/(mole K), } k = 8.617 \times 10^{-5} \text{ eV/K} \]

This is a fair approximation. The main benefit is physical insight.
An accurate formula for $P_{sat}$ (in Pascals) is

$$P_{sat} (T) = 1000 \times \exp \left( \sum_{n=0}^{3} a_n \times x^n \right), \quad x = \frac{1}{273 + T(°C)}$$

$$a_0 = 16.033225, \quad a_1 = -3.5151386 \times 10^3,$$

$$a_2 = -2.9085058 \times 10^5, \quad a_3 = 5.0972361 \times 10^6$$

which is accurate to better than 0.15% in the range 5 °C < T < 240 °C.

1 atm = 101325 pascals

This is an accurate formula.
Vapor Pressure and Relative Humidity

- Relative humidity at “hot” die in steady state.
  - Partial pressure of water vapor is the same everywhere:
    \[ P_{H_2O}(\text{die}) = P_{H_2O}(\text{ambient}) \]
  - So RH at die is given by:
    \[ H(\text{die}) \times P_{\text{sat}} \left( T_{\text{ambient}} + \Delta T_{\text{ja}} \right) = H(\text{ambient}) \times P_{\text{sat}} \left( T_{\text{ambient}} \right) \]
  - Where the ratio, \( h \) is defined as:
    \[ H(\text{die}) = h \times H(\text{ambient}) \]
    \[ h = \frac{P_{\text{sat}} \left( T_{\text{ambient}} \right)}{P_{\text{sat}} \left( T_{\text{ambient}} + \Delta T_{\text{ja}} \right)} \]
Example: At 20/85 and Tja = 4 C, the die is at 24/(0.784x85) = 24/67.

Curves labelled with Tja

Vapor Pressure and Relative Humidity
Test and Failure Analysis

- Moisture-related tests (85/85, HAST, Steam) have specific test/FA reqt’s.
  - Test must be done while unit contains moisture.
    - Within 48 hr.
  - Units must not be “wet”.
    - Wet = liquid water.
- Diagnostic Bake.
- Risk decision before destructive analysis.
HAST versus 85/85

- Moisture MUST be non-condensing. (RH < 100%).
- Both require about < 1% fail. Typical SS ~ 100.
- 130/85 HAST duration is 10x less than 85/85 duration. We’ll see how this was justified.

85/85 (JESD22-A101)

<table>
<thead>
<tr>
<th>Temperature(^1) (dry bulb °C)</th>
<th>Relative Humidity(^1) (%)</th>
<th>Temperature(^2) (wet bulb, °C)</th>
<th>Vapor Pressure(^3) (psia/kPa)</th>
<th>Duration(^3) (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>85 ± 2</td>
<td>85 ± 5</td>
<td>81.0</td>
<td>7.12/49.1</td>
<td>1000(-24, +168)</td>
</tr>
</tbody>
</table>

HAST (JESD22-A110)

<table>
<thead>
<tr>
<th>Temperature(^1) (dry bulb °C)</th>
<th>Relative Humidity(^1) (%)</th>
<th>Temperature(^2) (wet bulb, °C)</th>
<th>Vapor Pressure(^3) (psia/kPa)</th>
<th>Duration(^3) (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 ± 2</td>
<td>85 ± 5</td>
<td>124.7</td>
<td>33.3/230</td>
<td>96 (-0, +2)</td>
</tr>
<tr>
<td>110 ± 2</td>
<td>85 ± 5</td>
<td>105.2</td>
<td>17.7/122</td>
<td>264 (-0, +2)</td>
</tr>
</tbody>
</table>

\[\frac{33.3 - 14.2}{14.2} = 1.34 \text{ atmospheres} \Rightarrow \text{Pressure vessel required.}\]

6 week bottleneck in information turns.

10x less time

December 3, 2015
Example: Comparison of HAST Stds

Table 4-9 Reliability Test Standards Comparison Table

<table>
<thead>
<tr>
<th>Unsat. Pressure Cooker Test</th>
<th>Sony</th>
<th>EIAJ</th>
<th>JEDEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>110±2°C 85±5%RH 1.2x10^5 Pa</td>
<td>• Condition selection</td>
<td>• Condition selection</td>
<td>• Condition selection</td>
</tr>
<tr>
<td>120±2°C 85±5%RH 1.7x10^5 Pa</td>
<td>A</td>
<td>A</td>
<td>Severity selection</td>
</tr>
<tr>
<td>130±2°C 85±5%RH 2.3x10^5 Pa</td>
<td>B</td>
<td>110±2°C 85±5%RH 1.2x10^5 Pa</td>
<td>110±2°C 85±5%RH 1.2x10^5 Pa</td>
</tr>
<tr>
<td>• Voltage application if prescribed</td>
<td>• Voltage application if prescribed</td>
<td>408h, 192h, 96h</td>
<td>264±1h</td>
</tr>
<tr>
<td>• Test time prescribed individually</td>
<td>• Test time prescribed individually</td>
<td>192h, 96h, 48h</td>
<td>130±2°C 85±5%RH 2.3x10^5 Pa</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>96h, 48h, 24h</td>
</tr>
</tbody>
</table>

Intermittent Bias

Test and Failure Analysis Window

From Sony Quality and Reliability Handbook http://www.sony.net/Products/SC-HP/tec/catalog/qr.html

December 3, 2015

Plastic Package Reliability

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Cyclical Stress
One-Dimensional Diffusion Equation Solutions
8 hours on, 16 hours off cycling for PDIP

T(ambient) = 100°C
\( t(\text{sat}) = 28 \text{ hours} \)

T(ambient) = 60°C
\( t(\text{sat}) = 153 \text{ hours} \)

Moisture concentration at the die is constant if Period \( \ll t(\text{sat}) \)
Time-Varying Power Dissipation

• Most moisture-related mechanisms..
  – Have slow or zero rates at zero bias (V=0). \( AF = V \times H_j^m \times \exp(-Q / kT_j) \)
  – Have \( Q/m < 0.42 \text{ eV} \) so, in steady-state, depressed die humidity due to power dissipation slows the rate.

• There is an optimum duty cycle which maximizes the effective acceleration.

\( AF = V \times H_j^m \times \exp(-Q / kT_j) \)
Gold-Aluminum Bond Failure

- Kelvin resistance measurements.
- Resistance increase of Au bonds to Al pads vs bake time.
- Bake at 200 °C.
- Various levels of Br flame-retardant in molding compound.
- Br catalyzes Au-Al intermetallic growth.
- Br flame retardants are being phased out today.

Steady Power Dissipation

• Superimpose log(H) vs 1/T contour plots of
  – Peck model for THB acceleration factor.
  – Partial pressure of water vapor, Psat.

• Contours are straight lines:
  – Peck model: Iso-acceleration contours with slope proportional to $Q/m$.
  – Psat: Isobars with slope proportional to $Q_p = 0.42$ eV.

• Assumption: In steady state, the partial pressure of H$_2$O is the same in the ambient and at the die.

Steady Power Dissipation

Iso-acceleration contours for example mechanism \((m = 4.6, Q = 0.8 \text{ eV})\) superimposed on water vapor pressure isobars.

Typical Climate

Increasing steady-state dissipation (X to Y). Follows isobar.

Relative slope \(Q/m < 0.42 \text{ eV}: \) Deceleration \(Q/m > 0.42 \text{ eV}: \) Acceleration.
### Example: Comparison of HAST Stds

**Table 4-9: Reliability Test Standards Comparison Table**

<table>
<thead>
<tr>
<th></th>
<th>Sony</th>
<th>EIAJ</th>
<th>IEC 60749 (1996-10)</th>
<th>JEDEC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EIAJ ED-4701-3 (1997) Test method B-123A</td>
<td></td>
<td>CHAPTER 3 4C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Condition selection</td>
<td></td>
<td>• Severity selection</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>A</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>130±2°C</td>
<td>110±2°C</td>
<td>110±2°C</td>
<td>110±2°C</td>
</tr>
<tr>
<td></td>
<td>85±5%RH</td>
<td>85±5%RH</td>
<td>85±5%RH</td>
<td>85±5%RH</td>
</tr>
<tr>
<td></td>
<td>2.3×10^5 Pa</td>
<td>1.2×10^5 Pa</td>
<td></td>
<td>264±2h</td>
</tr>
<tr>
<td></td>
<td>Non-steady-state requirements</td>
<td>192h, 96h, 48h</td>
<td></td>
<td>96±8h</td>
</tr>
<tr>
<td></td>
<td>• Continue and perform the soldering heat resistance test.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Voltage application (prescribed individually)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Test time: 200 h</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td></td>
<td></td>
<td></td>
</tr>
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<td></td>
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<td></td>
<td>1.7×10^5 Pa</td>
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<tr>
<td></td>
<td>C</td>
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<tr>
<td></td>
<td>• Voltage application if prescribed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Test time: prescribed individually</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

From Sony Quality and Reliability Handbook [http://www.sony.net/Products/SC-HP/tec/catalog/qr.html](http://www.sony.net/Products/SC-HP/tec/catalog/qr.html)
JEDEC 85/85 and HAST Req’ts

- $T_j - T_a \leq 10^\circ C$: 100% duty cycle.
- $T_j - T_a > 10^\circ C$, 50% duty cycle.

Assumptions:
- 85/85
- Peck Model $m = 4.64$, $Q = 0.79 \text{ eV}$
- $AF = 0$ for $V = 0$.
- MC thickness 50 mils
- Kitano et. al MC properties.

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Vapor Pressure and Relative Humidity

Log scale

Temperature in deg C (Arrhenius Scale) vs. Pressure (Atm)

Coexistence of liquid and vapor

Q = 0.42 eV

Liquid Water

Water Vapor

Linear in 1/T (°K), with ticks placed at T (°C).

Plastic Package Reliability

December 3, 2015
This is an example of a packaged part as it might be used in a product.
This is a close-up of the package substrate showing the many layers of conductors and insulators.

- C4 bumps
- Conductive traces and vias (yellow)
- Polymer insulating layers (green)
- Substrate core
- A “land”
- OEM socket pin
Location: Silicon (vs. Package)

“Back end” = interconnects

“Front end” = transistors

Interlayer dielectric (ILD)
Metal interconnect
Via

Transistor

Source
Gate
Channel
Drain
Gate Oxide
Le
Cratering damage on bond pads
Bond Damage

Bond shear at die corners after temperature cycle
Bond Damage (TAB)

TAB cratering and diffusion barrier damage revealed by wet etch.
Bond Damage (TAB)

TAB bonds Au/Al intermetallic formed at cracks in Ti barrier
Bond Damage (TAB)

Crater under TAB bonds
"Popcorn" Design Rules

Cracking sensitivity of PLCC packages after saturation in 85/85 followed by vapor-phase reflow soldering at 215 °C.
Crack Propagation in Test Conditions

• Tensile Test of Notched Samples
  – Measure crack growth rate for sinusoidal load:
    – Sample geometry and load determine stress intensity factor, $K$.
    – Plot crack growth rate $da/dN$ versus $K$ on log-log plot to determine Coffin-Manson exponent, $m$:
Crack Propagation in Test Conditions

Slope of lines on log-log plot

\[ \frac{da}{dN} = Const \times (\Delta K)^m \]

\( m \approx 20 \)