Plastic Package Reliability

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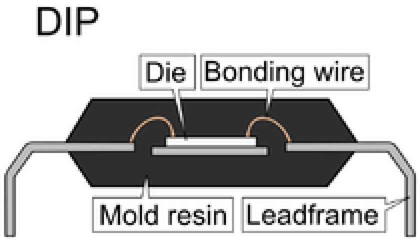
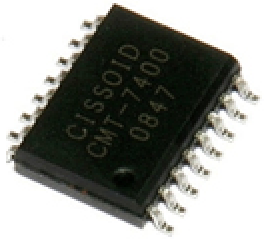
Outline

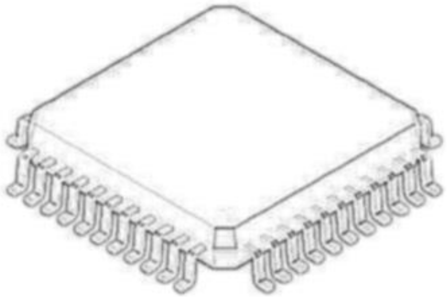
- ● Plastic Package Technology
- Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - Moisture
  - Thermal
  - Thermo-mechanical

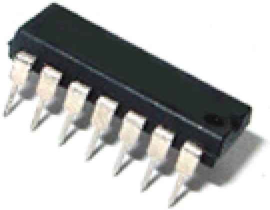
Plastic-Encapsulated Microcircuits

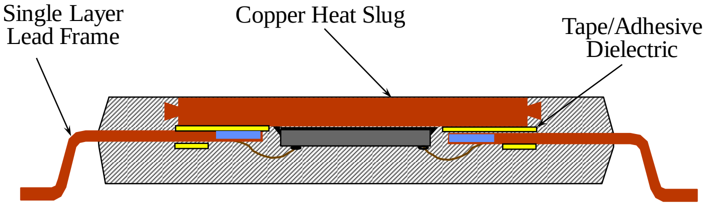
- Molding compound (MC) in PEMs comes in direct contact with the die and chip connections.

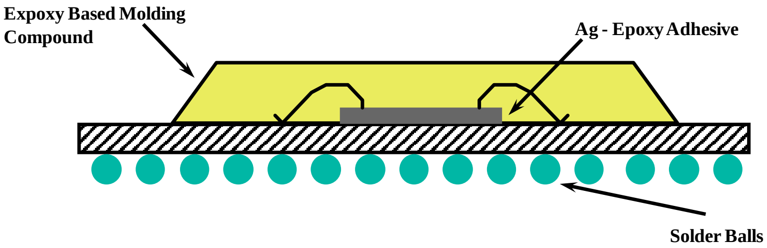


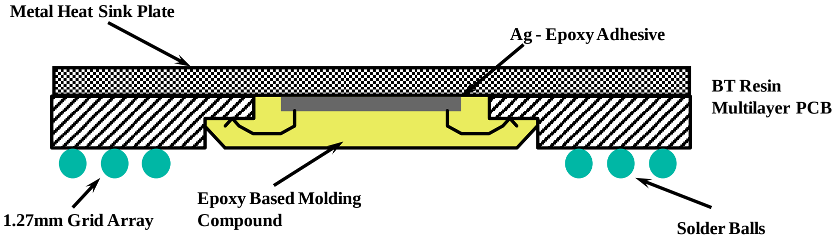












Plastic-Encapsulated Microcircuits

- Die is mounted on a lead frame (A42 or Cu).
- Bonds are made by.
  - Wirebond: Au, moving to Cu in early 2000's.
  - TAB: Tape-Automated Bonding.
  - C4: Controlled Collapse Chip Connect.
- Assembly is encapsulated in molding compound.
  - Molding compound is in direct contact with die, wire bonds, etc.
- External leads are trimmed and solder plated.

Alloy 42
Fe 58% Ni 42% alloy
with CTE matching Si.

Molding Compounds

- MC is thermoset (curing) epoxy, typically novolac.
  - Cures at ~ 170-180°C.
  - Silica "filler" controls CTE and increases thermal conductivity.
  - MCs are (now) free of ionic contaminants.
- Glass Transition ~ 140°C.
- Moisture properties of MC:
  - Permeable to moisture.
  - Absorbs moisture. "Hygroscopic."

Note distinction between thermo*set* and thermo*plastic*.

Molding Compound Properties

- At the glass transition (> 140 °C)..

MC strength decreases

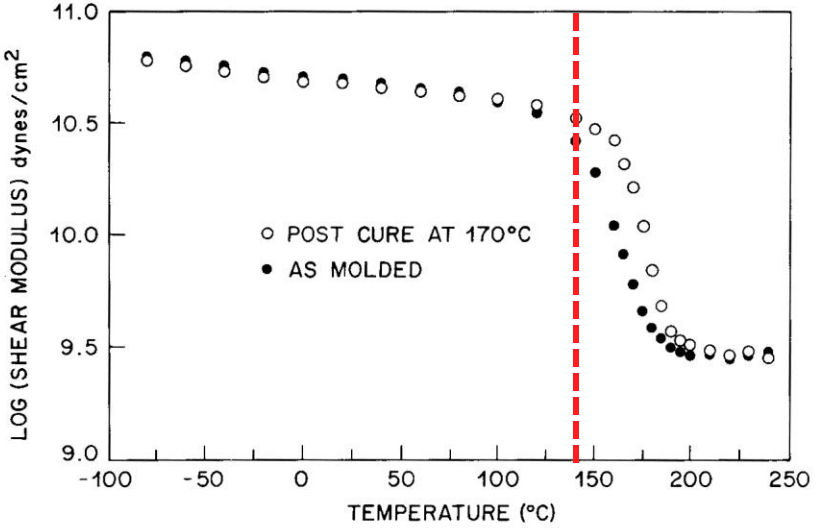


FIGURE 4-16 Shear modulus versus temperature data for an epoxy molding compound. Data show the effect of postcure on the thermomechanical properties. Frequency is 1 rad/sec.

CTE increases

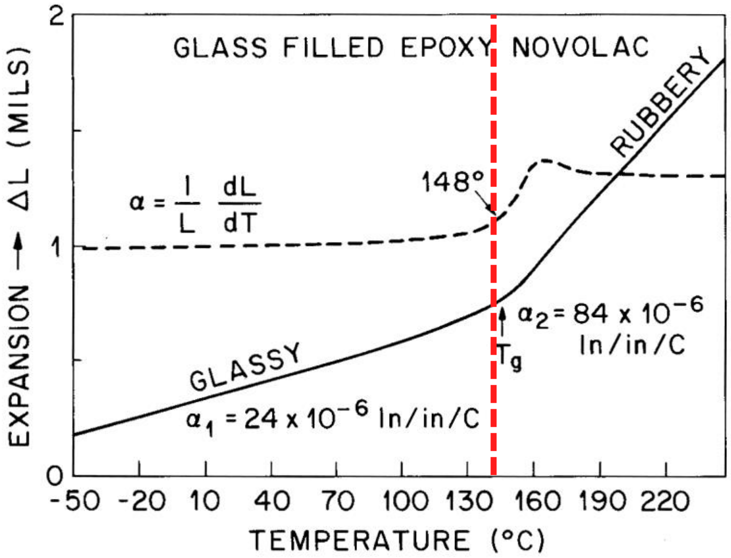


FIGURE 4-1 A plot of expansion versus temperature for an epoxy molding compound. The dashed line is the temperature derivative of expansion, which is defined as the coefficient of thermal expansion. Note the higher CTE above the glass transition temperature.

L. T. Manzione "Plastic Packaging of Microelectronic Devices," Van Nostrand Reinhold 1990.

Molding Compound Properties, ct'd

- Molding compound strongly absorbs water.
  - *Saturation* uptake is proportional to RH, and *independent of temperature.*
  - *Rate* of uptake *depends strongly on temperature*.

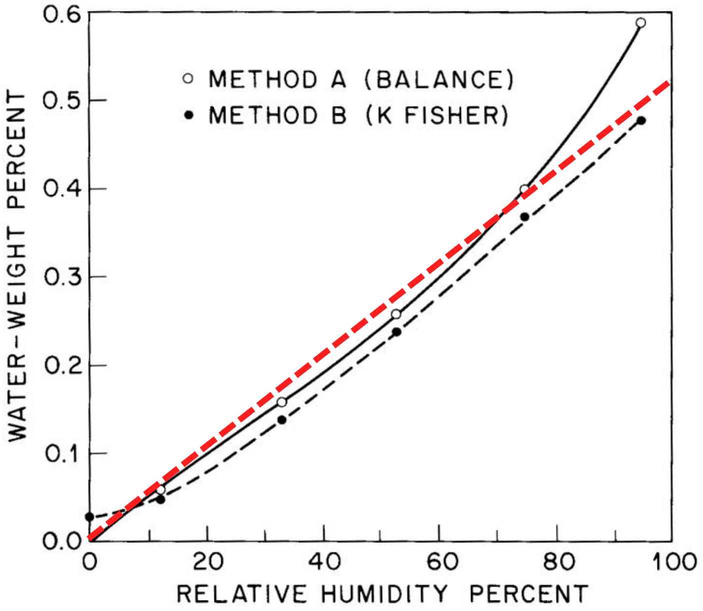


FIGURE 4-24 Plot of water uptake of epoxy molding compound preforms as a function of relative humidity of the conditioning atmosphere after three weeks of exposure at room temperature. K. Fisher is a hydrolysis technique for measuring water content. (Data of D. J. Boyle, J. T. Ryan and H. E. Bair, AT&T Bell Laboratories.)

L. T. Manzione "Plastic Packaging of Microelectronic Devices," Van Nostrand Reinhold 1990.

Key Material Properties

- Material properties which drive temperature cycling-induced failure mechanisms.

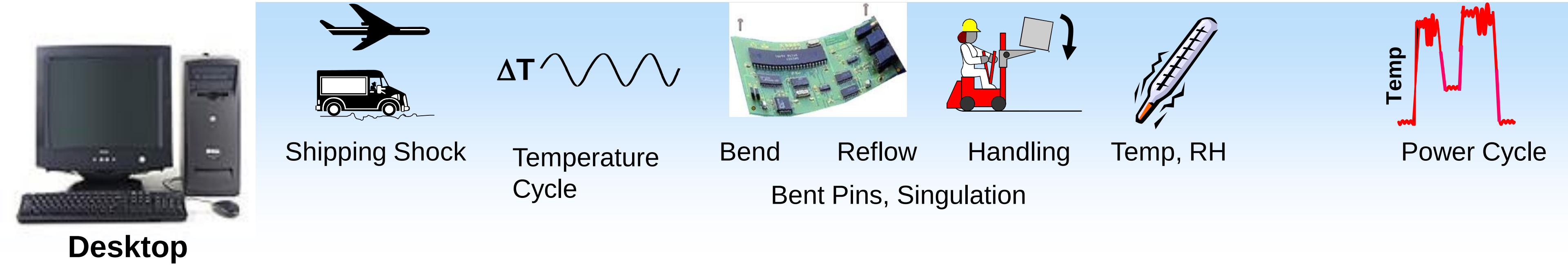
Material	Thermal Coeffic't of Expansion (ppm/°C) **"TCE"**	Young's Modulus (GPa)	Thermal Conductivity (W/m °C)
Copper	17	119	398
Alloy 42	5 Match!	145	15 Low!
Silicon	3	131	157
Molding Compound	21	18	0.6
Alumina	6.5	25	25
PC Board	15-17	11	25

Outline

- Plastic Package Technology
● Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - Moisture
  - Thermal
  - Thermo-mechanical

Life of an Integrated Circuit

Assembly → **Shipping** → **Storage** → **OEM/ODM Assembly** → **End-user Environment**



Desktop

Shipping Shock

Temperature Cycle

Bend

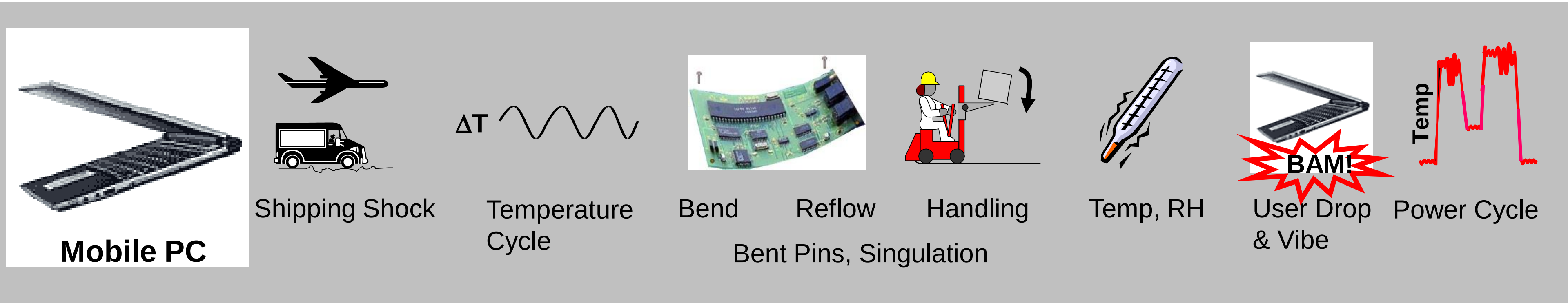
Reflow

Handling

Temp, RH

Power Cycle

Bent Pins, Singulation



Mobile PC

Shipping Shock

Temperature Cycle

Bend

Reflow

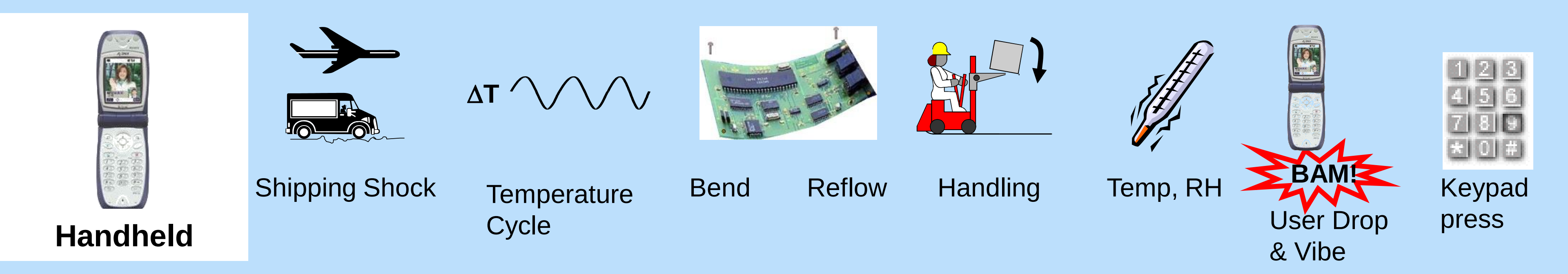
Handling

Temp, RH

User Drop & Vibe

Power Cycle

Bent Pins, Singulation



Handheld

Shipping Shock

Temperature Cycle

Bend

Reflow

Handling

Temp, RH

User Drop & Vibe

Keypad press

Slide by Scott C. Johnson.

Stress/Test Flow

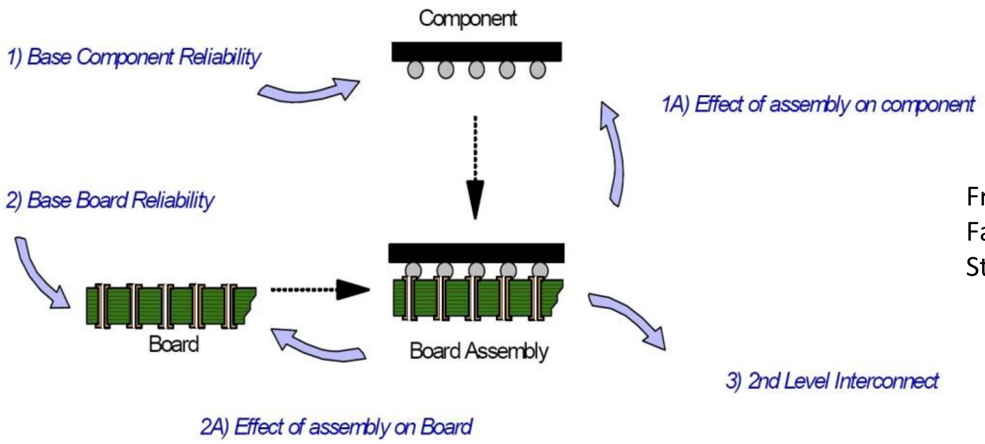


Figure 1 — Levels of Assembly - Interaction of packaging technical concerns

From: **JEP150** “Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components” (JEDEC)

Preconditioning

Simulate shipping, storing, and OEM board mounting process.

Environmental Stress

Simulate in-service end use conditions.

Electrical Test, Failure Analysis

Determine pass/fail. Diagnose failures.

Industry Reliability Standards

- International
  - ISO International Standard Organization
  - IEC International Electrotechnical Commission
- Europe
  - CEN, CENELEC Comite Européen de Normalisation Électrotechnique
- Japan
  - JIS Japanese Industrial Standard, EIAJ
- US
  - MIL (US Department of Defense), **EIA/JEDEC**

For US commercial products JEDEC standards have mostly superseded MIL standards.

Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Preconditioning

- Preconditioning simulates board assembly.
- Specified by
  - **JESD22-A113F** Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing.
  - IPC/JEDEC **J-STD-020D.01** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

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J-STD-020D.01

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http://www.jedec.org/

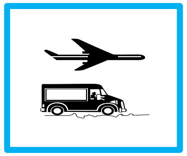
Free downloads, registration required.

Preconditioning

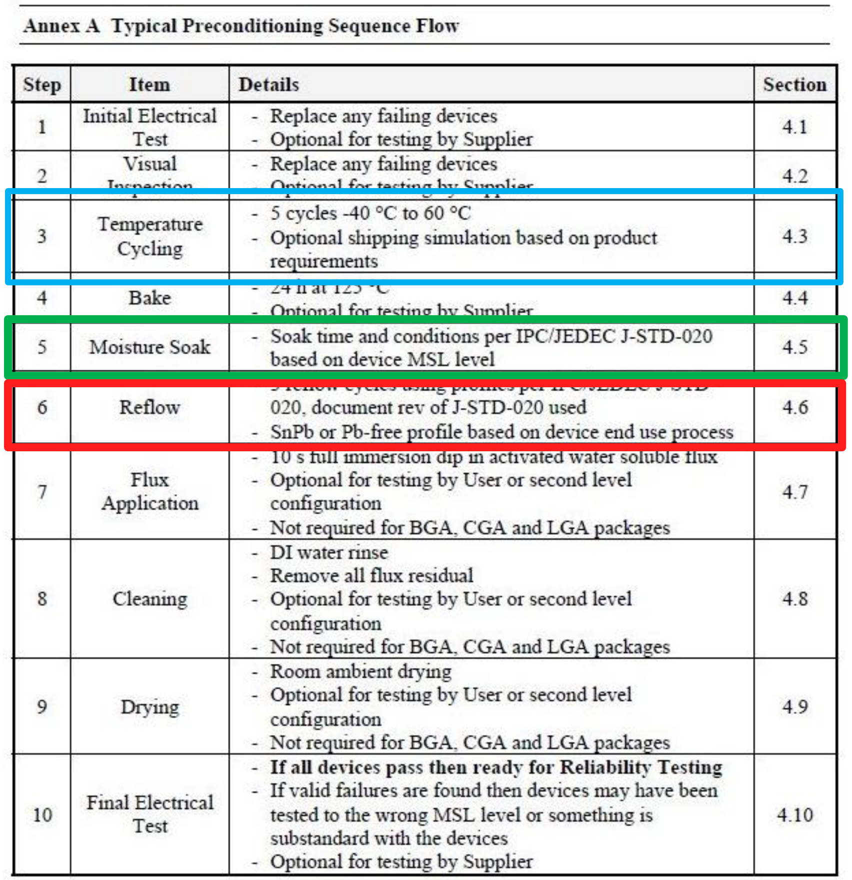
Environmental Stress

Electrical Test, Failure Analysis

Preconditioning Flow



JESD22-A113F



Annex A Typical Preconditioning Sequence Flow

Step	Item	Details	Section
1	Initial Electrical Test	- Replace any failing devices - Optional for testing by Supplier	4.1
2	Visual Inspection	- Replace any failing devices - Optional for testing by Supplier	4.2
3	Temperature Cycling	- 5 cycles -40 °C to 60 °C - Optional shipping simulation based on product requirements	4.3
4	Bake	- 24 h at 125 °C - Optional for testing by Supplier	4.4
5	Moisture Soak	- Soak time and conditions per IPC/JEDEC J-STD-020 based on device MSL level	4.5
6	Reflow	- 3 reflow cycles using profiles per IPC/JEDEC J-STD-020, document rev of J-STD-020 used - SnPb or Pb-free profile based on device end use process	4.6
7	Flux Application	- 10 s full immersion dip in activated water soluble flux - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.7
8	Cleaning	- DI water rinse - Remove all flux residual - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.8
9	Drying	- Room ambient drying - Optional for testing by User or second level configuration - Not required for BGA, CGA and LGA packages	4.9
10	Final Electrical Test	- **If all devices pass then ready for Reliability Testing** - If valid failures are found then devices may have been tested to the wrong MSL level or something is substandard with the devices - Optional for testing by Supplier	4.10

IPC/JEDEC J-STD-020D.01

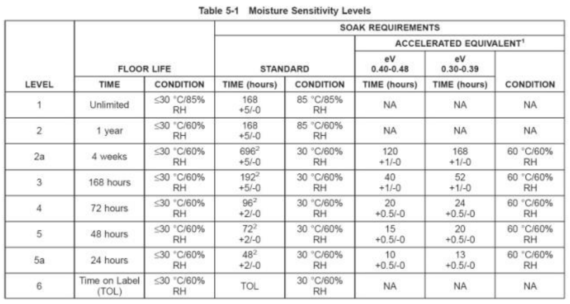
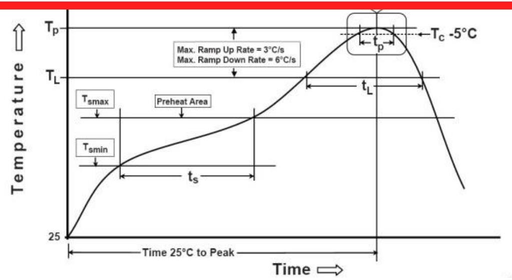


Table 5-1 Moisture Sensitivity Levels

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			STANDARD		ACCELERATED EQUIVALENT[1]		
					eV 0.40-0.48	eV 0.30-0.39	
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696[2] +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192[2] +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96[2] +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72[2] +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48[2] +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA



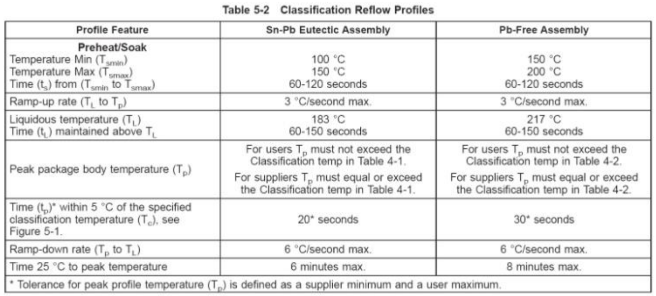
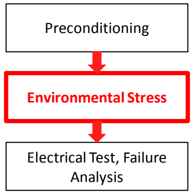


Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

Slide 50


Preconditioning

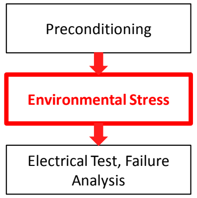
Environmental Stress

Electrical Test, Failure Analysis

Environmental Test

- Stress-based testing (traditional).

  To keep things simple, we'll follow this approach.
  - Standards: **JESD47**, MIL-STD-883.
  - Pro:
    - Well-established standards. Lots of historical data. Good for comparisons.
    - Little information about mechanism or use is required.
  - Con:
    - Overstress: May foreclose a technology.
    - Understress: Misses a mechanism.
      - May not accurately reflect a use environment.
- Knowledge-based testing.
  - Risk assessment of Use and Mechanism guides test.


Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

JESD47 Example

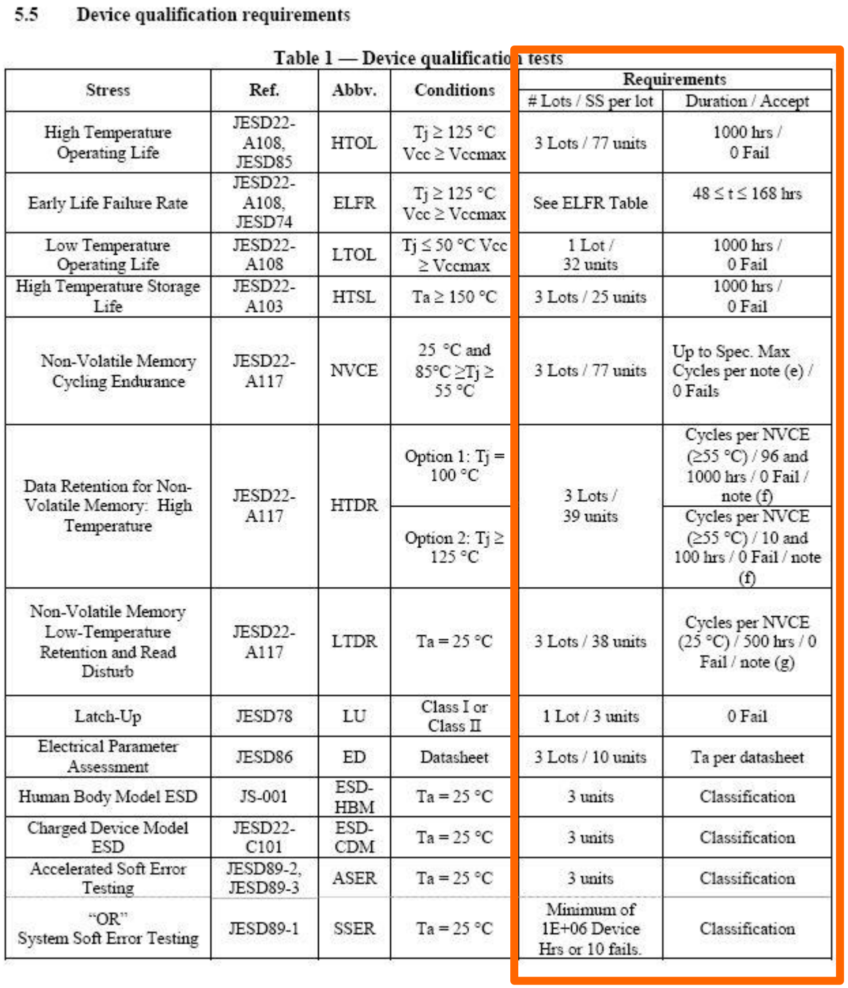

5.5 **Device qualification requirements**

Table 1 — Device qualificatio tests

Stress	Ref.	Abbv.	Conditions	Requirements	
				# Lots / SS per lot	Duration / Accept
High Temperature Operating Life	JESD22-A108, JESD85	HTOL	Tj ≥ 125 °C Vcc ≥ Vccmax	3 Lots / 77 units	1000 hrs / 0 Fail
Early Life Failure Rate	JESD22-A108, JESD74	ELFR	Tj ≥ 125 °C Vcc ≥ Vccmax	See ELFR Table	48 ≤ t ≤ 168 hrs
Low Temperature Operating Life	JESD22-A108	LTOL	Tj ≤ 50 °C Vcc ≥ Vccmax	1 Lot / 32 units	1000 hrs / 0 Fail
High Temperature Storage Life	JESD22-A103	HTSL	Ta ≥ 150 °C	3 Lots / 25 units	1000 hrs / 0 Fail
Non-Volatile Memory Cycling Endurance	JESD22-A117	NVCE	25 °C and 85°C ≥Tj ≥ 55 °C	3 Lots / 77 units	Up to Spec. Max Cycles per note (e) / 0 Fails
Data Retention for Non-Volatile Memory: High Temperature	JESD22-A117	HTDR	Option 1: Tj = 100 °C	3 Lots / 39 units	Cycles per NVCE (≥55 °C) / 96 and 1000 hrs / 0 Fail / note (f)
			Option 2: Tj ≥ 125 °C		Cycles per NVCE (≥55 °C) / 10 and 100 hrs / 0 Fail / note (f)
Non-Volatile Memory Low-Temperature Retention and Read Disturb	JESD22-A117	LTDR	Ta = 25 °C	3 Lots / 38 units	Cycles per NVCE (25 °C) / 500 hrs / 0 Fail / note (g)
Latch-Up	JESD78	LU	Class I or Class II	1 Lot / 3 units	0 Fail
Electrical Parameter Assessment	JESD86	ED	Datasheet	3 Lots / 10 units	Ta per datasheet
Human Body Model ESD	JS-001	ESD-HBM	Ta = 25 °C	3 units	Classification
Charged Device Model ESD	JESD22-C101	ESD-CDM	Ta = 25 °C	3 units	Classification
Accelerated Soft Error Testing	JESD89-2, JESD89-3	ASER	Ta = 25 °C	3 units	Classification
"OR" System Soft Error Testing	JESD89-1	SSER	Ta = 25 °C	Minimum of 1E+06 Device Hrs or 10 fails.	Classification

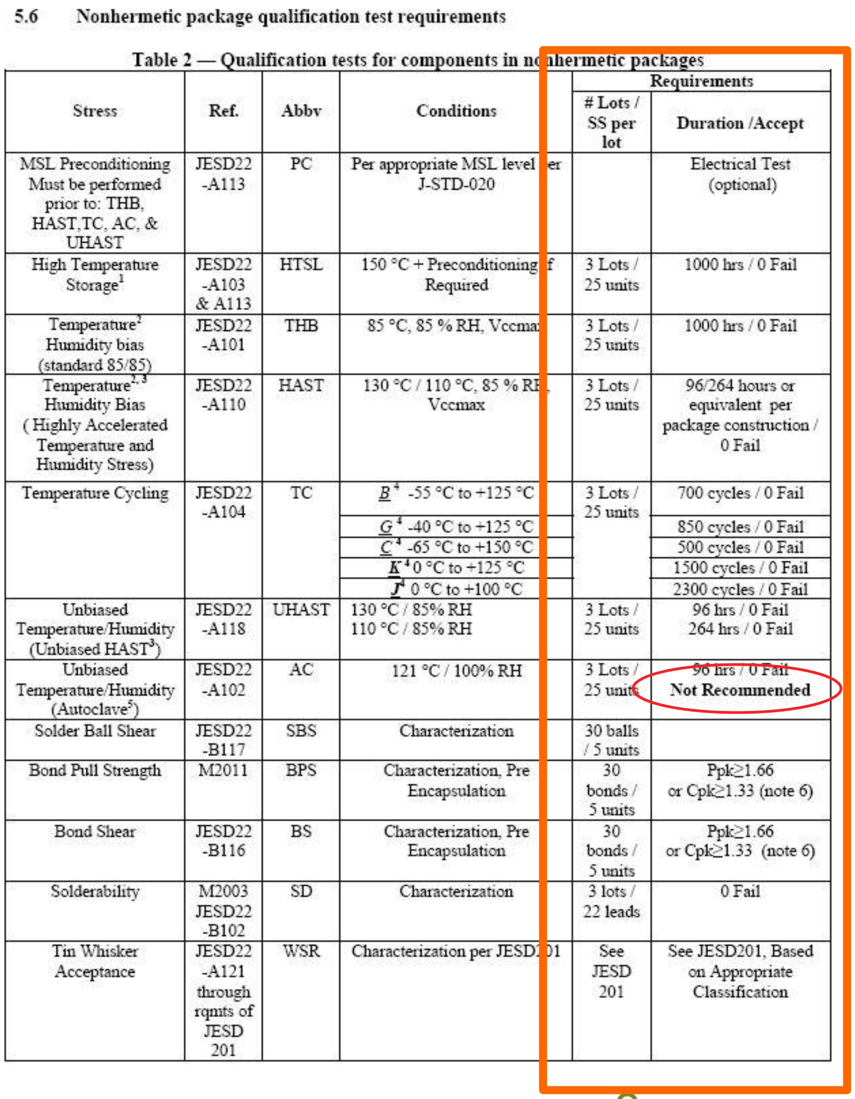
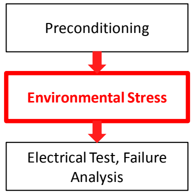

5.6 **Nonhermetic package qualification test requirements**

Table 2 — Qualification tests for components in no hermetic packages

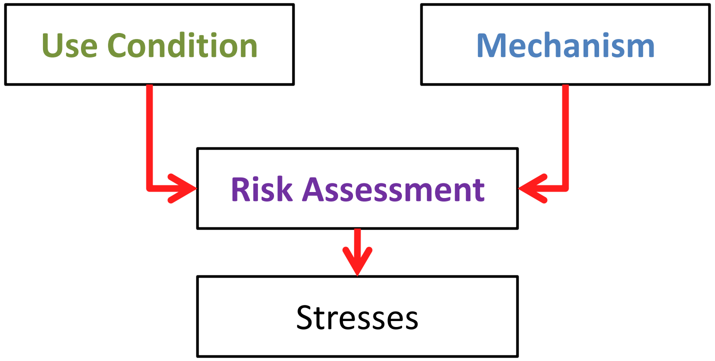
Stress	Ref.	Abbv	Conditions	Requirements	
				# Lots / SS per lot	Duration /Accept
MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 -A113	PC	Per appropriate MSL level er J-STD-020		Electrical Test (optional)
High Temperature Storage^1	JESD22 -A103 & A113	HTSL	150 °C + Preconditioning f Required	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature^2 Humidity bias (standard 85/85)	JESD22 -A101	THB	85 °C, 85 % RH, Vccmax	3 Lots / 25 units	1000 hrs / 0 Fail
Temperature^{2,3} Humidity Bias (Highly Accelerated Temperature and Humidity Stress)	JESD22 -A110	HAST	130 °C / 110 °C, 85 % RH, Vccmax	3 Lots / 25 units	96/264 hours or equivalent per package construction / 0 Fail
Temperature Cycling	JESD22 -A104	TC	B^4 -55 °C to +125 °C	3 Lots / 25 units	700 cycles / 0 Fail
			G^4 -40 °C to +125 °C		850 cycles / 0 Fail
			C^4 -65 °C to +150 °C		500 cycles / 0 Fail
			K^4 0 °C to +125 °C		1500 cycles / 0 Fail
			J^4 0 °C to +100 °C		2300 cycles / 0 Fail
Unbiased Temperature/Humidity (Unbiased HAST^3)	JESD22 -A118	UHAST	130 °C / 85% RH 110 °C / 85% RH	3 Lots / 25 units	96 hrs / 0 Fail 264 hrs / 0 Fail
Unbiased Temperature/Humidity (Autoclave^5)	JESD22 -A102	AC	121 °C / 100% RH	3 Lots / 25 units	~~96 hrs / 0 Fail~~ **Not Recommended**
Solder Ball Shear	JESD22 -B117	SBS	Characterization	30 balls / 5 units	
Bond Pull Strength	M2011	BPS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Bond Shear	JESD22 -B116	BS	Characterization, Pre Encapsulation	30 bonds / 5 units	Ppk≥1.66 or Cpk≥1.33 (note 6)
Solderability	M2003 JESD22 -B102	SD	Characterization	3 lots / 22 leads	0 Fail
Tin Whisker Acceptance	JESD22 -A121 through rqmts of JESD 201	WSR	Characterization per JESD 01	See JESD 201	See JESD201, Based on Appropriate Classification

Note: TS (**JESD22-A106**) and AC (Steam) (**JESD22-A102**) are not recommended. *Very* different from use.

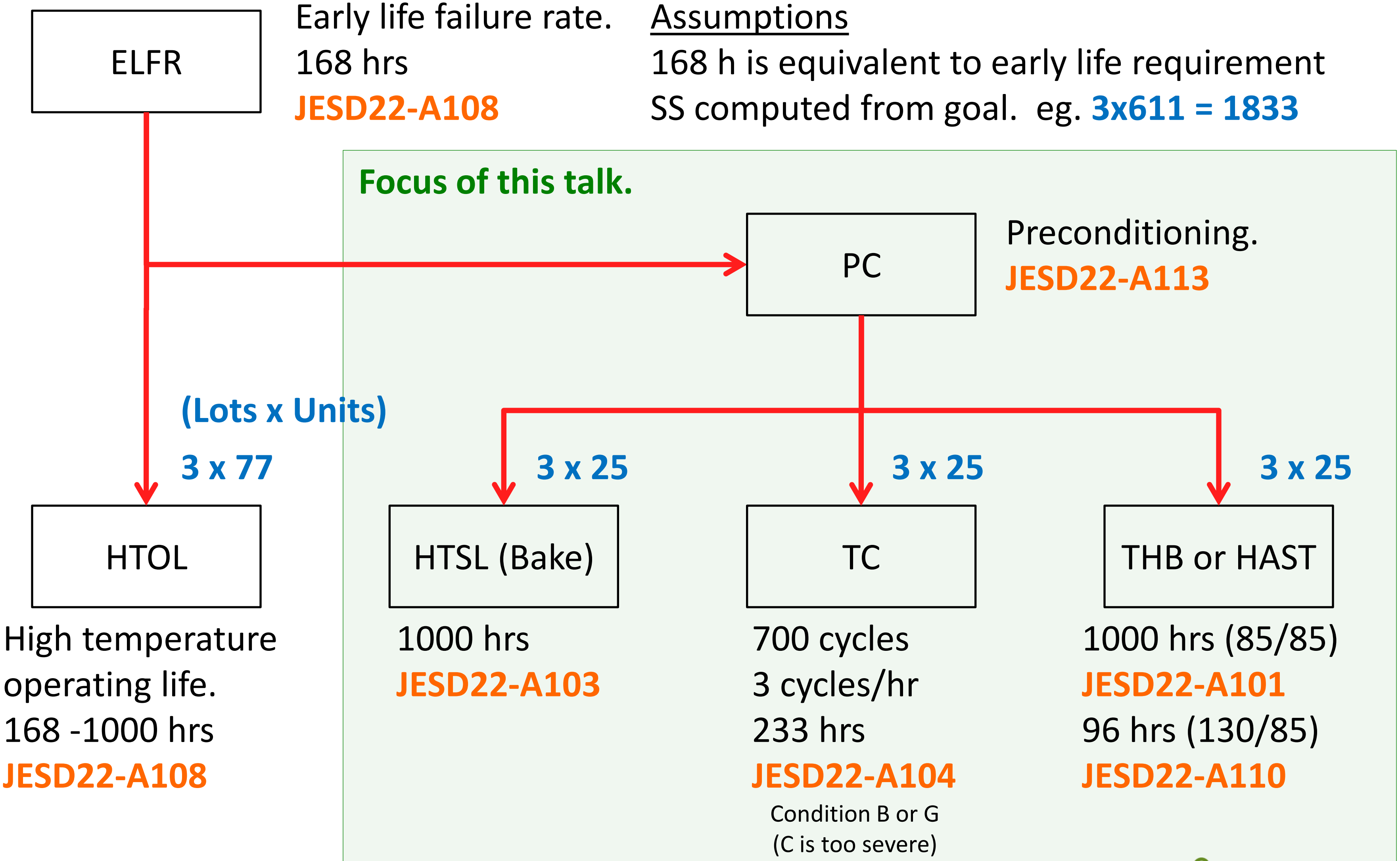


Knowledge-Based Test

- Knowledge-Based Testing
  - Stress depends on knowledge of **use conditions** and **mechanisms**.
  - **Risk assessment**, using methods
    - JEDEC: **JESD94**, **JEP143**, **JEP148**
    - **Sematech**: “Understanding and Developing Knowledge-based Qualifications of Silicon Devices” **#04024492A-TR**
  - Pro:
    - Stresses fit the product and its use. May make a product feasible.
  - Con:
    - Easy to miss mechanisms in new technologies and overlook use conditions in new applications.
    - Tempting to misapply to “uprate” devices, relax requirements.



Example Stress Flow



ELFR

Early life failure rate.
168 hrs
JESD22-A108

Assumptions
168 h is equivalent to early life requirement
SS computed from goal. eg. 3x611 = 1833

Focus of this talk.

PC

Preconditioning.
JESD22-A113

(Lots x Units)

3 x 77

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

3 x 25

HTSL (Bake)

1000 hrs
JESD22-A103

3 x 25

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

3 x 25

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Outline

- Plastic Package Technology
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- Mechanisms
  - ● Moisture-mechanical
  - Moisture
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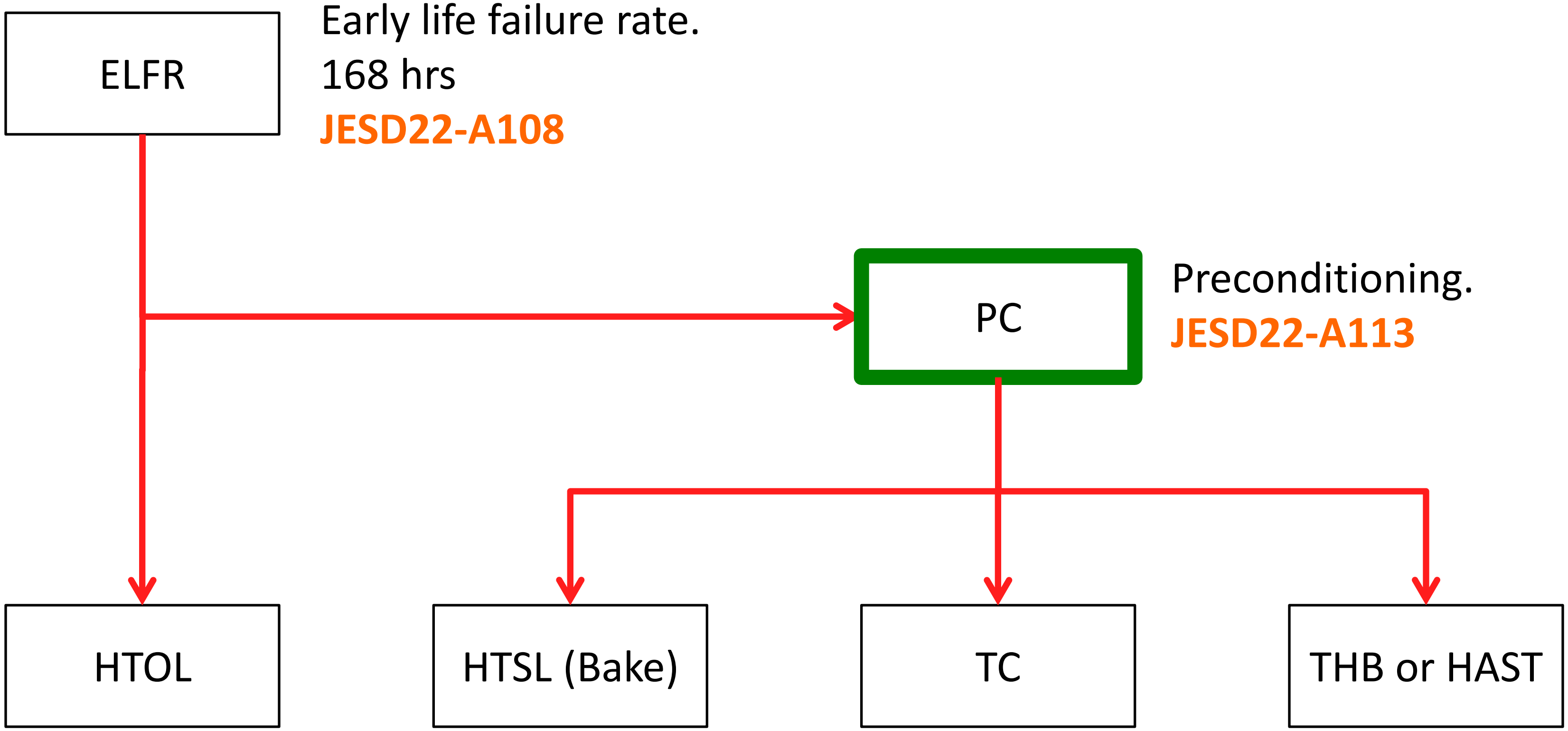
Popcorn Mechanism



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

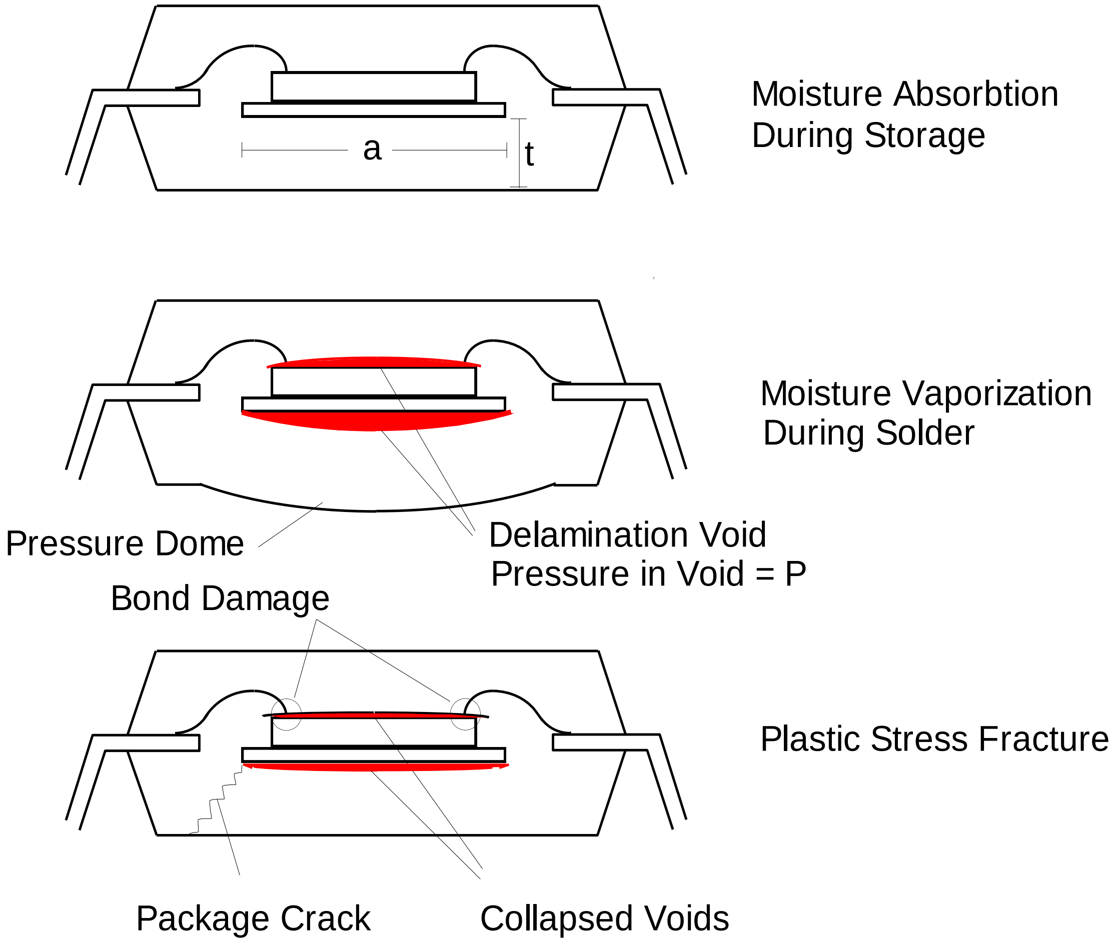
TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Popcorn Mechanism



Moisture Absorbtion
During Storage

Moisture Vaporization
During Solder

Pressure Dome

Delamination Void
Pressure in Void = P

Bond Damage

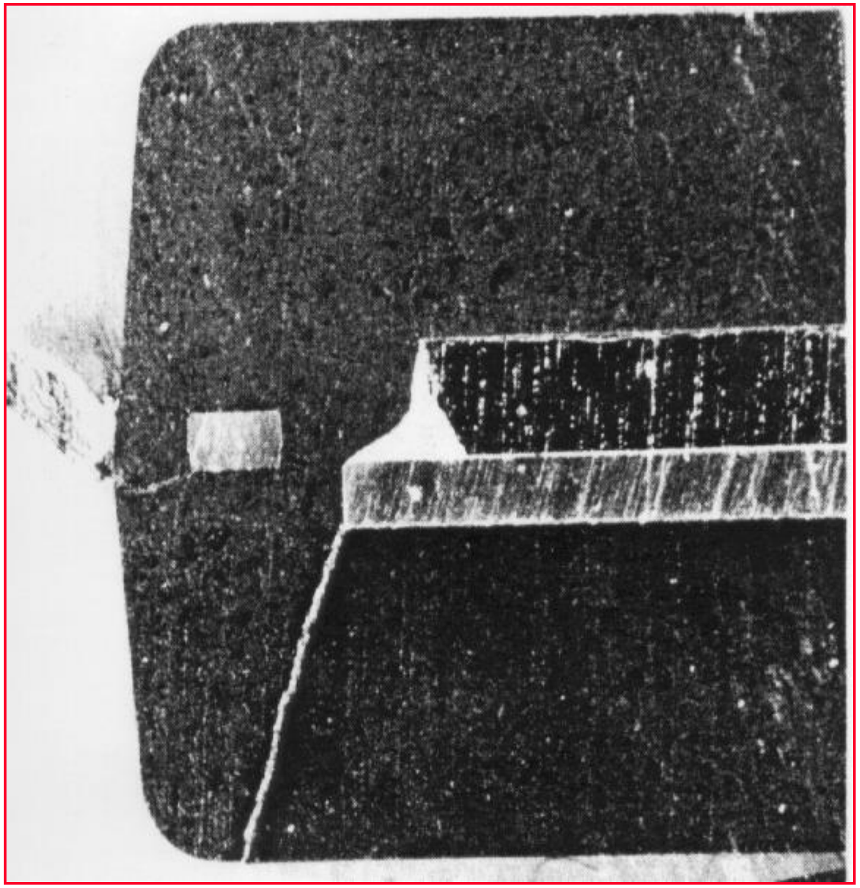
Plastic Stress Fracture

Package Crack

Collapsed Voids

Plastic package cracking due to “popcorn” effect during solder reflow

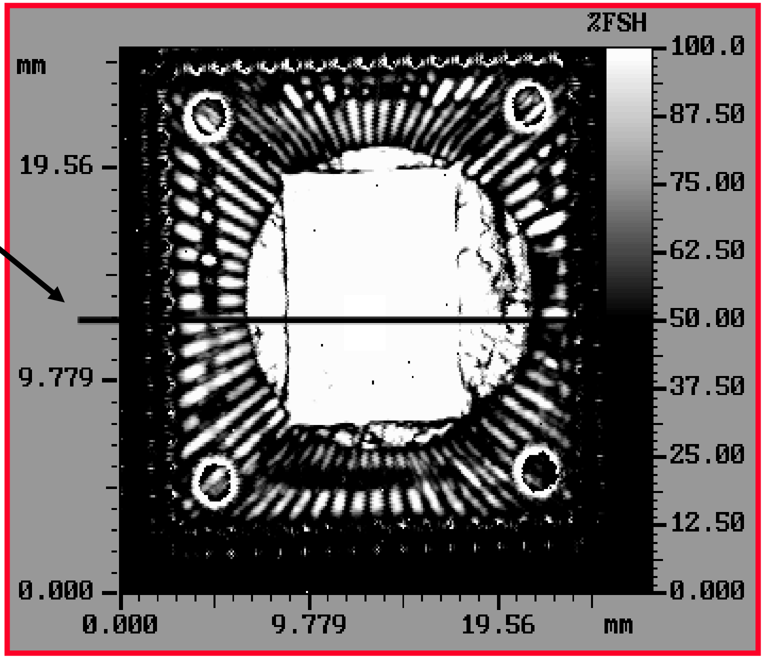
Popcorn Damage



Plastic package cracking due to “popcorn” effect during solder reflow

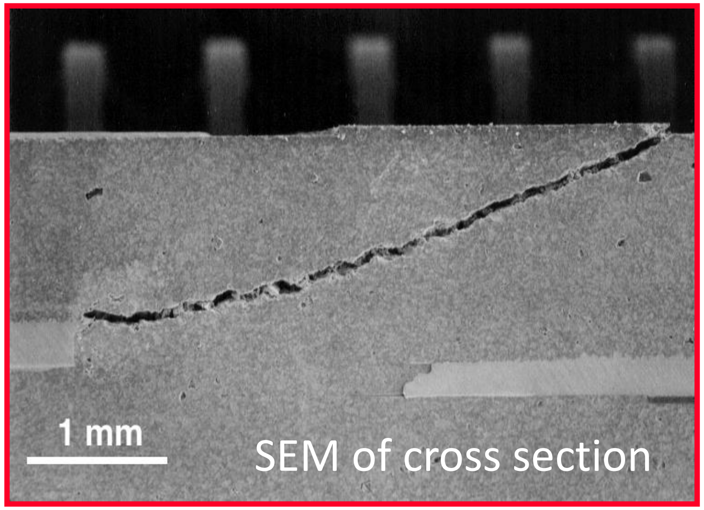
Popcorn Damage

B-Scan line

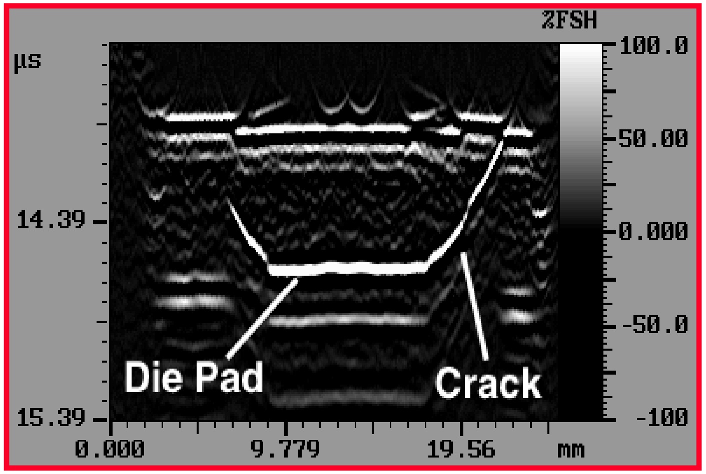


Pulse-echo acoustic image through back of 68PLCC that developed popcorn cracks during solder reflow

Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, in "Characterization of Integrated Circuit Packaging Materials", Butterworth-Heinemann, 79-96, 1993.

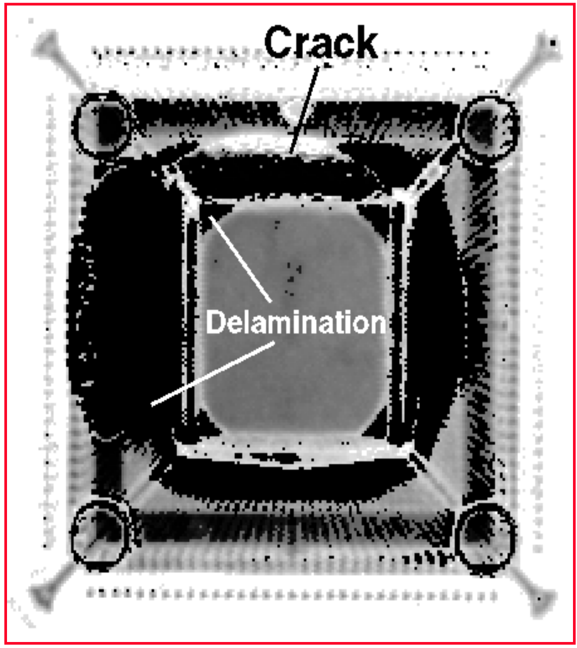


SEM of cross section

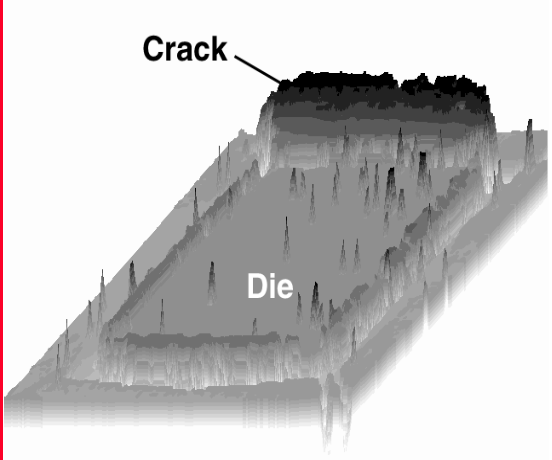


Acoustic B-scan

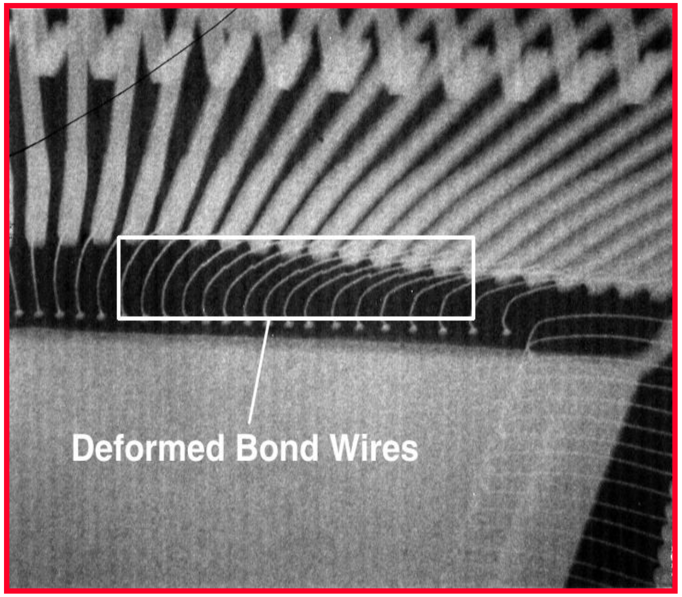
Popcorn Damage



Pulse-echo acoustic image through top (delamination in black)



Acoustic time-of-flight image indicating package crack



Real-time x-ray image showing deformation in wires where they intersect the crack

132 lead PQFP which was damaged during solder reflow.

Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, in "Characterization of Integrated Circuit Packaging Materials", Butterwoth-Heinemann, 79-96, 1993.

Factors Affecting Popcorning

- Molding compound moisture content
  - Temperature/humidity/time exposure before solder.
- Package geometry
  - Dimensions of die paddle.
  - Thickness of molding compound under paddle.
- Peak temperature reached during soldering.
- Adhesion of molding compound to die and/or lead frame.

Not on this list: Pre-existing voids in the plastic package.

H_2O Diffusion/Absorption in MC

Diffusion Coefficient:

$$D = D_0 \exp\left(-\frac{Q_d}{kT} \right)$$

$$D_0 = 4.7 \times 10^{-5} \text{ m}^2/\text{sec} \quad Q_d = 0.50 \text{ eV}$$

Saturation Coefficient:

Source: [Kitano, et al IRPS 1988]

$$S = S_0 \exp\left(\frac{Q_s}{kT} \right)$$

$$S_0 = 2.76 \times 10^4 \text{ mole/m}^3\text{Pa} \quad Q_s = 0.40 \text{ eV}$$

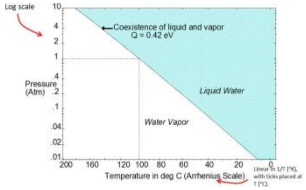
Henry's Law:

$$M_{\text{sat}} = PS = H\underbrace{P_{\text{sat}}}S$$

H_2O vapor pressure.

Clausius-Clapeyron (approximate):

$$P_{sat} \simeq P_\infty \exp\left(-\frac{Q_p}{kT} \right)$$



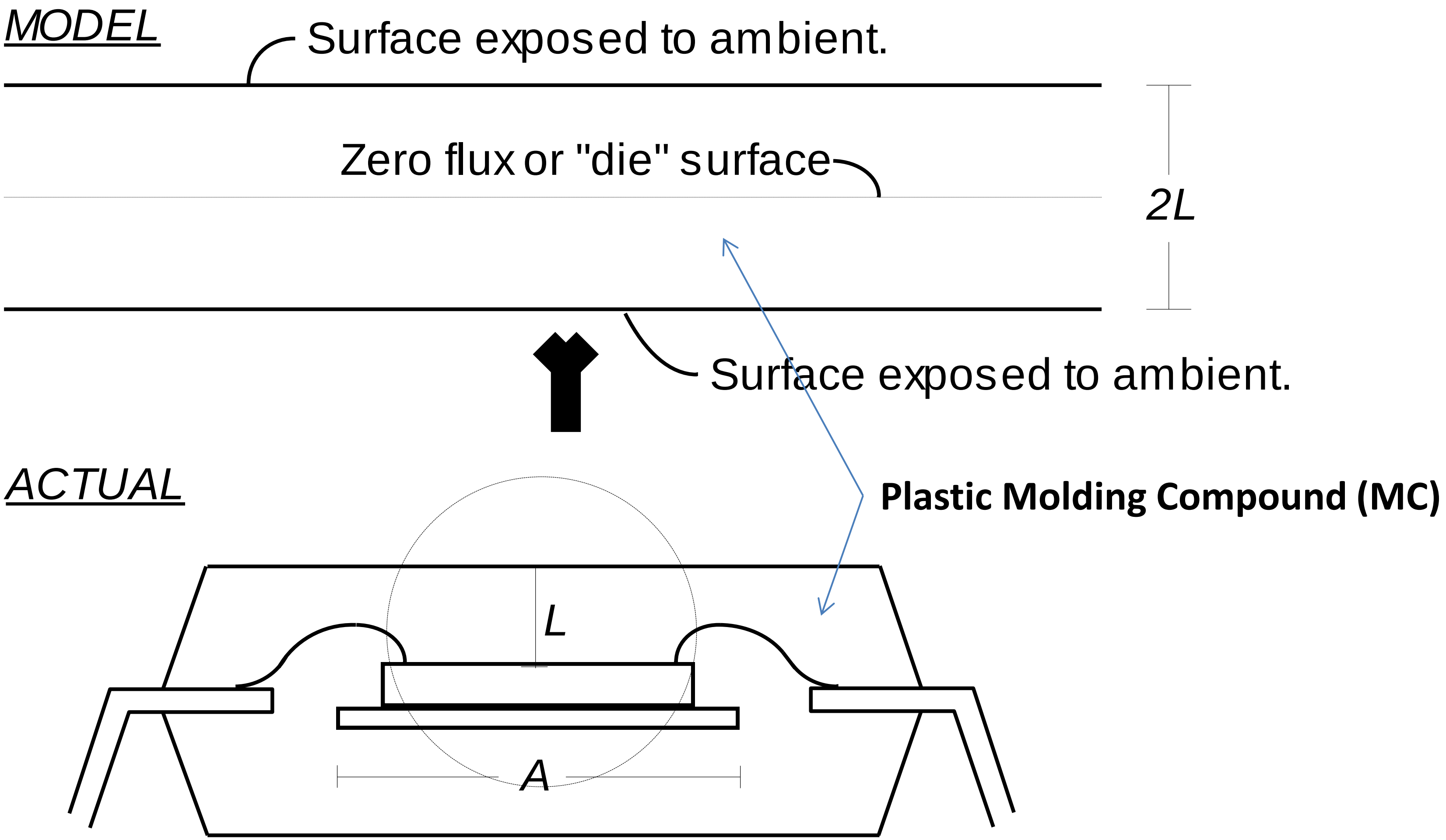
$$P_\infty = 4.58 \times 10^5 \text{ Atm}, \ Q_p = 0.42 \text{ eV}$$

Key Observation: Saturated moisture content of molding compound is nearly independent of temperature, and is proportional to RH.

$$M_{sat} = HP_\infty S_0 \exp\left[\frac{(Q_s - Q_p)}{kT} \right] \qquad Q_s - Q_p = -0.02 \text{ eV}$$

Nearly zero!

H_2O Diffusion/Absorption in MC



MODEL

Surface exposed to ambient.

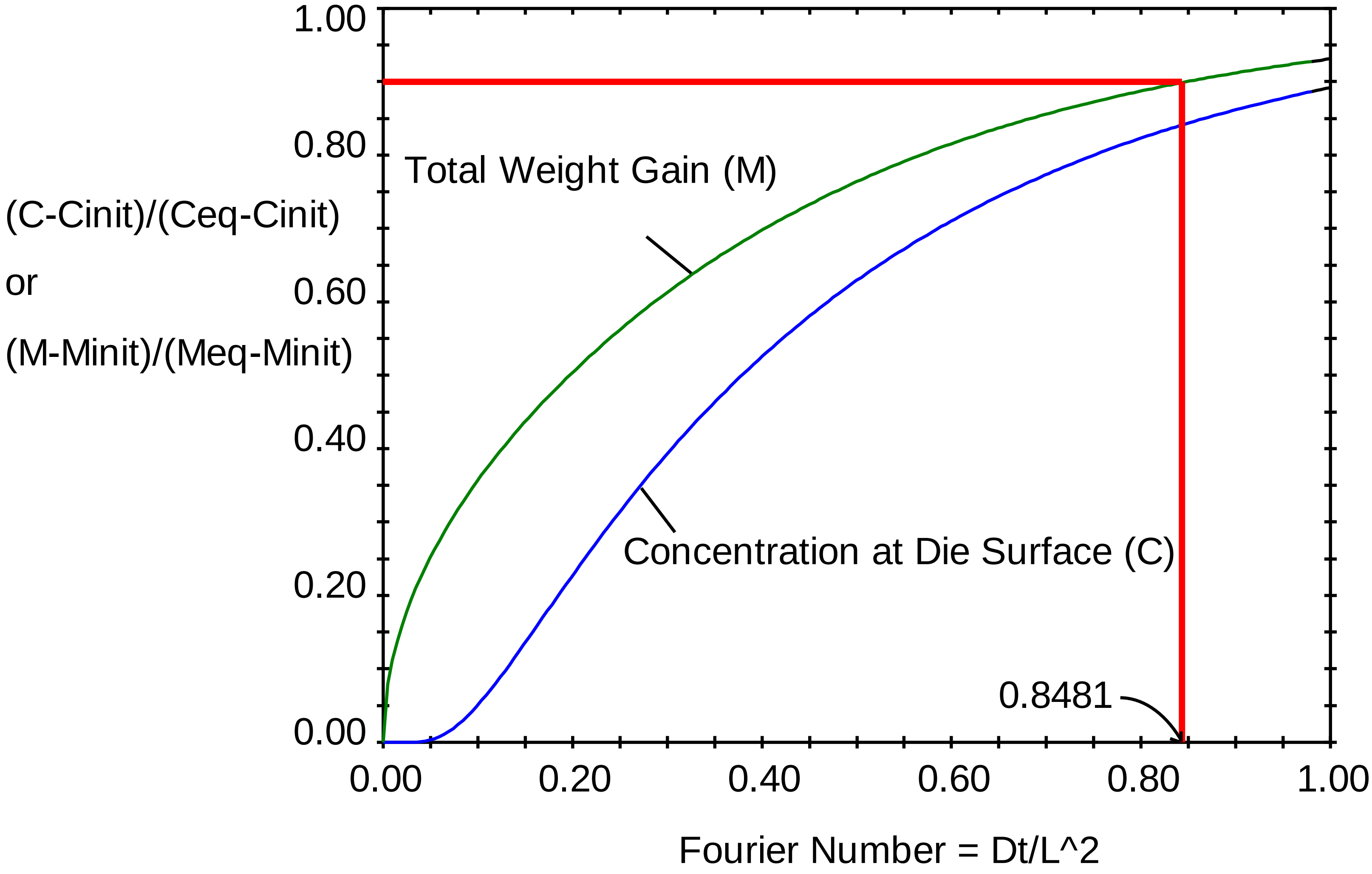
Zero flux or "die" surface

Surface exposed to ambient.

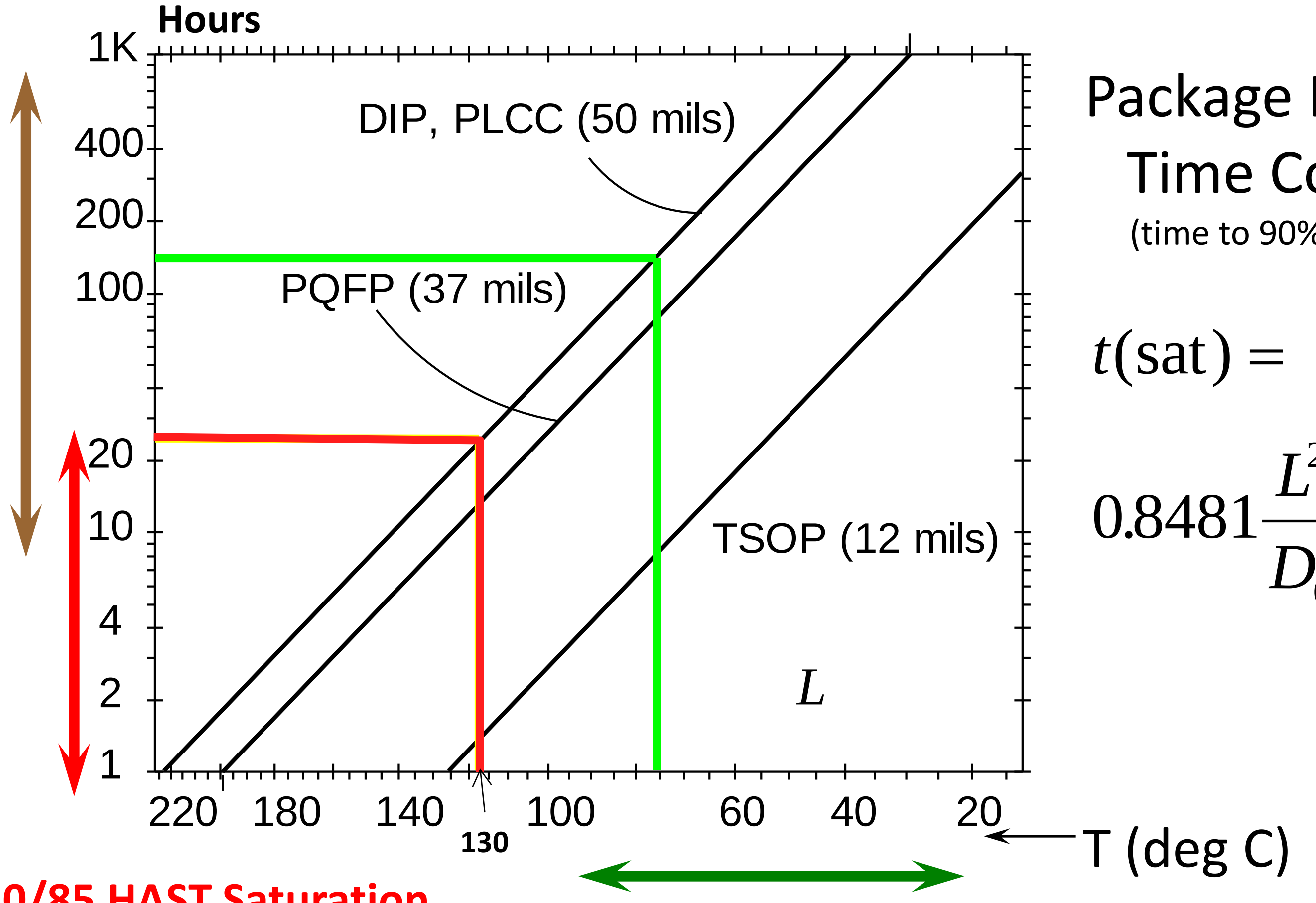
ACTUAL

Plastic Molding Compound (MC)

H_2O Diffusion/Absorption in MC



Time to 90% Saturation After Humidity Step



Typical 130/85 HAST Saturation Times

Normal Operating Range

Package Moisture Time Constant

(time to 90% saturation)

$$t(\text{sat}) =$$

$$0.8481\frac{L^2}{D_0}\exp\left(\frac{Q_d}{kT_{mc}}\right)$$

Popcorn Model

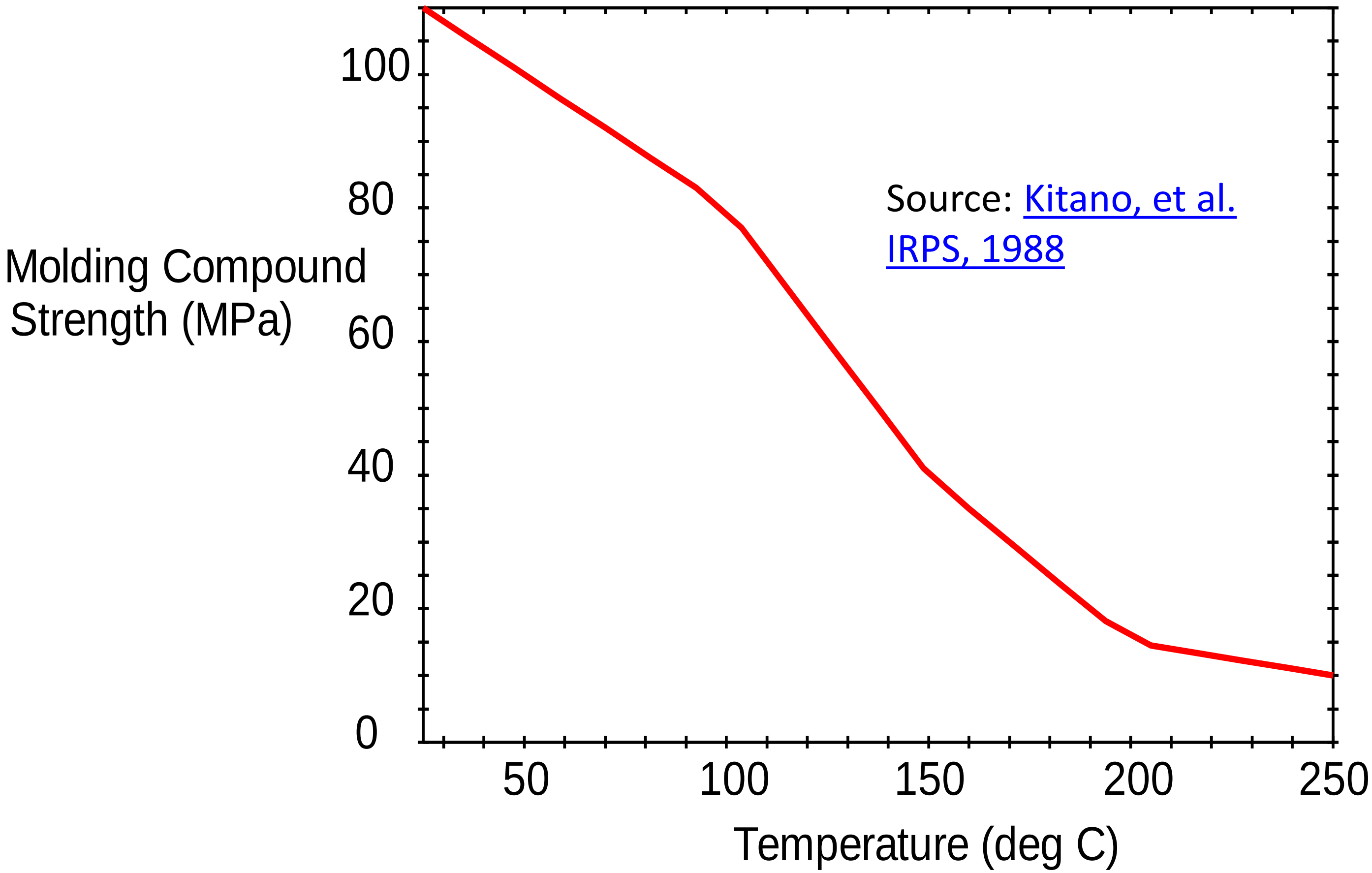
- A crack propagates to the surface when maximum bending stress σ_{max} exceeds a fracture stress characteristic of the molding compound

$$\sigma_{max} > \sigma_{crit}(T_{reflow})$$

- σ_{crit} depends on MC formulation, and on temperature (see next slide).

Source: I. Fukuzawa, et. al. "Moisture Resistance Degradation of Plastic LSIs by Reflow Solder Process," IRPS, 1988

Popcorn Model, σ_{crit}



Source: Kitano, et al. IRPS, 1988

σ_{crit} is proportional to molding compound strength.

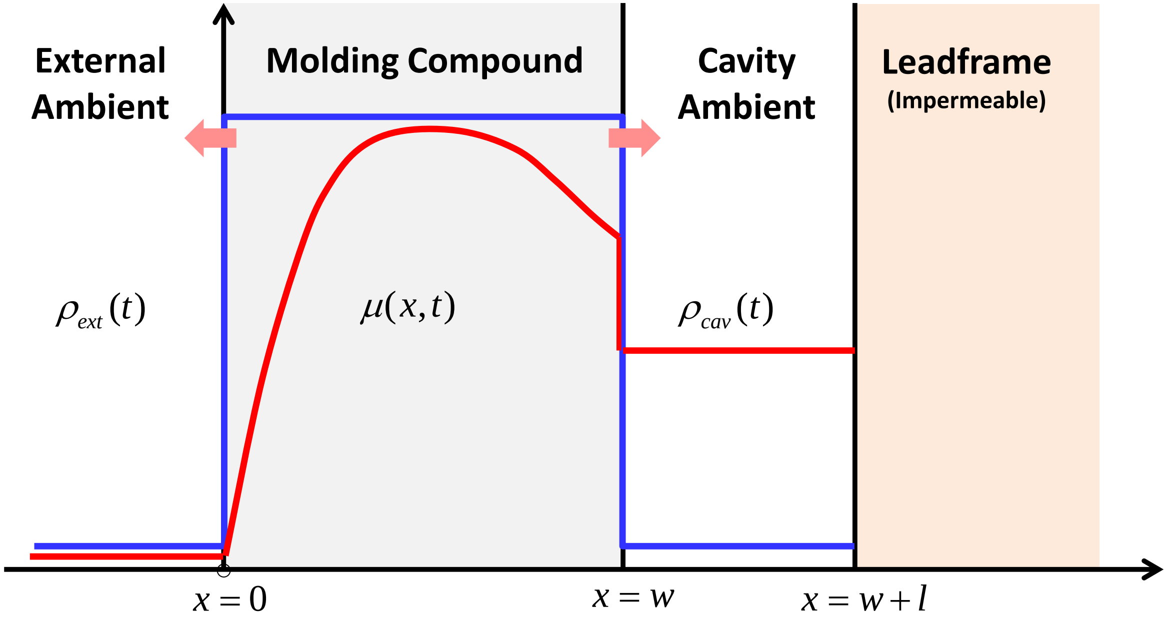
Popcorn Model, σ_{max}

- Maximum bending stress occurs at center of long edge of die and is given by:

$$\sigma_{max} = 6 \times K \times \left(\frac{a}{t}\right)^2 P$$

  - *a* is the length of the die edge.
  - *t* is the thickness of the molding compound over the die.
  - *K* is a geometrical factor (K = 0.05 for square pad).
  - *P* is the internal pressure. Depends on
    - Moisture content of molding compound.
      - Depends in turn on RH and T of previous soak ambient.
    - Peak temperature during reflow.

Popcorn Model, Internal Pressure



$\mu(x,t) \equiv$ Concentration Profile in Molding Cpd.

$\rho_{\text{cav}}(t) \equiv$ Moisture Concentration in Cavity

$P_{\text{cav}}(t) = R \times T_1 \times \rho_{\text{cav}}(t) =$ Cavity Pressure

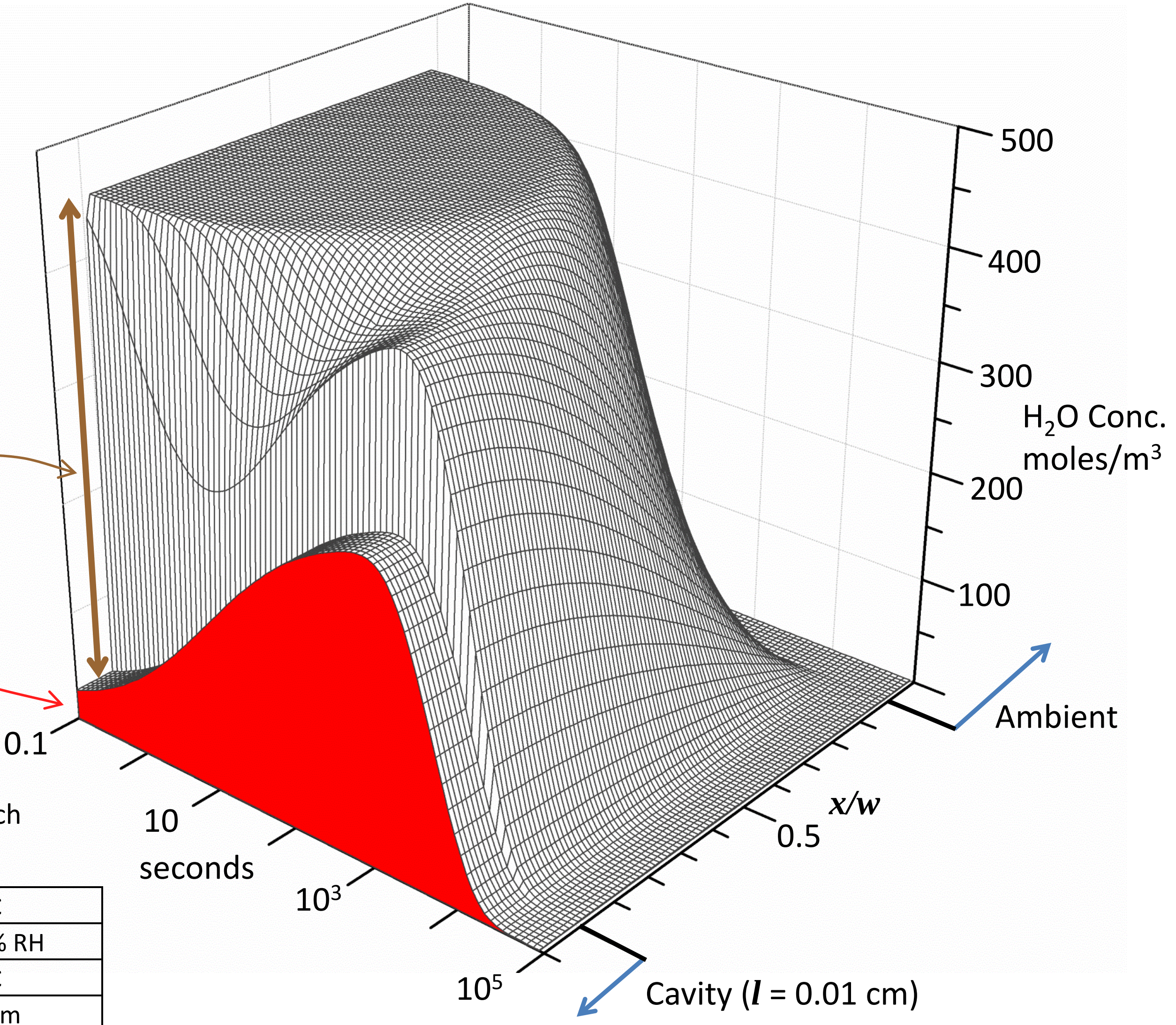
$\mu_0 = H_0 \times P_{sat}(T_0) \times S(T_0) \equiv$ Initial Moisture Conc. In Mold. Cpd.

For $t > 0$ the boundary condition at $x = 0$ is:

$$P_{\text{cav}}(t) = \frac{\mu(0,t)}{S(T_1)}$$

Henry's Law

Popcorn Model, Internal Pressure



Moisture conc. in MC

>> (~ 30x)

Moisture conc. in cavity.

C. G. Shirley, "Popcorn Cavity Pressure," IEEE Transactions on Device and Materials Reliability, Vol. 14, No. 1, pp. 426-431, March 2014

Inputs	T_0	25	C
	H_0	85	% RH
	T_1	215	C
	W_	0.2	cm
	L_	0.01	cm

Popcorn Model, Internal Pressure

$$P_{\text{cav}} \xrightarrow[\mathrm{l}\to 0;\ w\to\infty\ (\text{or } t\to 0)]{} H_0 \times P_{\text{sat}}(T_0)\times\frac{S(T_0)}{S(T_1)}$$

Delamination pressure exists even with no physical void.

Example:

- Unit preconditioned in 85/85 for a long time, then subjected to 215 C solder shock.
- Saturation coefficient has activation energy of 0.4 eV. (eg. Kitano et. al.)
- Steam table pressure at 85 C is 0.57 atm.

$$P_{\text{cav}} = 0.85\times 0.57\times\exp\left\{\frac{0.40\ \text{eV}}{8.62\times 10^{-5}\ \ \text{eV}/{}^\circ\text{K}}\left(\frac{1}{273+85}-\frac{1}{273+215}\right)\right\}$$

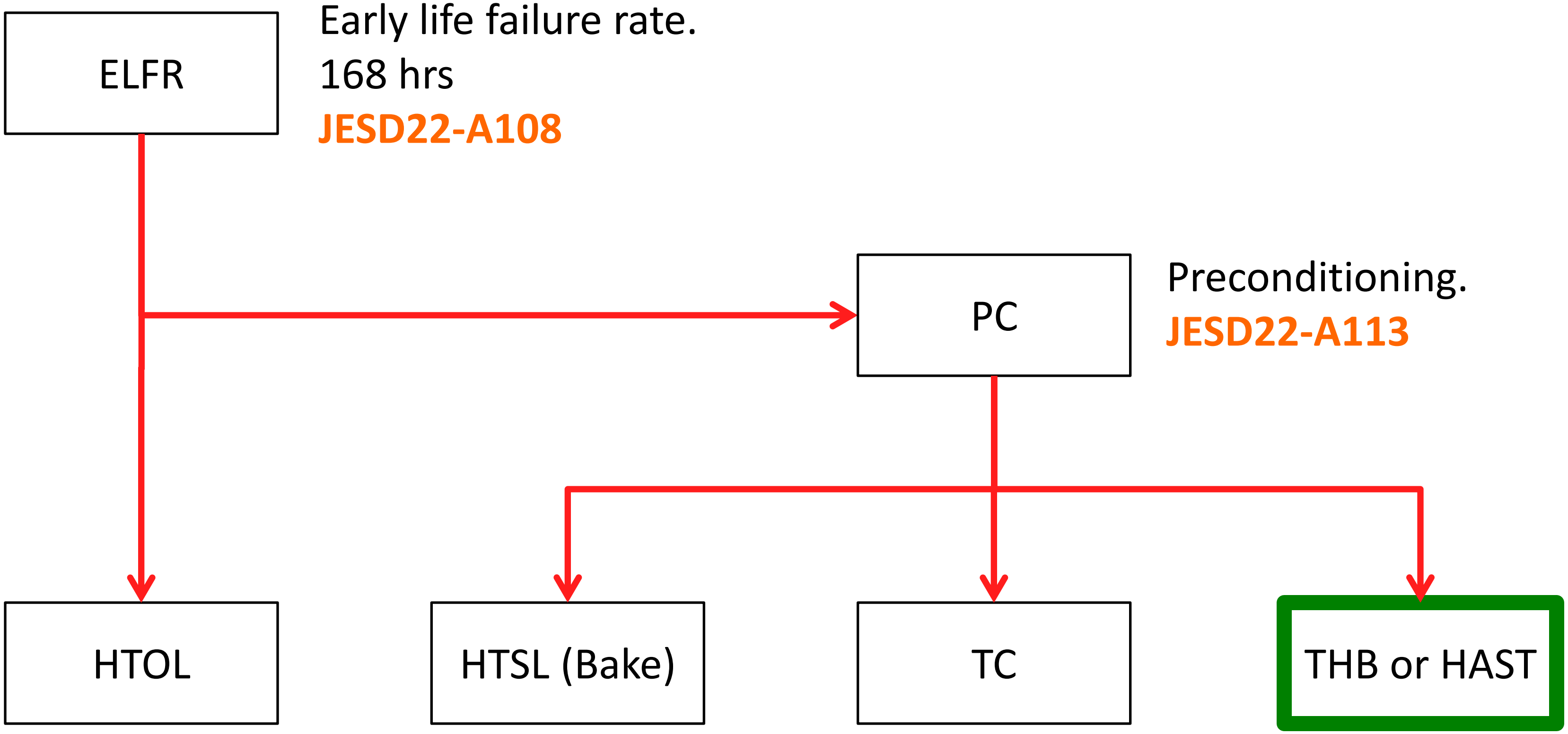
$$= 15.3\ \ \text{Atmospheres}$$

Wow!!

Outline

- Plastic Package Technology
- Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - ● Moisture
  - Thermal
  - Thermo-mechanical

Example Stress Flow



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

HAST System

- Large vessel (24” dia) requires forced convection.

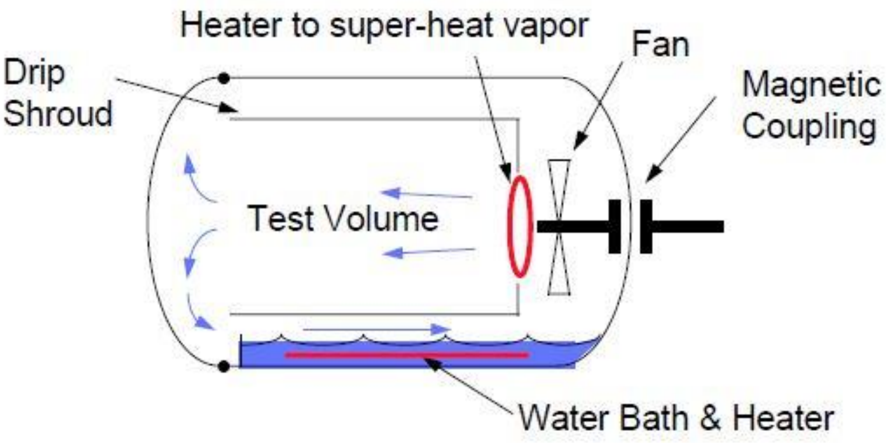
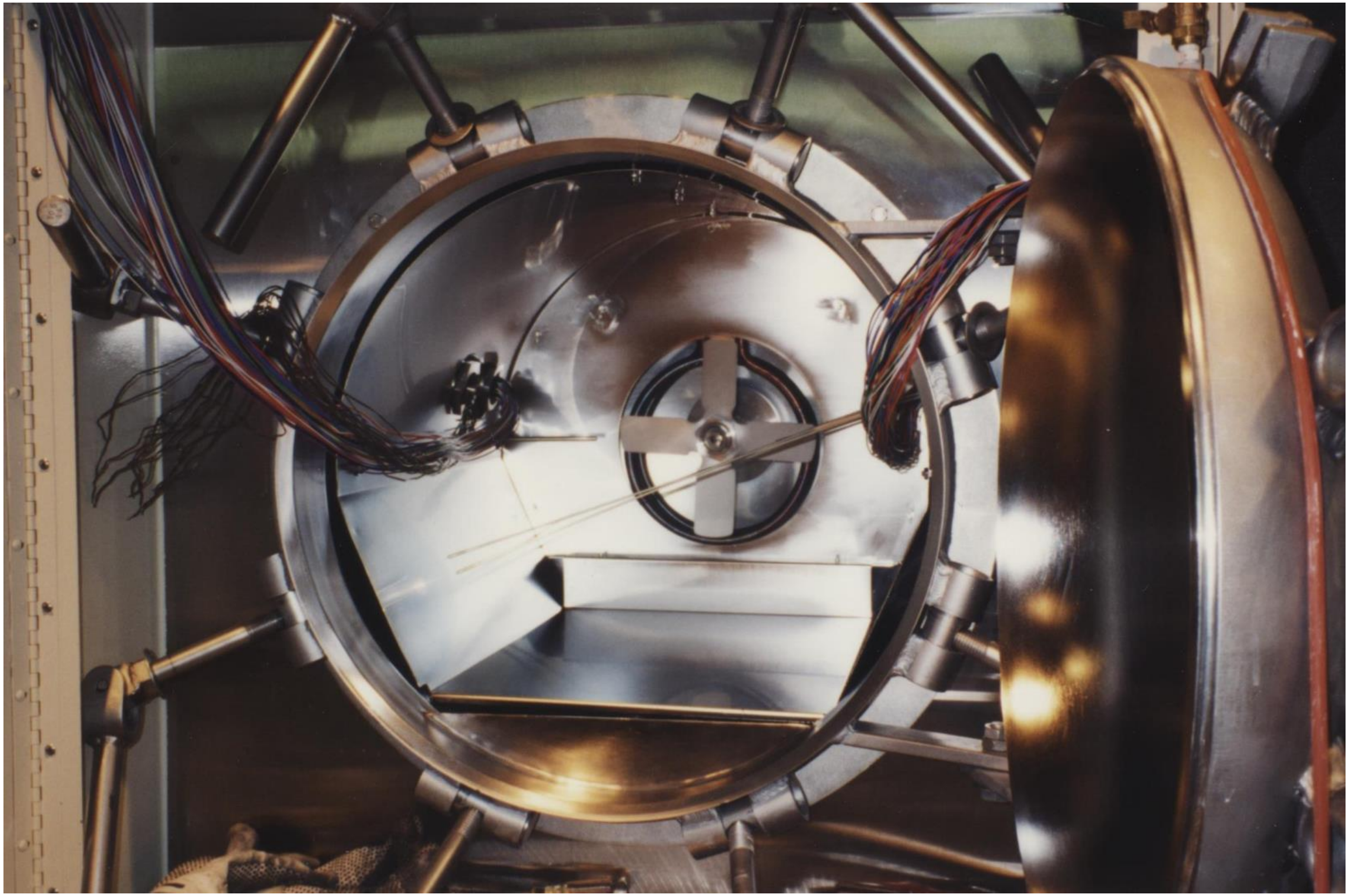


Fig. 3 The NG HAST chamber operates on the principle of forced convection. This ensures efficient mixing, minimizing temperature gradients across the test volume. Reliability of the fan drive is ensured by a proven design of magnetic coupling feed through.

C. G. Shirley, “A New Generation HAST System”, Non-proprietary Report to Intel, Despatch Industries, and Micro-Instrument Corp. describing learnings during development of NG HAST. December, 1994.

HAST System



HAST System


LPB series
WARNING
HIGH VOLTAGE
HIGH TEMPERATURES MAY BE PRESENT INSIDE. DO NOT TOUCH HOT SURFACES.

HAST Ramp Up Requirements

- Ramp Up: Avoid condensation on load.

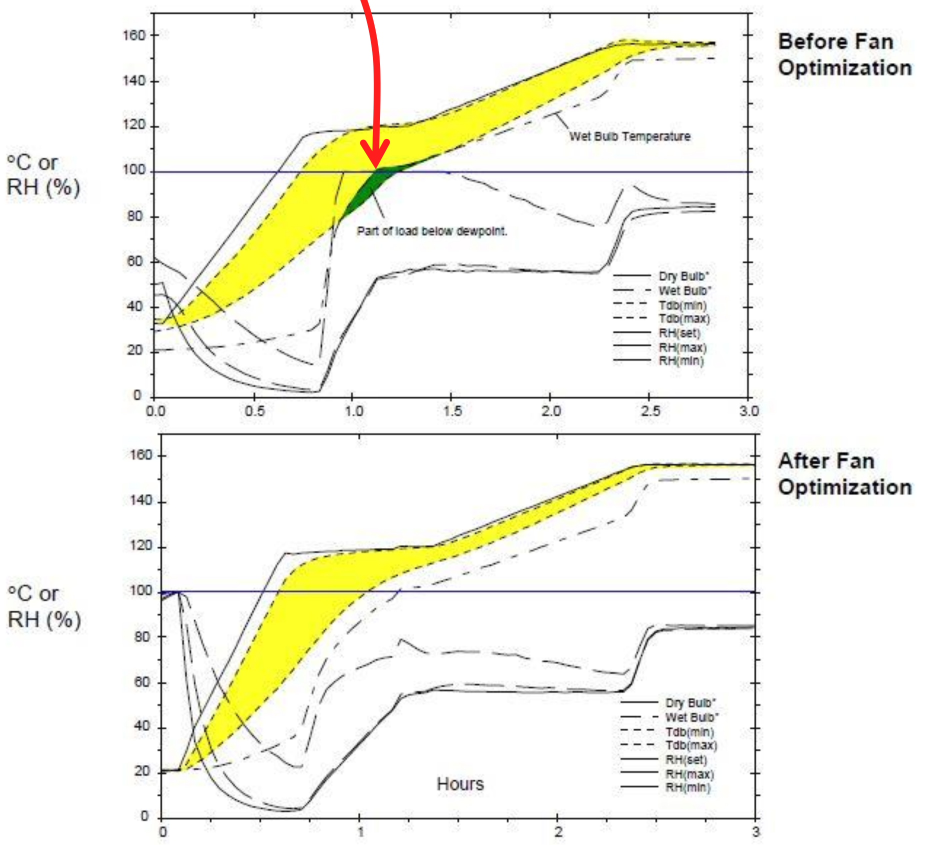
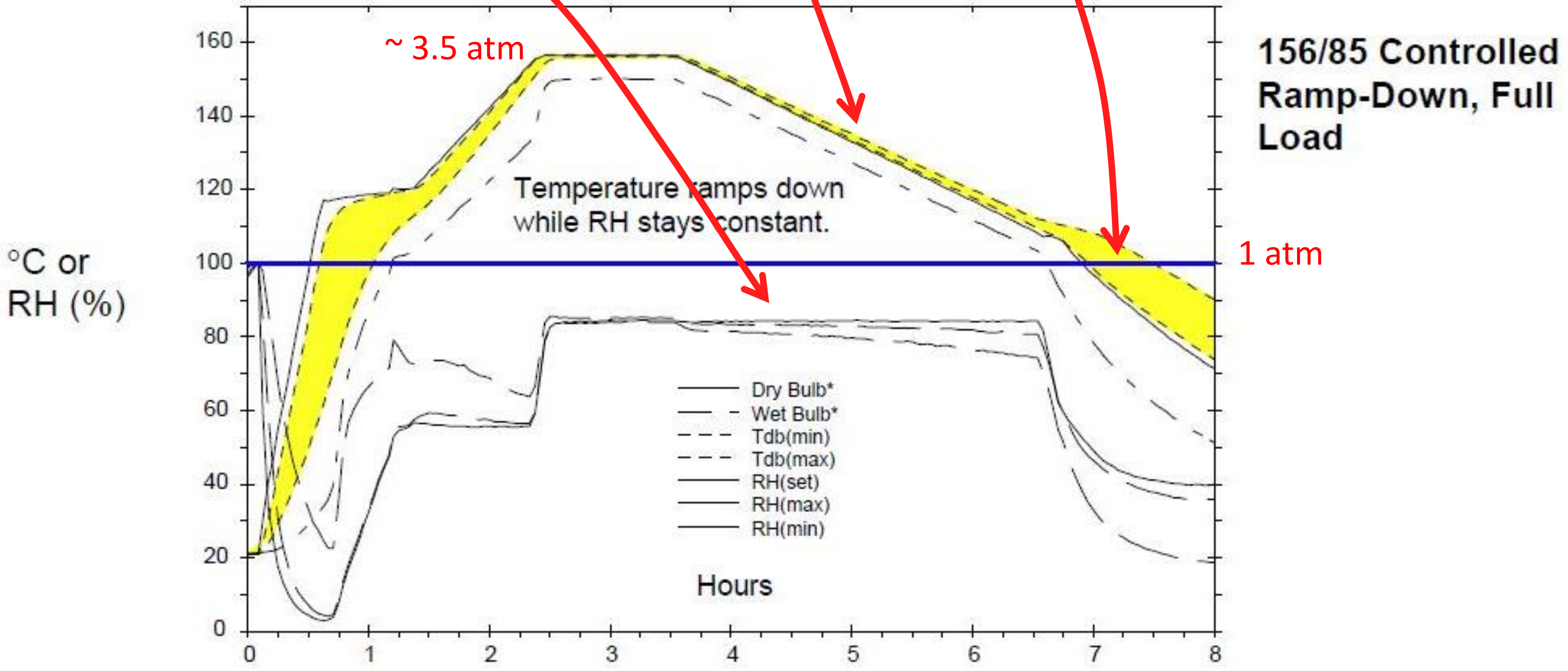


Fig. 4 Full-load ramp-up profile to 156/85 before (top) and after (bottom) optimization of fan. After optimization, the wet-bulb temperature is always below temperature at any point in the load.

HAST Ramp-Down Requirements

- Mechanical pressure relief must be slow (3 h).
- Vent when pressure reaches 1 atm.
- Hold RH at test value.
  - Units must retain moisture acquired during test.



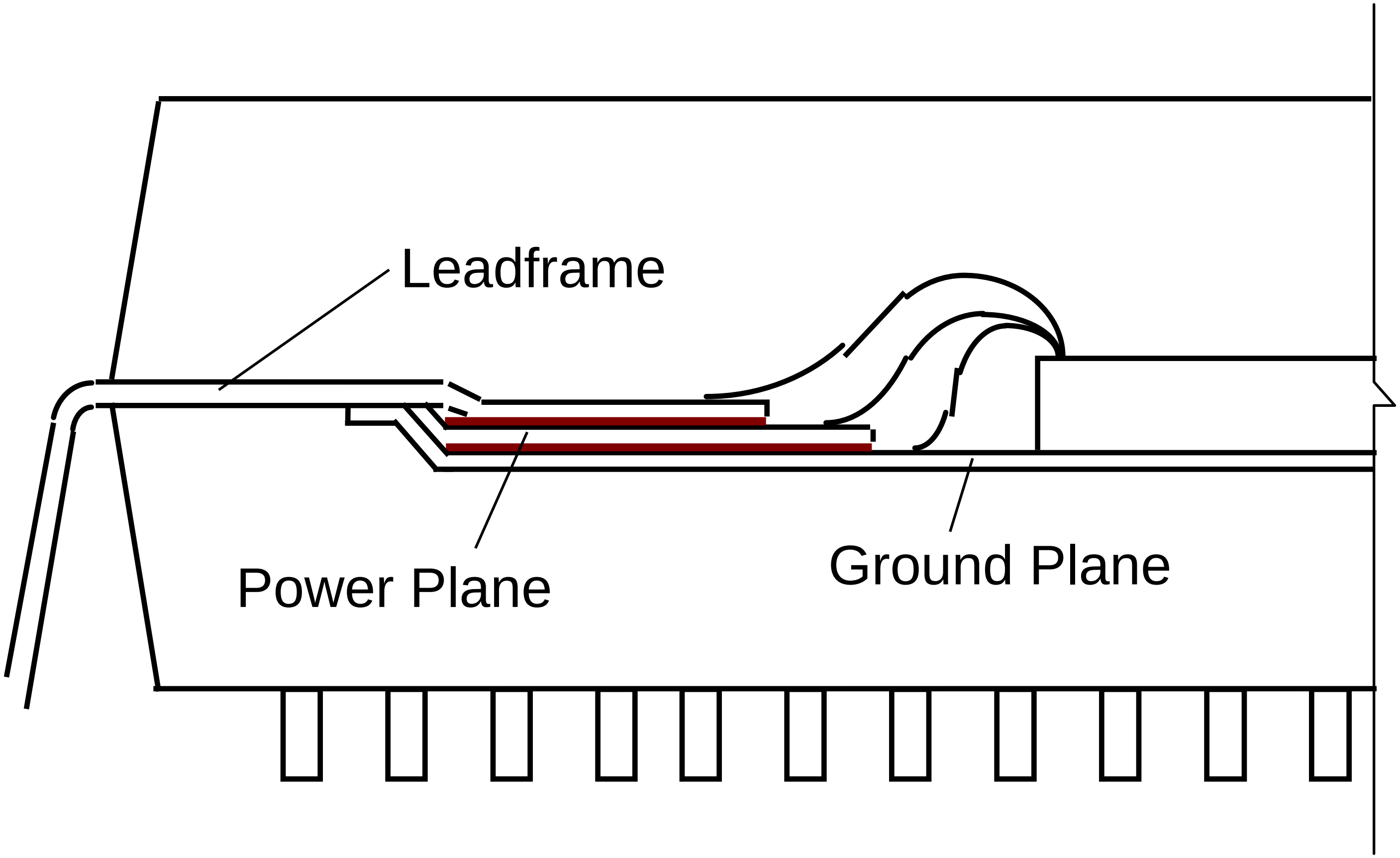
Peck's Acceleration Model

- Fundamental environmental parameters are *T*, *H* and *V*, *at the site* of the failure mechanism.
  - If the die is the site, this is denoted by "*j*".
- A frequently used acceleration model is due to Peck

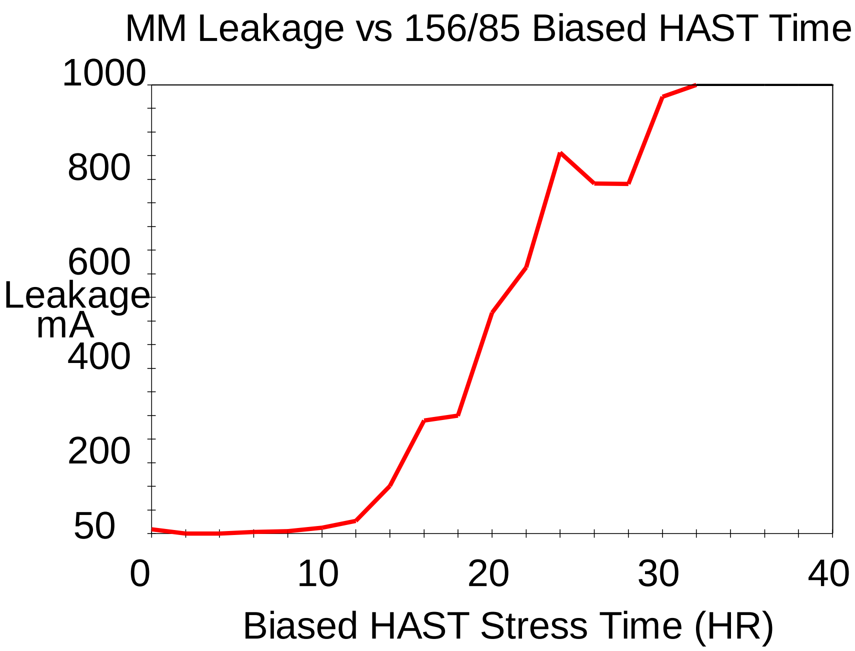
$$AF = (a + b \times V) \times H_j^m \times \exp(-Q/kT_j)$$

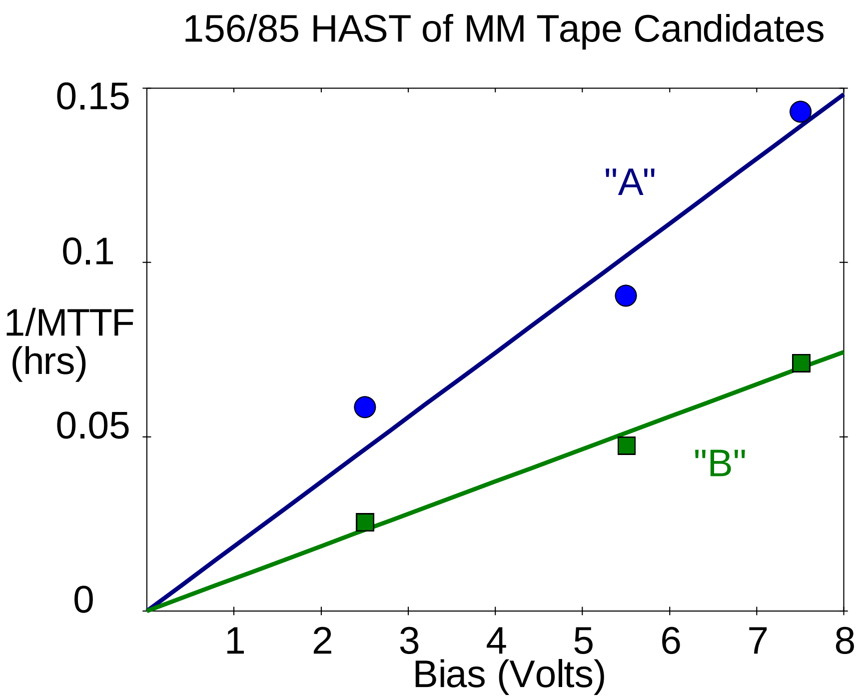
- Find *a*, *b*, *m*, *Q* from experiments with steady-state stress and negligible power dissipation.
- Typically *a* is small or zero: Bias is required.
- Requires *H* > 0 for acceleration: Moisture is required.

Moisture: MM Tape Leakage



Moisture: MM Tape Leakage





Experimental Tape Data:

Tape	m	Q eV
“A”	>12	0.74
“B”	5	0.77

Source: C. Hong, Intel, 1991

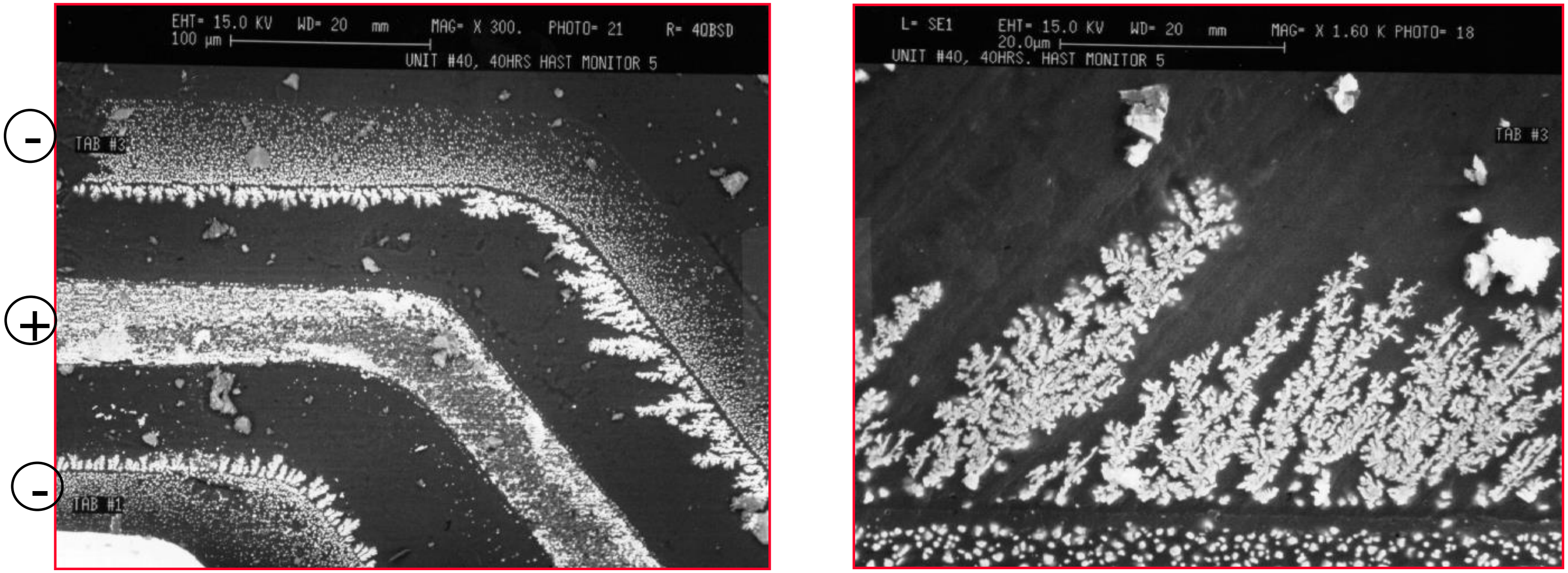
Acceleration factor is proportional to bias.

$$AF =$$

$$\text{Constant} \times V \times H^m \exp(-Q/kT)$$

Moisture: Internal Metal Migration

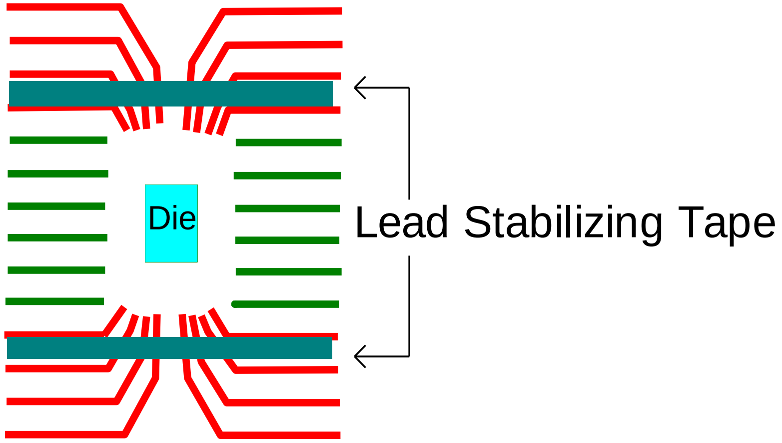
- TAB Inter-lead Leakage/Shorts
  - Accelerated by voltage, temperature and humidity
  - Seen as early as 20 hrs 156/85 HAST
  - Highly dependent on materials & process



Copper dendrites after 40 hours of biased 156/85 HAST

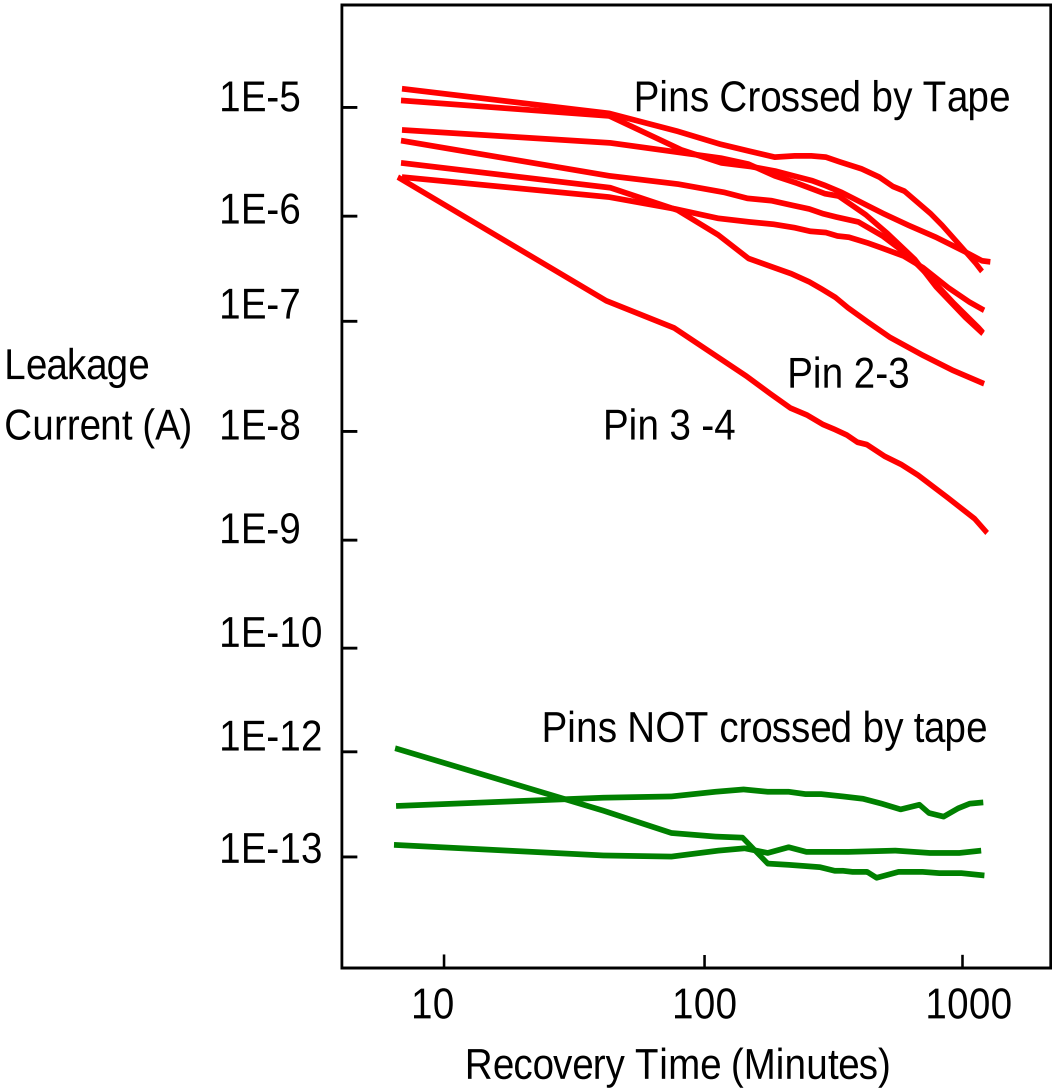
Lead-Stabilizing Tape Leakage

- A vendor process excursion.
- Leakage observed after 336 hours of steam.
- Re-activated by 48 hours at 70C/100% RH
- No leakage seen between leads not crossed by tape
- Rapid decay for leads crossing end of tape
  - Tape dries from exterior inwards



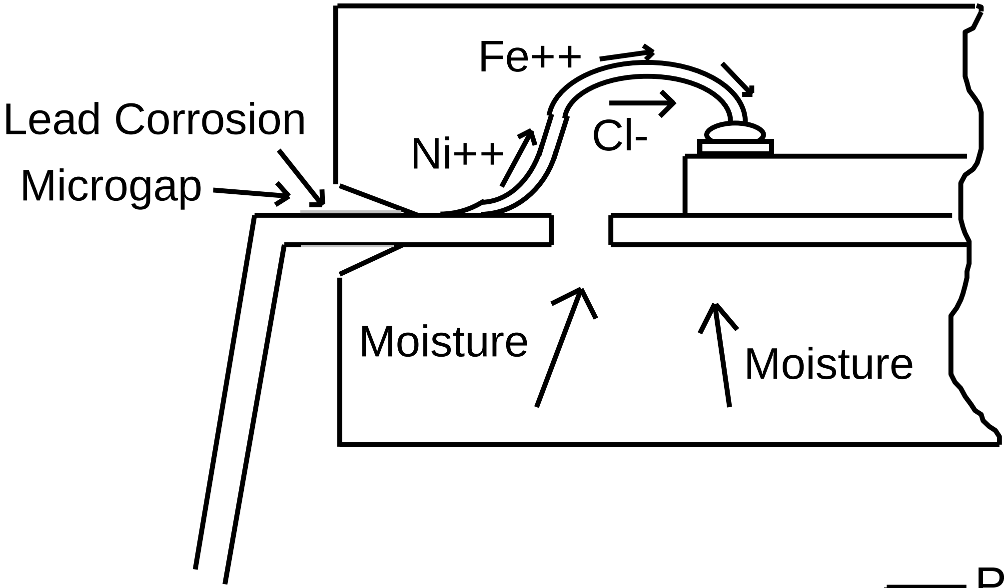
Tape provides mechanical stability to long leads during wirebond.

Lead-Stabilizing Tape Leakage



Source: S. Maston, Intel

Aluminum Bond Pad Corrosion

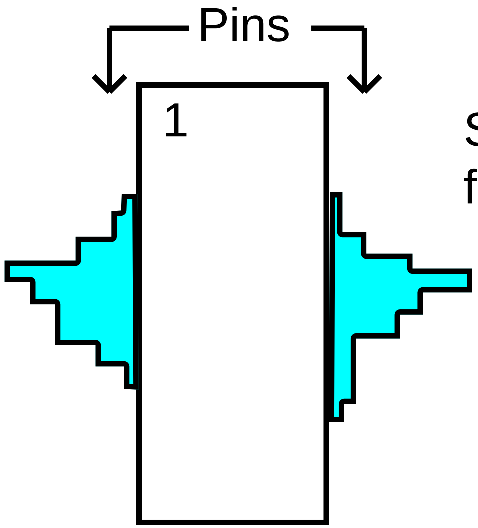


$$AF =$$

$$\text{Constant} \times V \times H^{m} \exp(-Q/kT)$$

Source	m	Q (eV)
Peck (a)	2.66	0.79
Hallberg&Peck (b)	3.0	0.9

(a) IRPS, 1986; (b) IRPS, 1991.



Shortest path has highest failure rate.

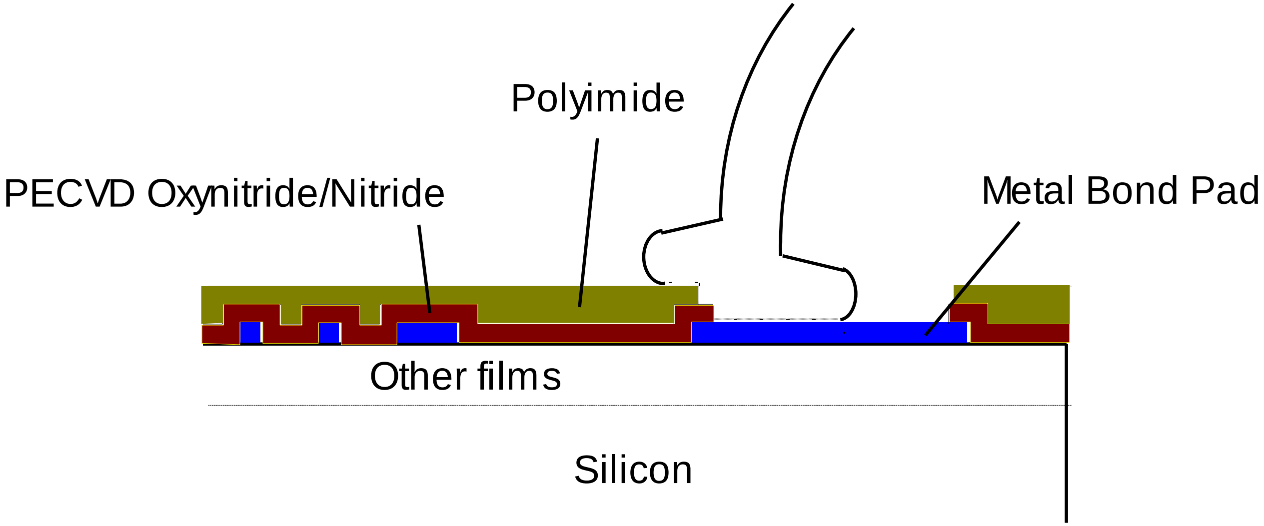
Source: P.R. Engel, T. Corbett, and W. Baerg, "A New Failure Mechanism of Bond Pad Corrosion in Plastic-Encapsulated IC's Under Temperature, Humidity and Bias Stress" Proc. 33rd Electronic Components Conference, 1983.

Passivation in Plastic Packages

- Passivation is the final layer on the die.
- Passivation has two main functions:
  - Moisture Barrier
    - Molding compound is not a moisture barrier.
    - Silicon oxides are not good moisture barriers.
    - PECVD silicon nitride or silicon oxynitride film is a good barrier.
    - Film must be thick enough to avoid pinholes, coverage defects.
  - Mechanical Protection
    - Silicon nitride films are brittle.
    - Polyimide compliant film protects silicon nitride.
    - Polyimide can react with moisture (depending on formulation).

Polyimide/Au Bond Failure

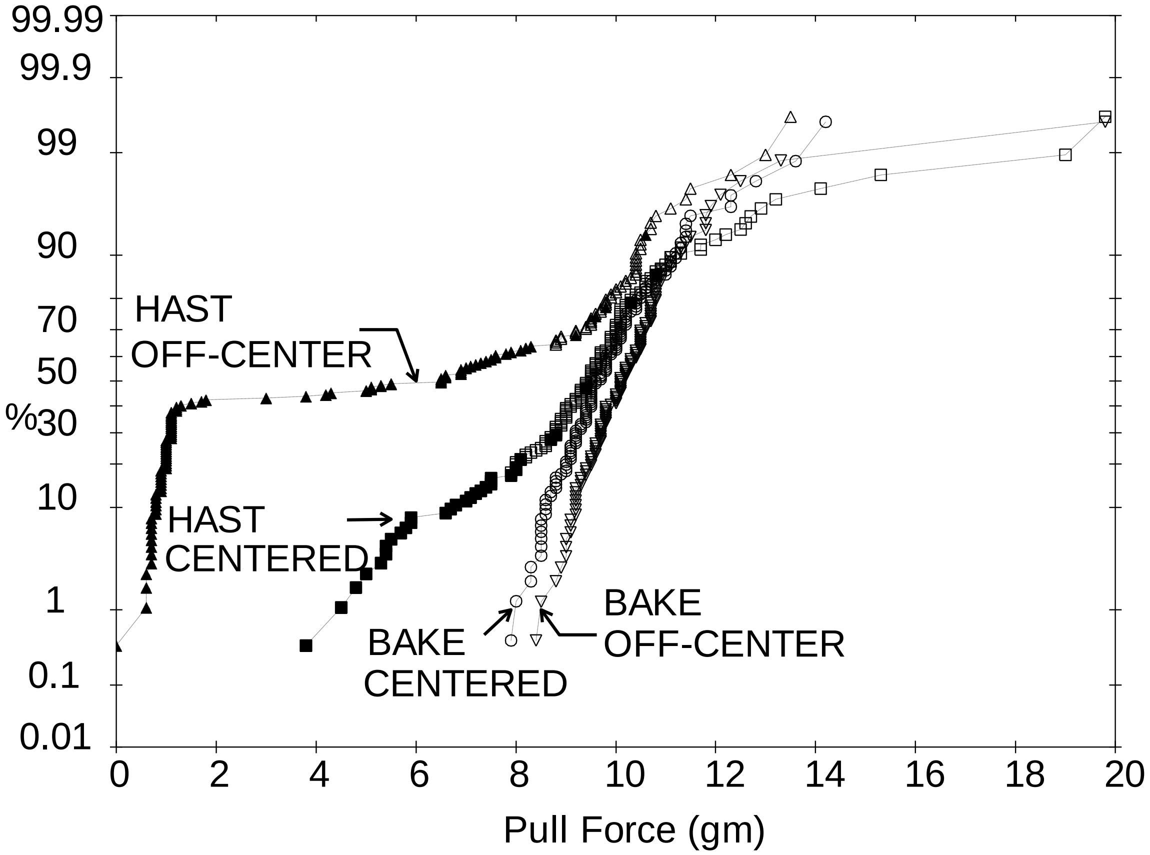
- Bonds overlapping passivation don't necessarily violate design rules.
- But can activate polyimide-related "purple plague" failure mechanisms in combination with moisture.
- Acceleration modeling showed no field jeopardy.



Moisture-Related Gold Bond Degrad’n

Effect of 80 hours of 156/85 HAST vs 156/0 Bake and Centered vs Off-Centered Bonds on Wire Pull Test Data

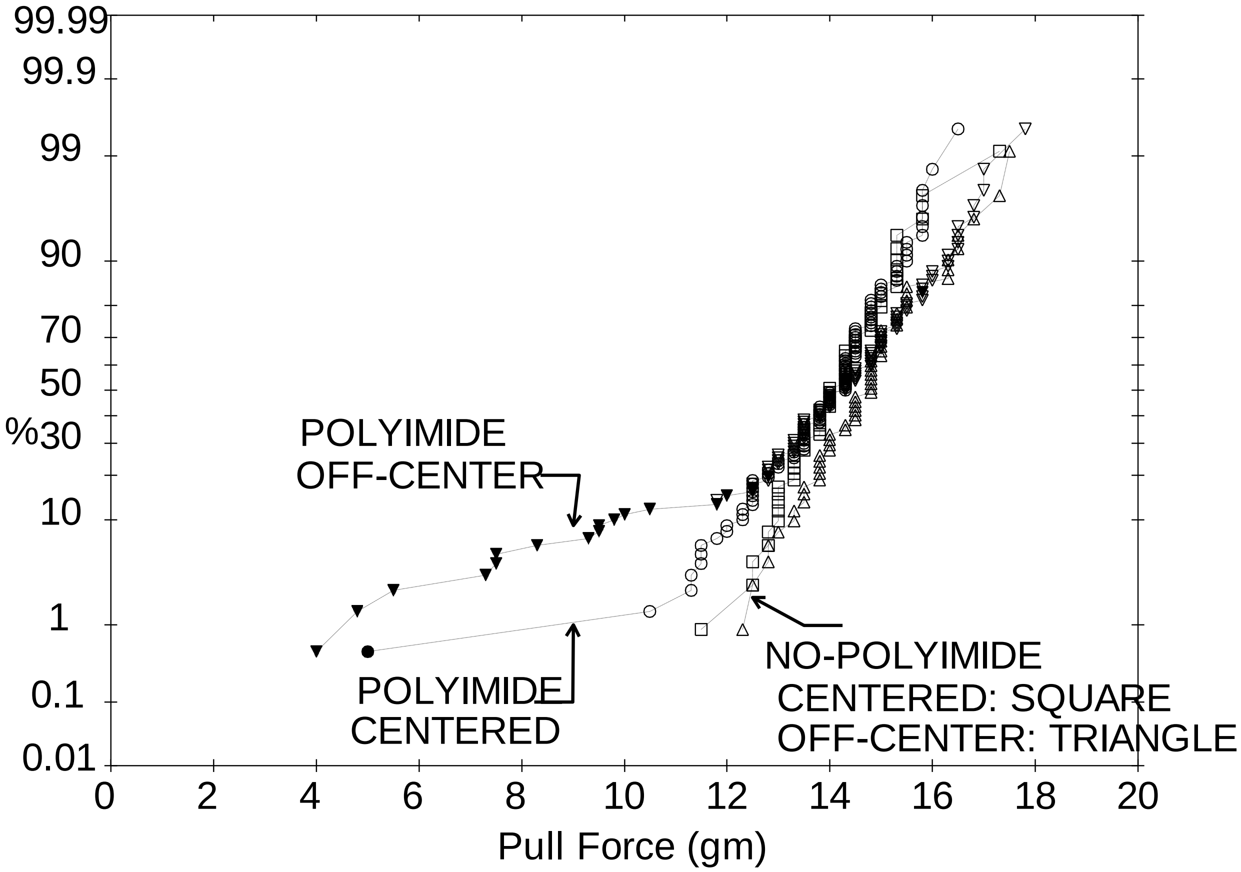
(all *with* polyimide)



Source: G. Shirley and M. Shell, IRPS, 1993

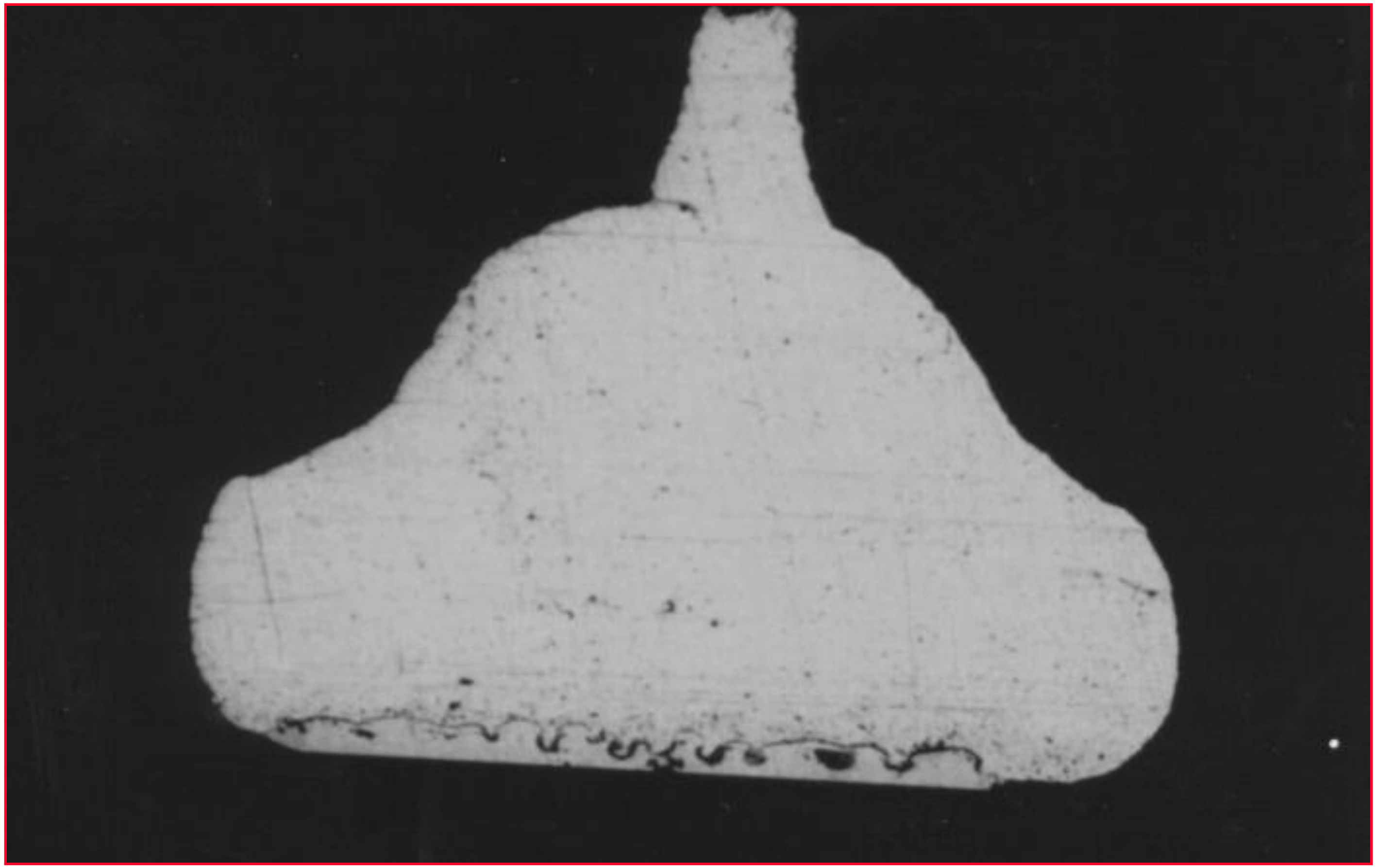
Moisture-Related Gold Bond Degrad'n

Wire Pull Strength of Polyimide vs No Polyimide and Centered vs Off-Centered Bonds after 40 hours of 156/85 HAST



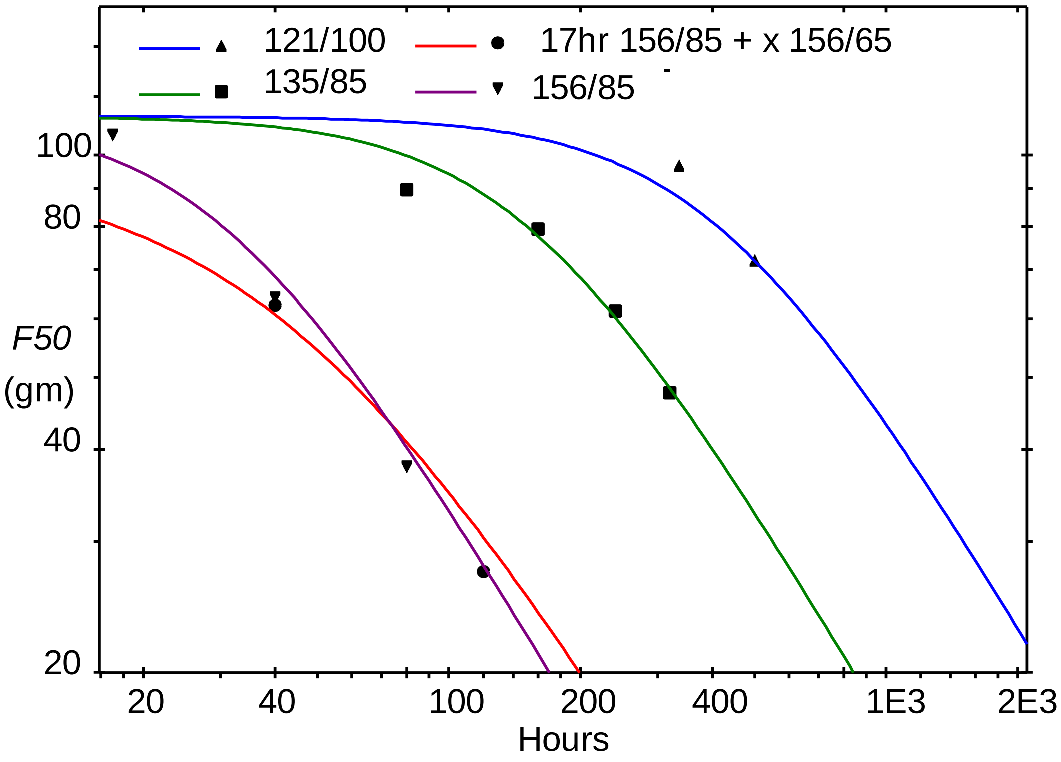
Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993

Moisture-Related Purple Plague



Cross-section of gold ball bond on aluminum pad
after 80 hours at 156C/85%RH

Moisture-Related Gold Bond Degrad’n



$$b = 112.7 \;\; \text{gm}$$

$$a_0 = 1.13 \times 10^{10} \;\; (\text{gm - hrs})^{-1}$$

$$m = 0.98; \quad Q = 1.15 \;\; \text{eV}$$

$$F_{50} = \frac{1}{\sqrt{(at)^2 + 1/b^2}}$$

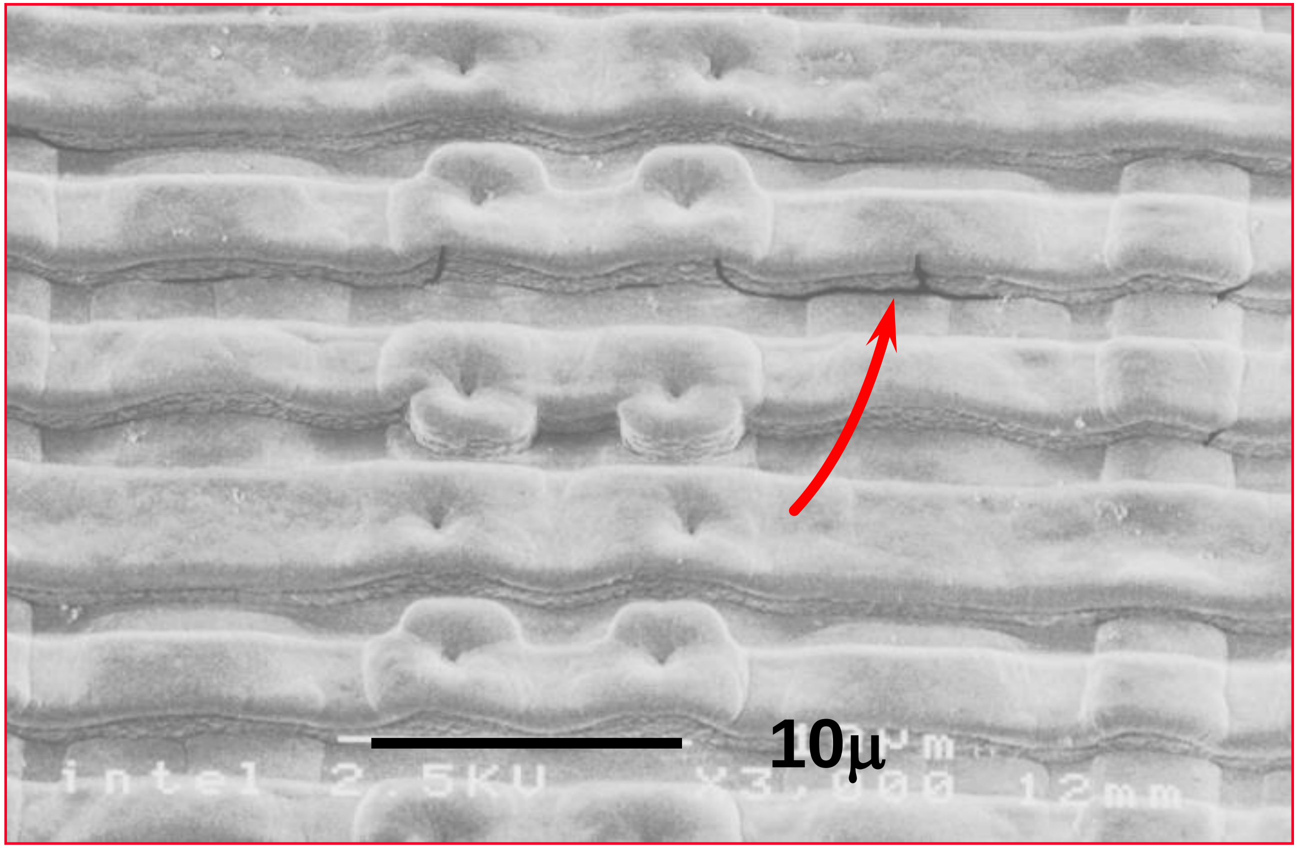
$$a = a_0 \times h^m \times \exp(-Q/kT)$$

$$F_P = F_{50} \times \exp(-\sigma \times Z_P)$$

$$\sigma = 0.17$$

Source: G. Shirley and M. Shell-DeGuzman, IRPS, 1993

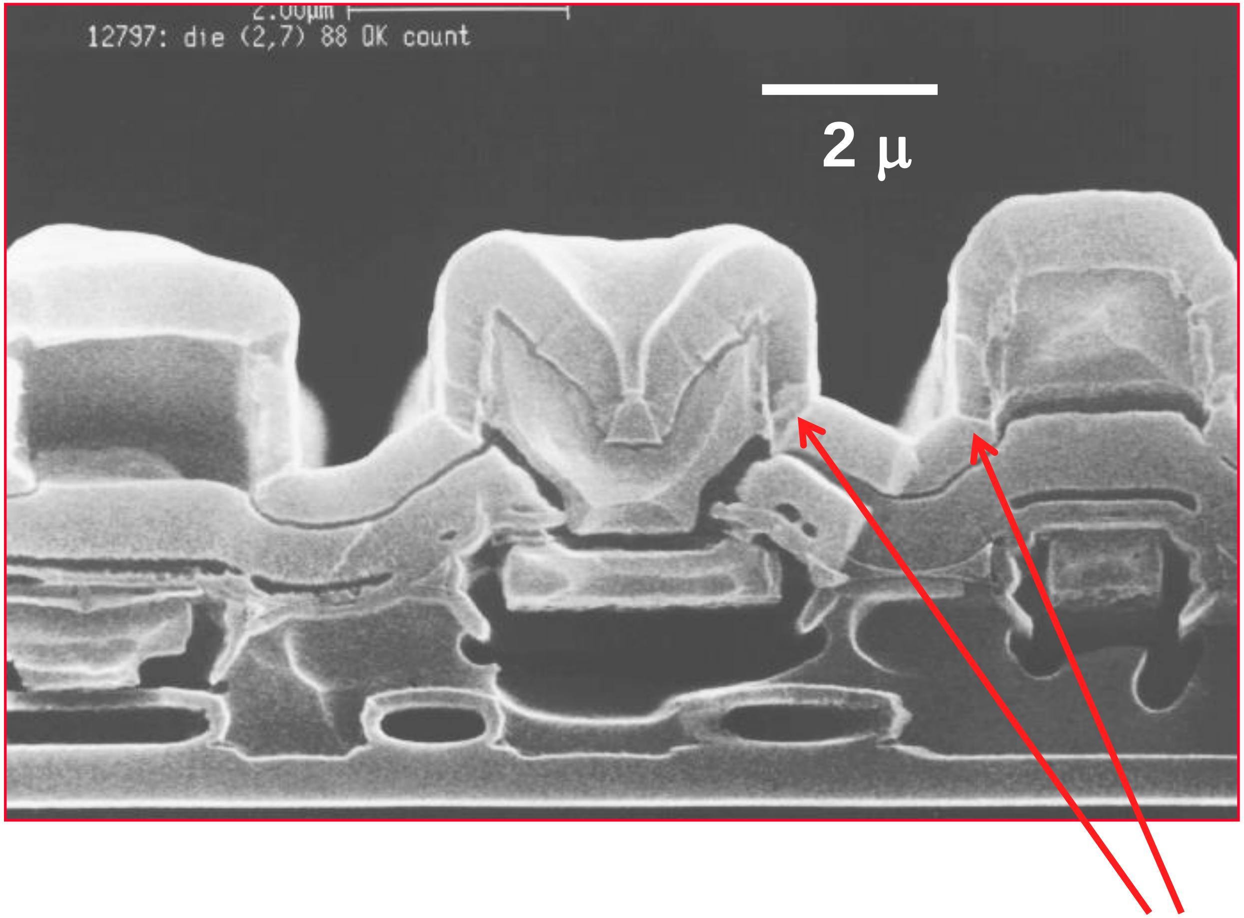
Circuit Failure Due to Passiv'n Defects



Site of failing bit. SRAM after HAST stress.

Courtesy M. Shew, Intel

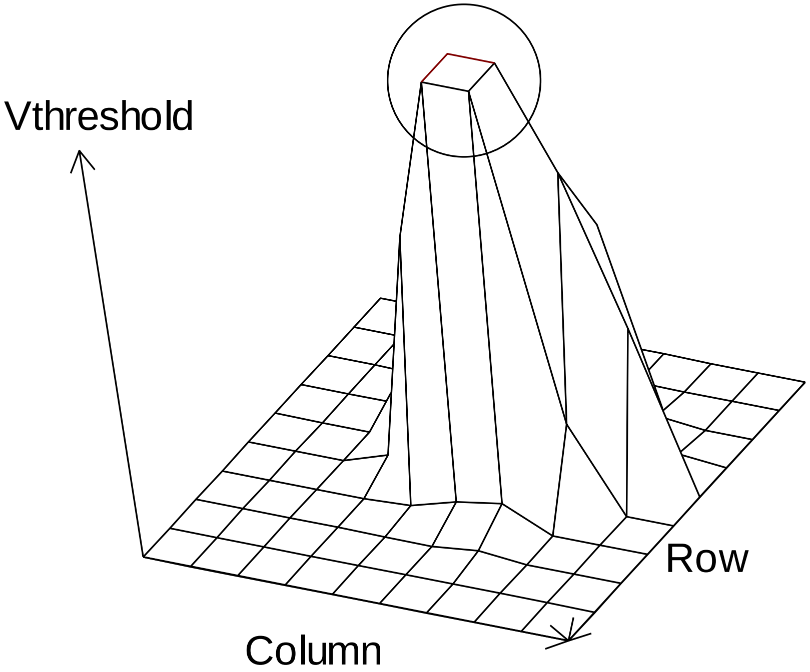
Circuit Failure Due to Passiv’n Defects



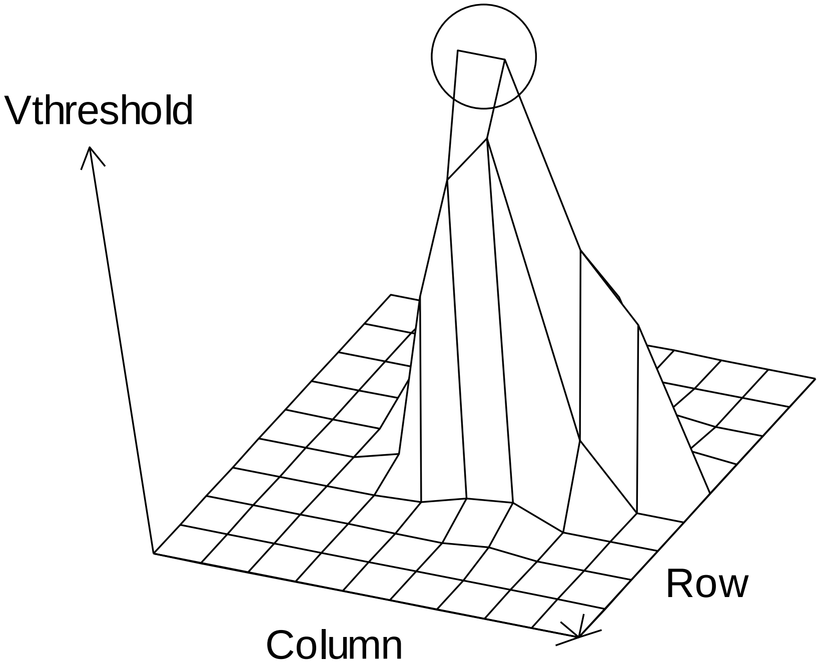
Etch-decorated cross-section of passivation. Note growth seams.

Circuit Failure Due to Passiv’n Defects

SRAM VOLTAGE THRESHOLD MAP FOR CELL PULLUP TRANSISTOR
(Baseline threshold is 0.89 V. Passivation is 0.6 μ nitride, no polyimide.)



After 120 h 156/85. 4 failed bits with Vt > 2.5 V

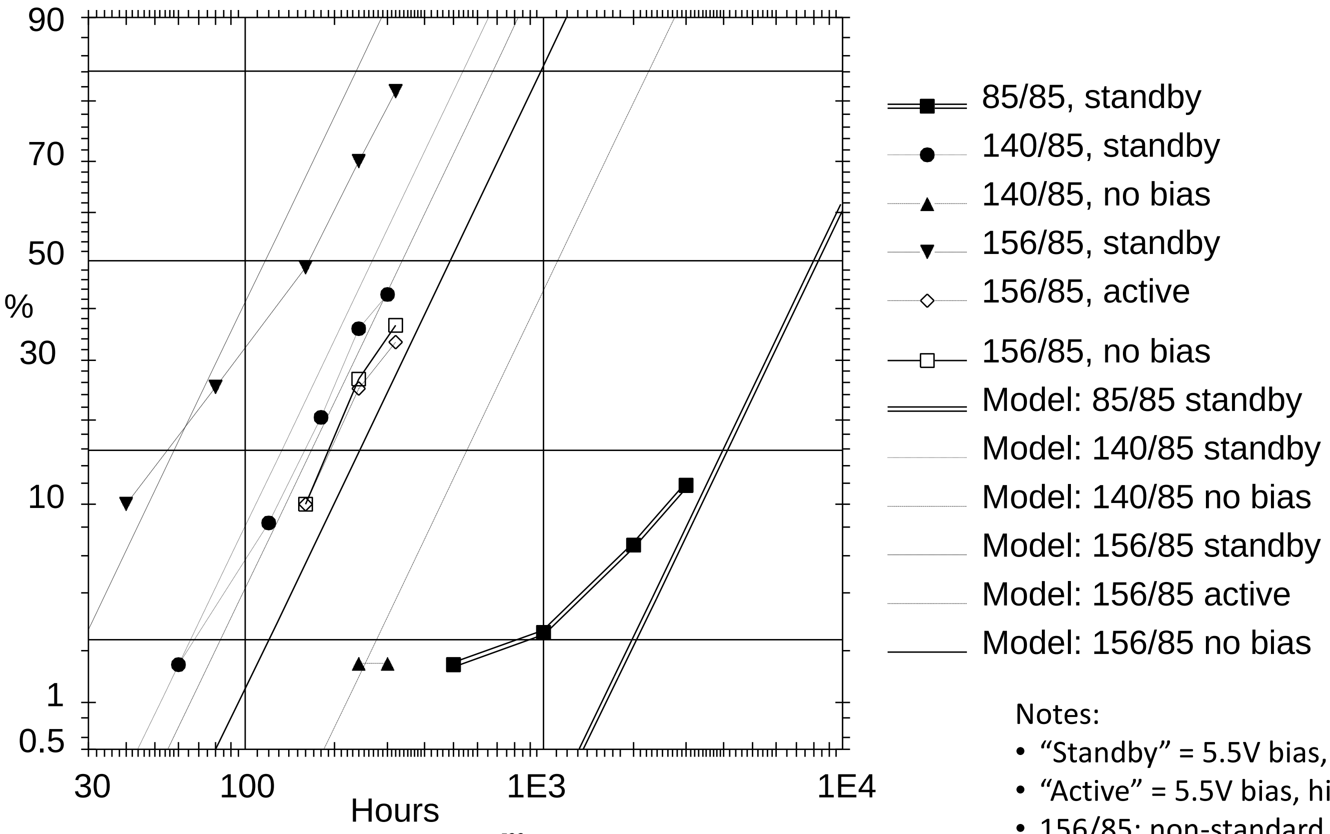


2 bits recover after further 2 hr bake at 150 C

Source: C. Hong, Intel

Acceleration Model Fit of HAST Data

SRAM HAST and 85/85 Bit Failures (No Polyimide)



$$AF = \text{Constant} \times (a + bV) \times H^m \times \exp(-Q/kT)$$

$$a = 0.24 \quad b = 0.14 \quad m = 4.64 \quad Q = 0.79 \ \text{eV}$$

Notes:

- "Standby" = 5.5V bias, low power
- "Active" = 5.5V bias, high power
- 156/85: non-standard, limit of pressure vessel.
- Source: C. G. Shirley, C. Hong. Intel

Peck Model Parameters

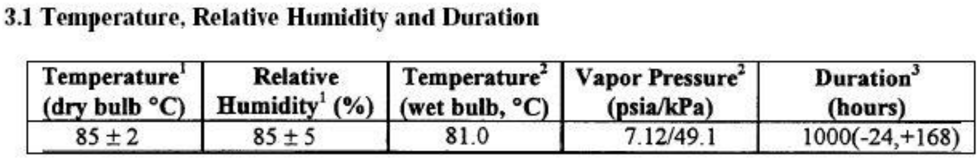
Mechanism	Q(eV)	m	Q/m	Q/m < 0.42eV?	Hours of 130/85 ≡ 1kh 85/85	Reference
MM Tape A	0.74	12	0.06	Yes	69	2
MM Tape B	0.77	5	0.15	Yes	62	2
Single Bit SRAM	0.79	4.6	0.17	Yes	57	3
Corrosion, THB (early Peck)	0.79	2.66	0.30	Yes	57	4
Corrosion, THB (later Peck)	0.90	3	0.30	Yes	39	5
Bond Shear	1.15	0.98	1.17	No	16	6

Yes/No: Increasing power dissipation at die, slows/accelerates the moisture mechanism.

1. Kitano, A. Nishimura, S. Kawai, K. Nishi, "Analysis of Package Cracking During Reflow Soldering Process," Proc. 26th Ann. Int'l Reliability Physics Symposium, pp90-95 (1988)
2. S. J. Huber, J. T. McCullen, C. G. Shirley. ECTC Package Rel. Course, May 1993. Package tape leakage acceleration data courtesy C. Hong.
3. G. Shirley and C. Hong, "Optimal Acceleration of Cyclic THB Tests for Plastic-Packaged Devices," in Proc. 29th Ann. Int'l Reliability Physics Symposium, pp12-21 (1991)
4. S. Peck, "Comprehensive Model for Humidity Testing Correlation," in Proc. 24th Ann. Int'l Reliability Physics Symposium, pp44-50 (1986).
5. Hallberg and D. S. Peck, "Recent Humidity Accelerations, A Base for Testing Standards," Quality and Reliability Engineering International, Vol. 7 pp169-180 (1991)
6. G. Shirley and M. Shell-DeGuzman, "Moisture-Induced Gold Ball Bond Degradation of Polyimide-Passivated Devices in Plastic Packages," in 31st Ann. Int'l Reliability Physics Symposium, pp217-226 (1993).

HAST versus 85/85, ct'd

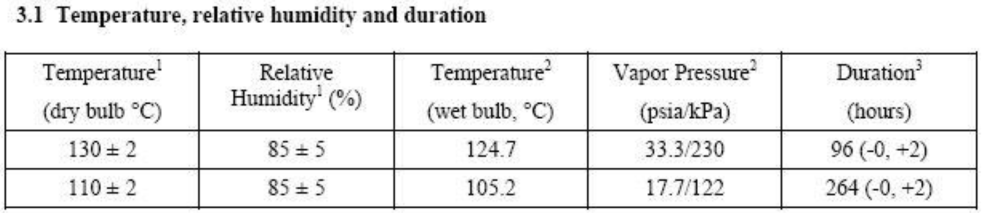
- For all mechanisms surveyed, 1000 hours of 85/85 is equivalent to < 96 hr of 85/85.
- For packages < 10 mils covering die, moisture saturation occurs within 10 h at 130/85.
- For T_j-$T_a > 10°\text{C}$, most mechanisms (with $Q/m < 0.42$ eV) can be more accelerated with cyclical bias.
- 85/85
  - **JESD22-A101**



3.1 Temperature, Relative Humidity and Duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
85 ± 2	85 ± 5	81.0	7.12/49.1	1000(-24,+168)

- HAST
  - **JESD22-A110**



3.1 Temperature, relative humidity and duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
130 ± 2	85 ± 5	124.7	33.3/230	96 (-0, +2)
110 ± 2	85 ± 5	105.2	17.7/122	264 (-0, +2)

Outline

- Plastic Package Technology
- Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - Moisture
  - ● Thermal
  - Thermo-mechanical

Focus Topic: Acceleration

- Acceleration between two stresses is the ratio of times (or cycles) to achieve the same effect.
- The "same effect" could be the same fraction failing.
    - eg. The ratio of median (not mean!) times to failure in different stresses is the Acceleration Factor (AF).
        - AF is proportional to 1/MTTF

"Activation energy"

$$AF(2|1)=\frac{MTTF_1}{MTTF_2}=\exp\left\{\frac{Q}{k_B}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right\}$$

Thermal ("Arrhenius")

$$AF(2|1)=\frac{MTTF_1}{MTTF_2}=\exp\left\{\frac{Q}{k_B}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right\}\exp\left\{C\left(V_2-V_1\right)\right\}$$

Thermal and Voltage

$$AF(2|1)=\frac{MTTF_1}{MTTF_2}=\left\{\frac{a+bV_2}{a+bV_1}\right\}\left\{\frac{RH_2}{RH_1}\right\}^m\exp\left\{\frac{Q}{k_B}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right\}$$

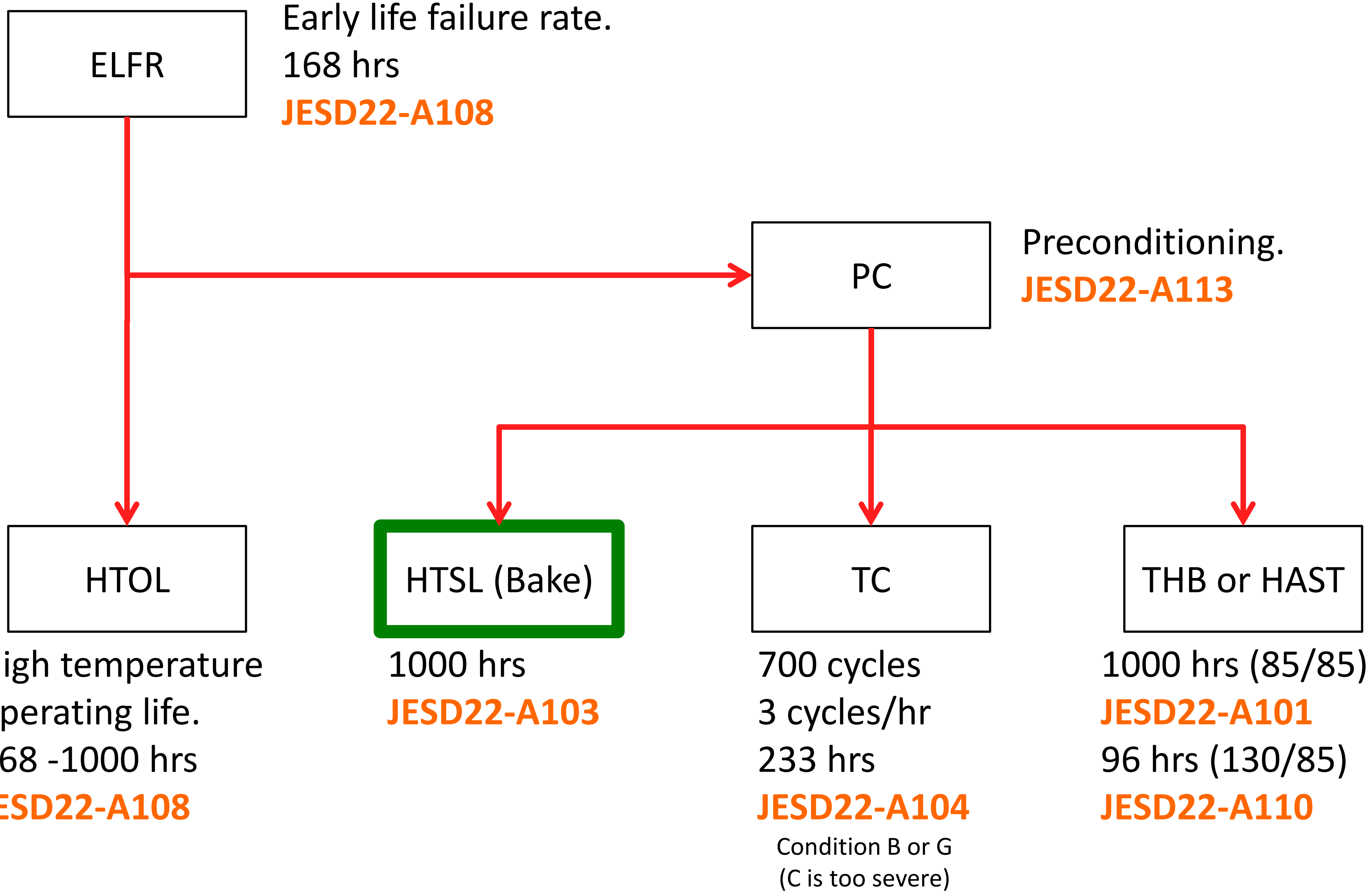
Moisture ("Peck")

$$AF(2|1)=\frac{MCTF_1}{MCTF_2}=\left\{\frac{\Delta T_2}{\Delta T_1}\right\}^m$$

Thermal Cycle ("Coffin-Manson")

"cycles"

Thermal Mechanisms



ELFR

Early life failure rate.
168 hrs
JESD22-A108

PC

Preconditioning.
JESD22-A113

HTOL

High temperature operating life.
168 -1000 hrs
JESD22-A108

HTSL (Bake)

1000 hrs
JESD22-A103

TC

700 cycles
3 cycles/hr
233 hrs
JESD22-A104
Condition B or G
(C is too severe)

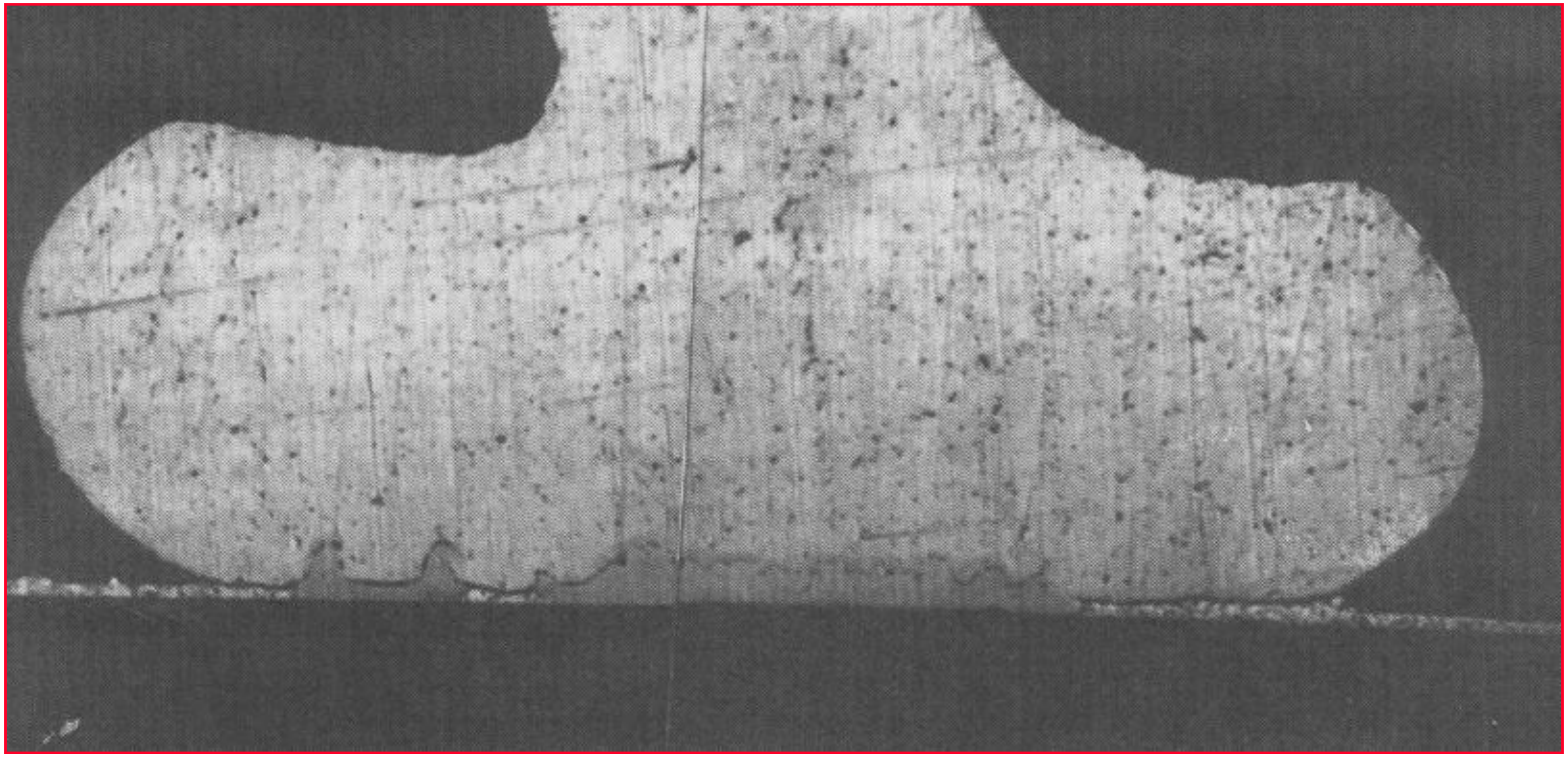
THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Gold-Aluminum Bond Failure

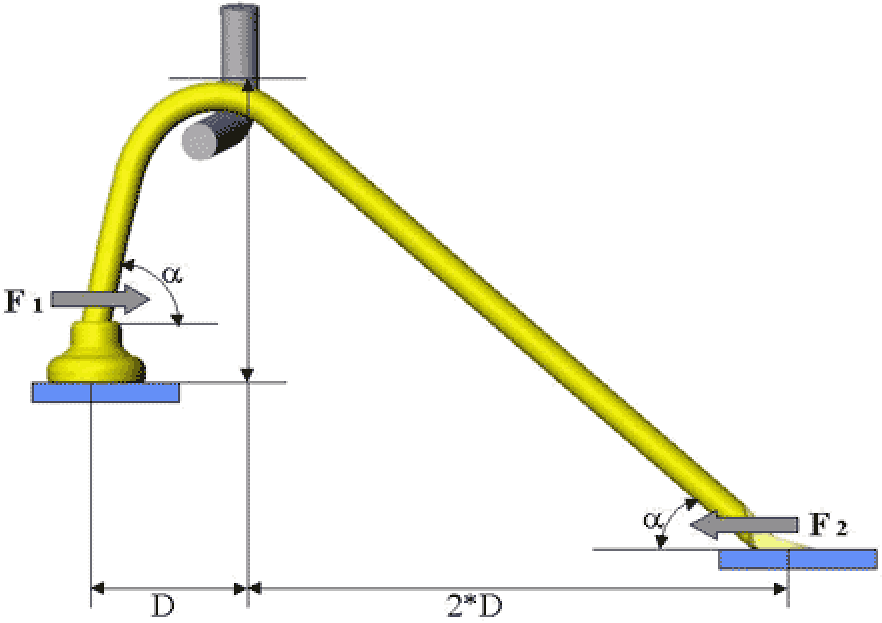
- Gold and Aluminum interdiffuse.
  - Intermetallic phases such as $AuAl_2$ (“Purple Plague”) form.
  - Imbalance in atomic flux causes Kirkendall voiding.
  - Bromine flame retardant is a catalyst.
- Kirkendall voids lead to
  - Bond weakening - detected by wire pull test.
  - Resistance changes in bond - detected by Kelvin measurement of bond resistance.

Thermal (Ordinary) Purple Plague



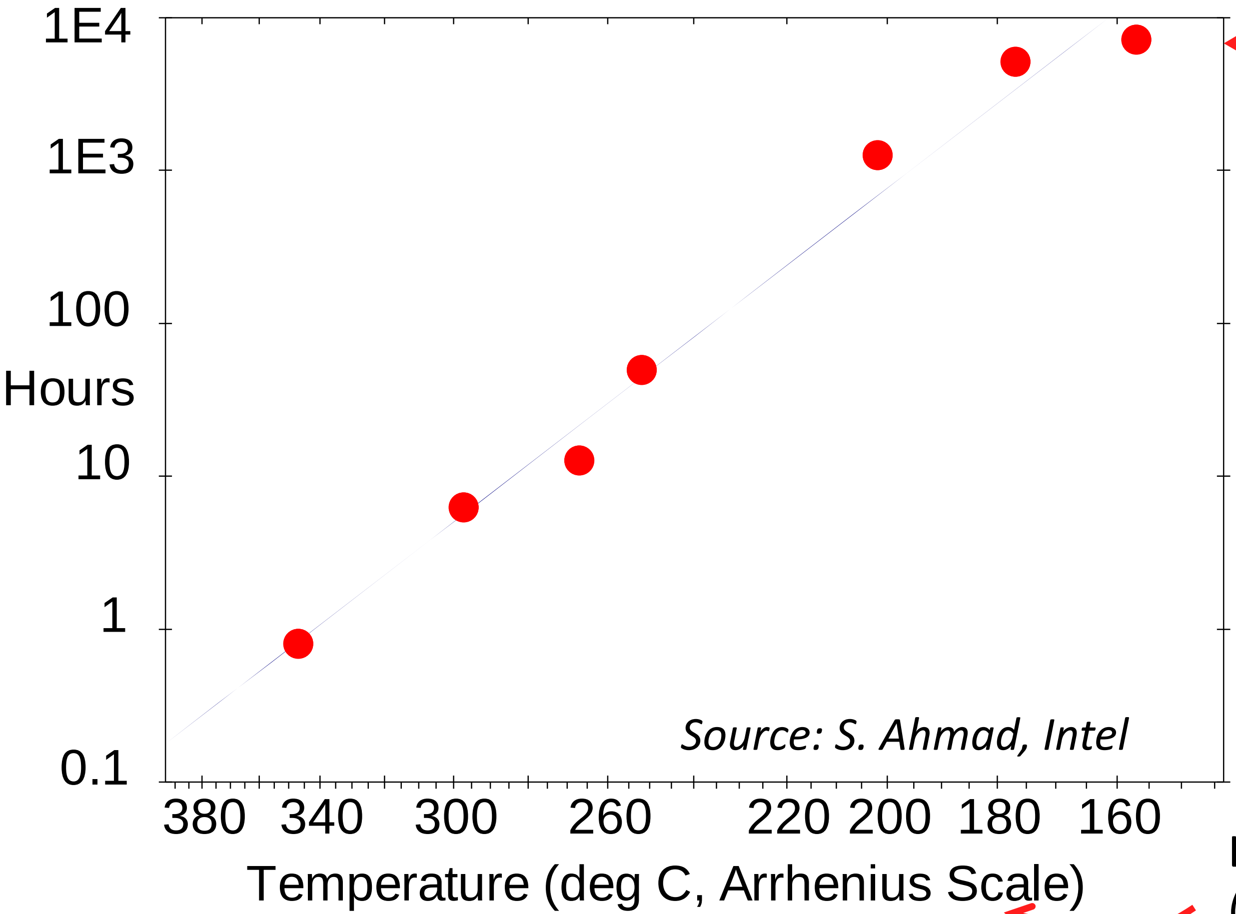
Cross-section of gold ball bond on aluminum pad
after 200 hours at 160°C

Wire Bond Pull Test



Gold-Aluminum Bond Failure

Log scale



Source: S. Ahmad, Intel

1 year (!)
(8760h)

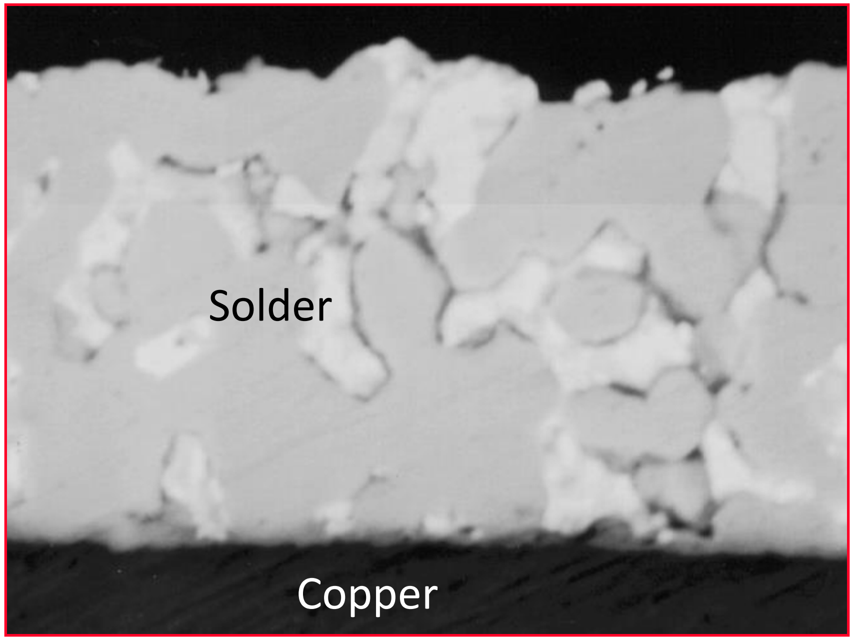
Linear in 1/T (°K), with ticks placed at T (°C).

Arrhenius plot of time to 10% of wire pull failure.
Activation energy (Q) = 1.17 eV.

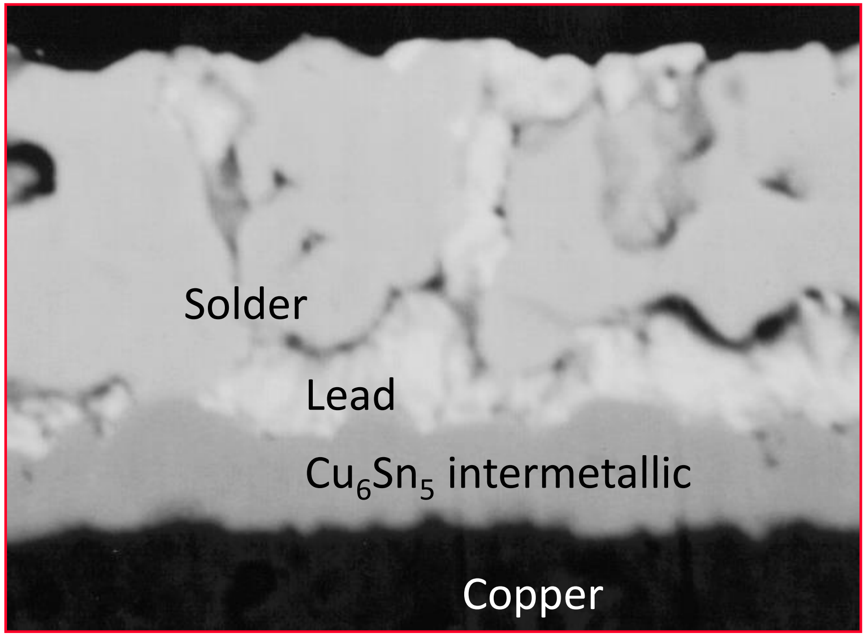
Thermal Degradation of Lead Finish

- Only an issue for copper lead frames (not Alloy 42).
- Cu_3Sn or Cu_6Sn_5 inter-metallic phases grow at the interface between solder or tin plating.
- Activation energy (Q) for inter-metallic phase growth is 0.74 eV.
- If inter-metallic phase grows to surface of solder or tin plate, solder wetting will not occur.
- Main effect is to limit the number of dry-out bakes of surface mount plastic components.

Thermal Degradation of Lead Finish

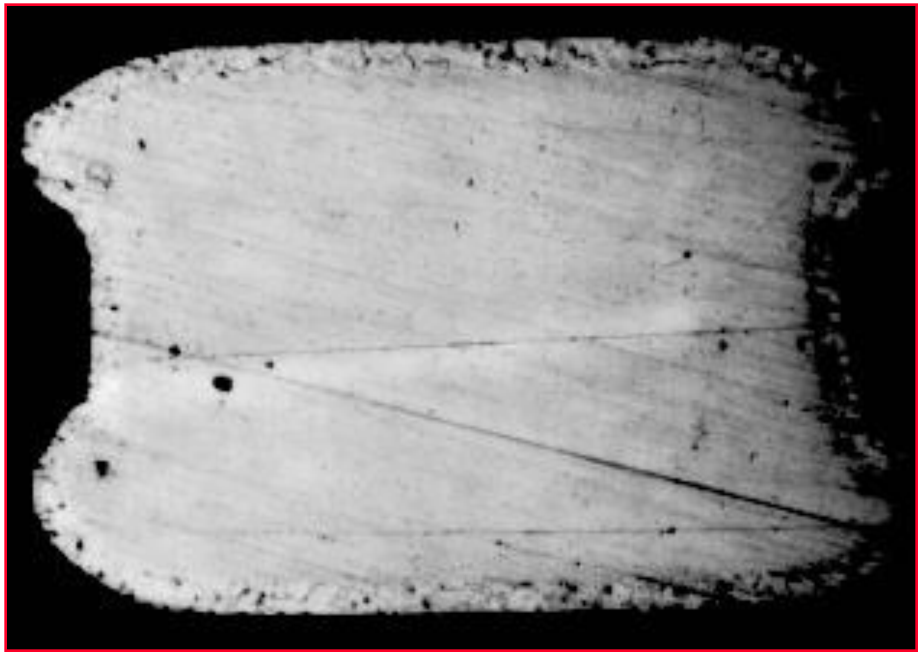


Post-plating solder plate

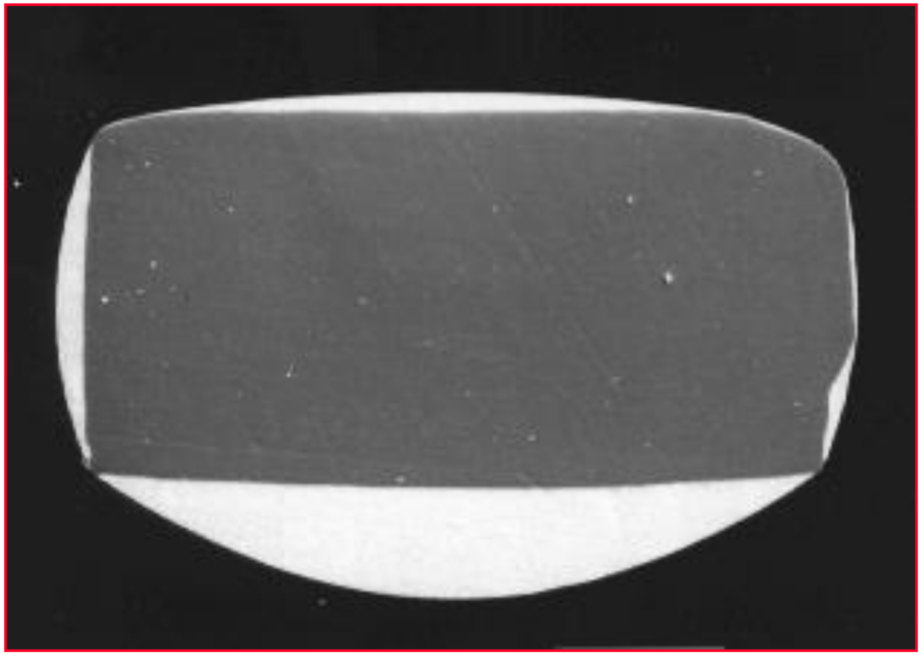


Post burn-in solder plate showing copper-tin intermetallic

Thermal Degradation of Lead Finish



X-section of solder-*plated* lead

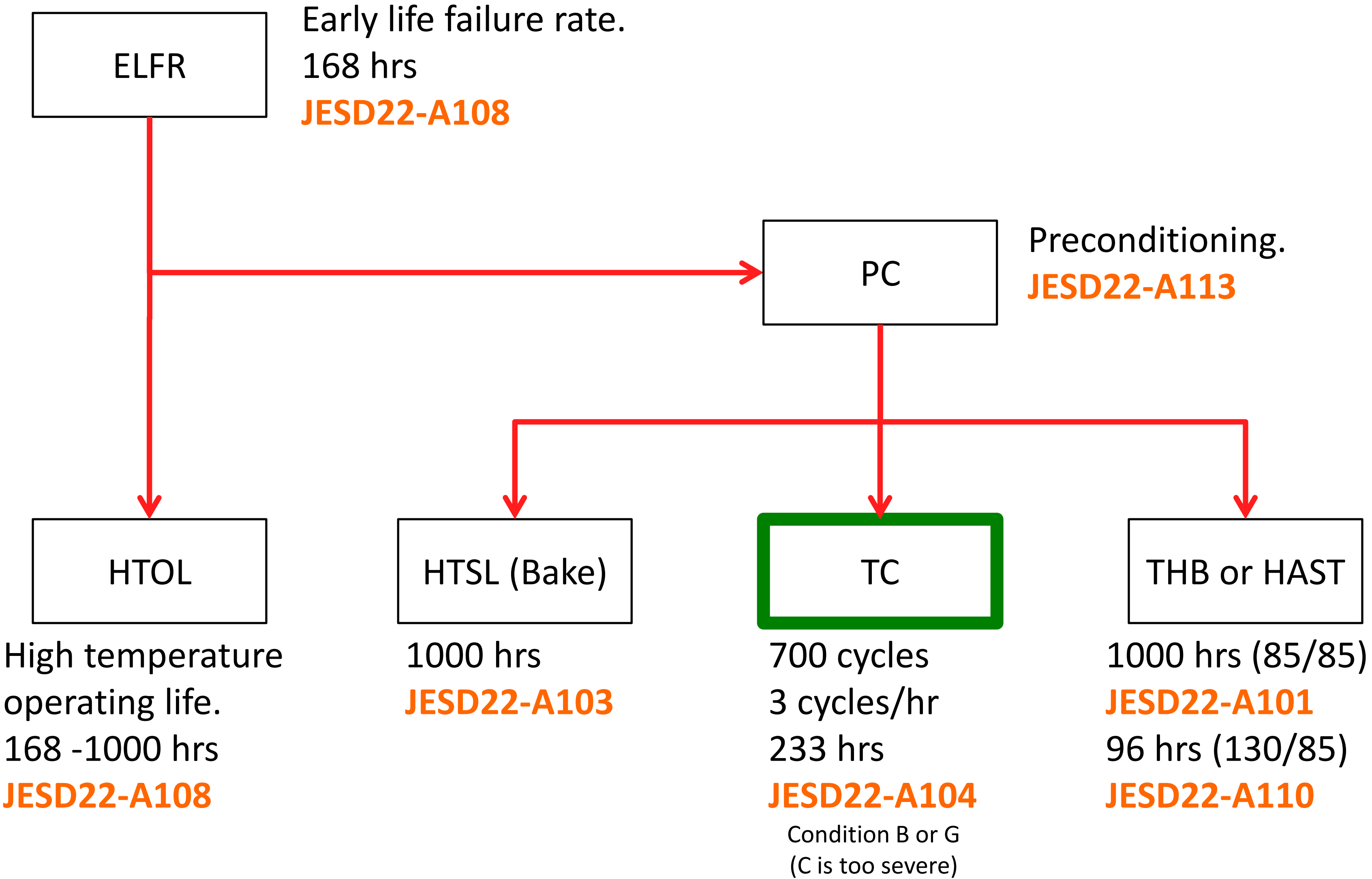


X-section of solder-*coated* lead

Outline

- Plastic Package Technology
- Stress and Test Flows
- Mechanisms
  - Moisture-mechanical
  - Moisture
  - Thermal
  - ● Thermo-mechanical

Thermomechanical Mechanisms



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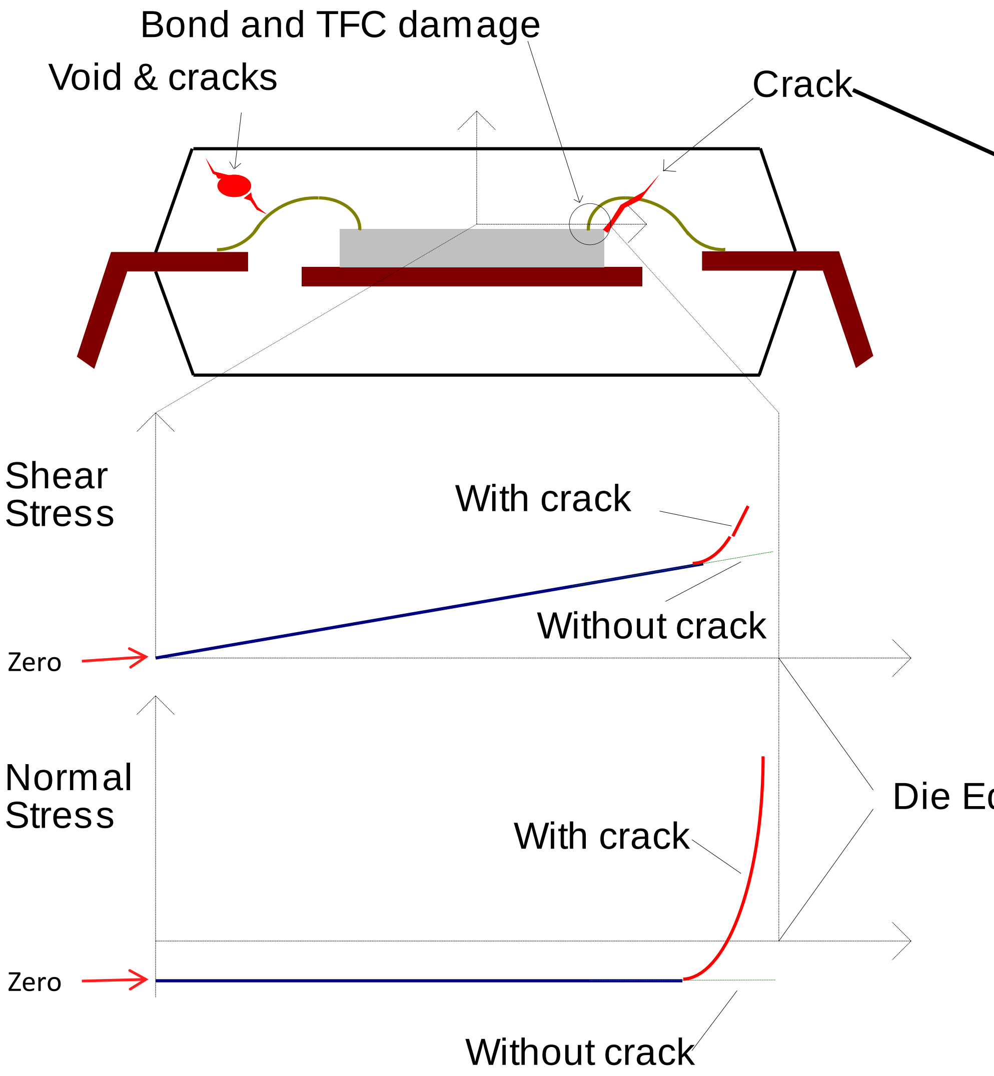
Condition B or G
(C is too severe)

THB or HAST

1000 hrs (85/85)
JESD22-A101
96 hrs (130/85)
JESD22-A110

Cracking Due to Temperature Cycle



Bond and TFC damage

Void & cracks

Crack

Shear Stress

With crack

Without crack

Zero

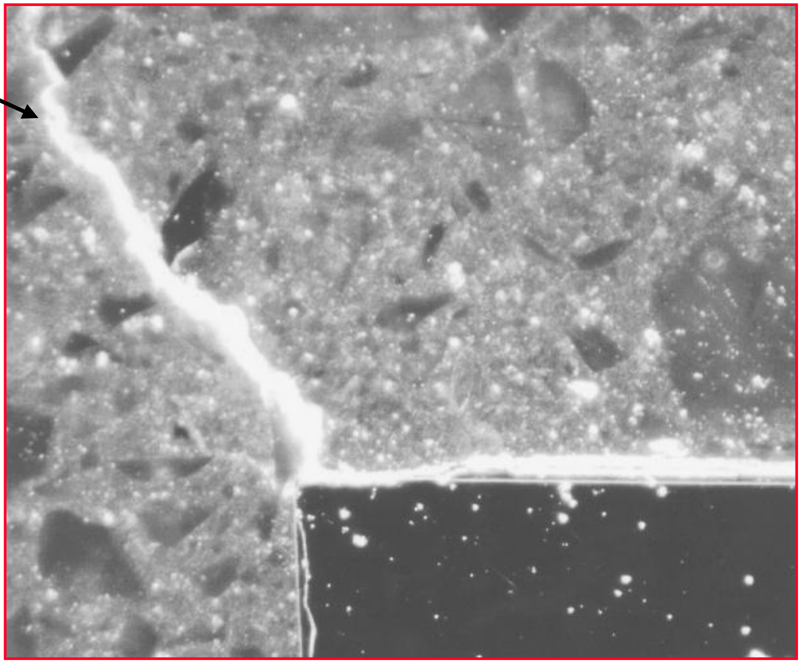
Normal Stress

With crack

Zero

Without crack

Die Edge



Crack Propagation in Package

- The rate of crack propagation is also given by

$$\frac{da}{dN} = Const \times (\Delta K)^m$$

- But in plastic packages under temperature cycling, the stress concentration factor is

Important

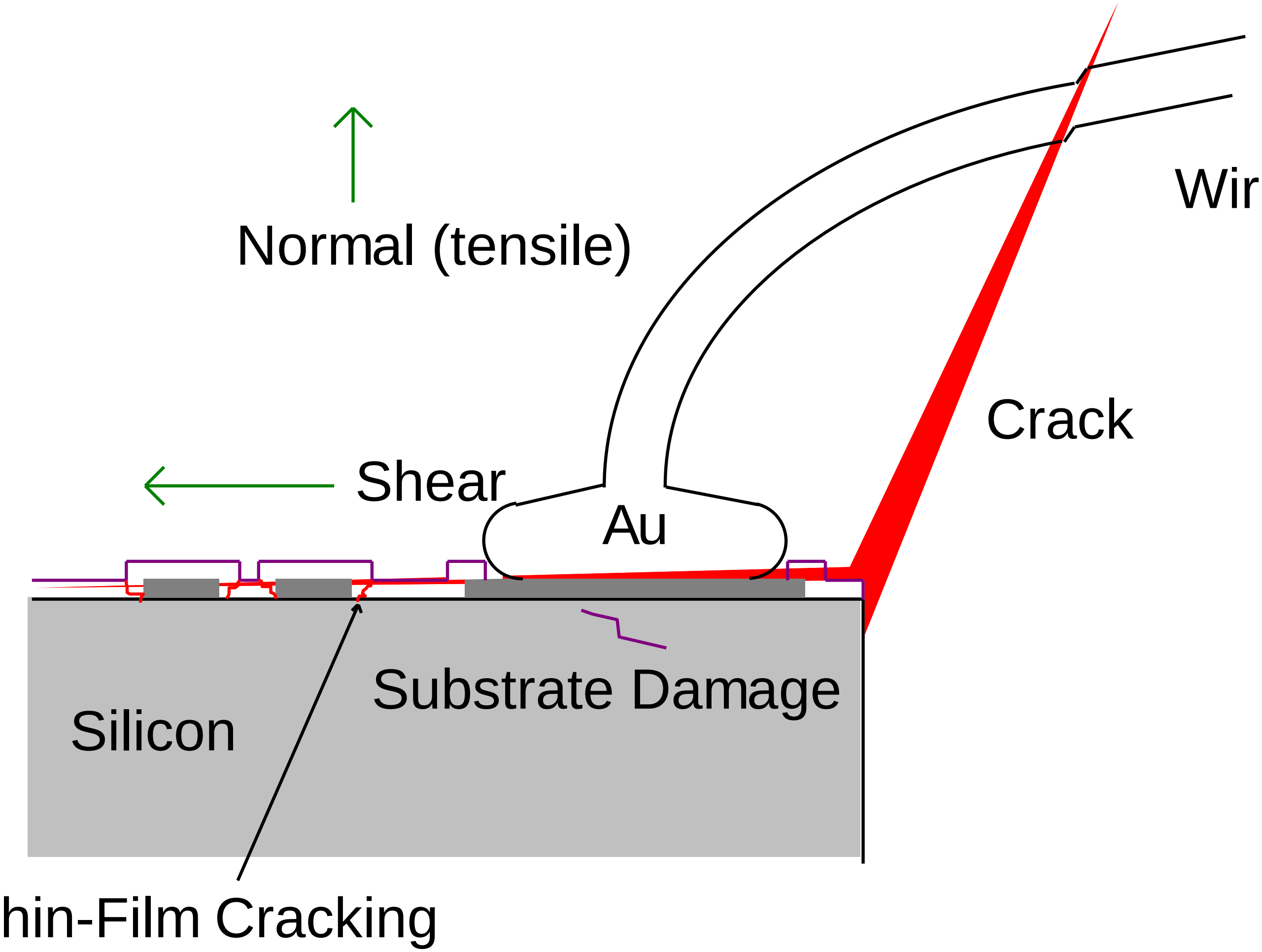
$$\Delta K = Const \times (\alpha_{moldingcompound} - \alpha_{silicon}) \times (T_{min} - T_{neutral})$$

- α is the TCE of MC.

ΔT in temperature cycling-driven models is the temperature difference between the neutral (usually cure) temperature, and the minimum temperature of the cycle. T_{max} is less important.

Package Cracking and Delamination..

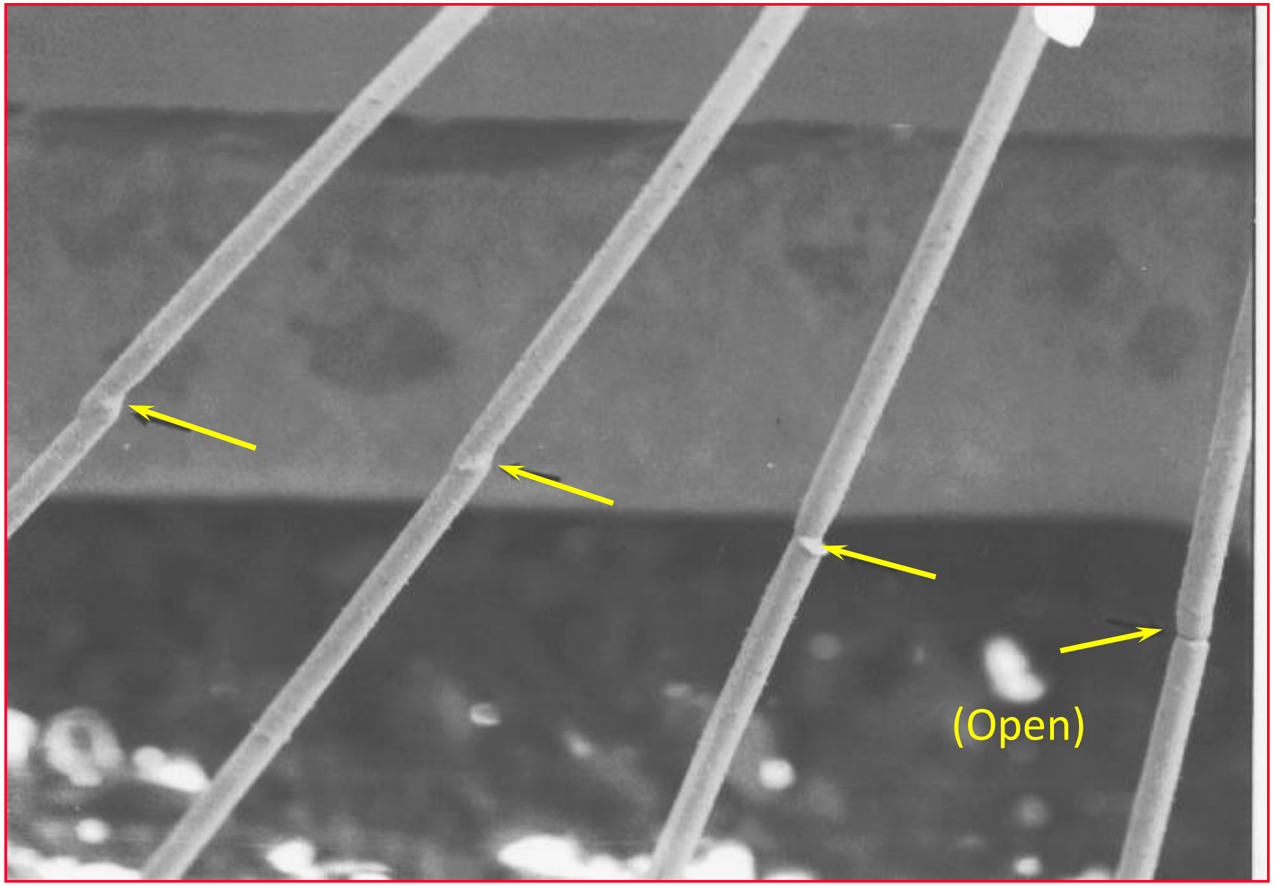
..damages Wires, Bonds, and Passivation Films.



Bond Damage: Wires and Ball Bonds

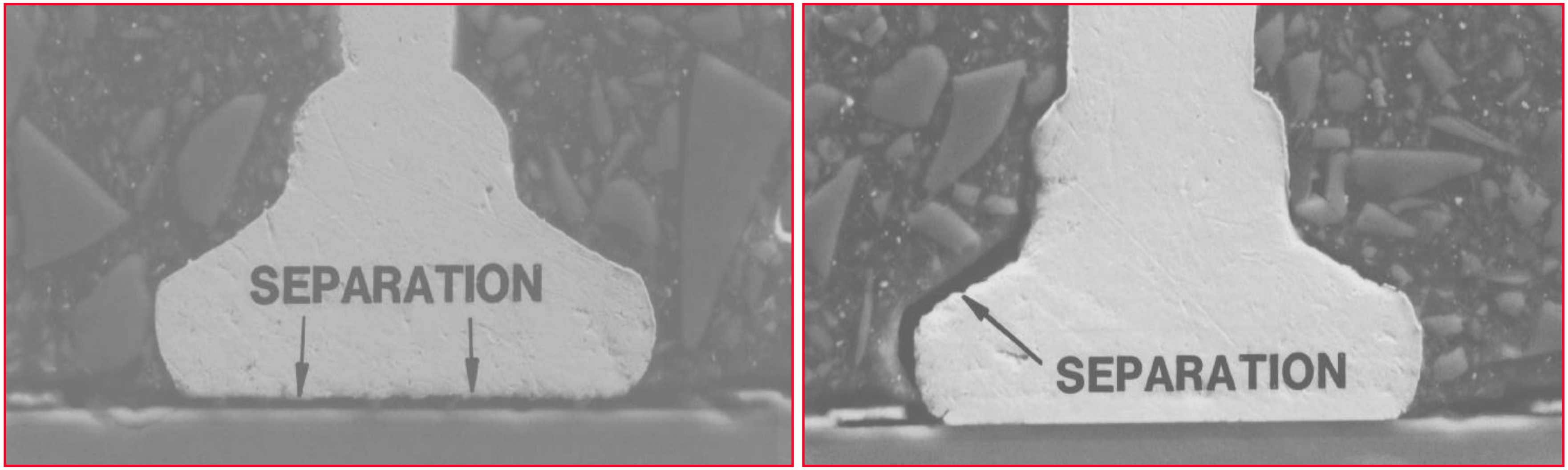
- Cracks can intersect wires, TAB leads.
- Bonds can be sheared at the bond/pad interface
- Shear and tensile normal stress can break wires at their necks.
- Substrate cracks induced during bonding can propagate and cause “cratering” or “chip-out”.

Wire Damage



Wires sheared by wire crack

Bond Damage



Sheared Bond

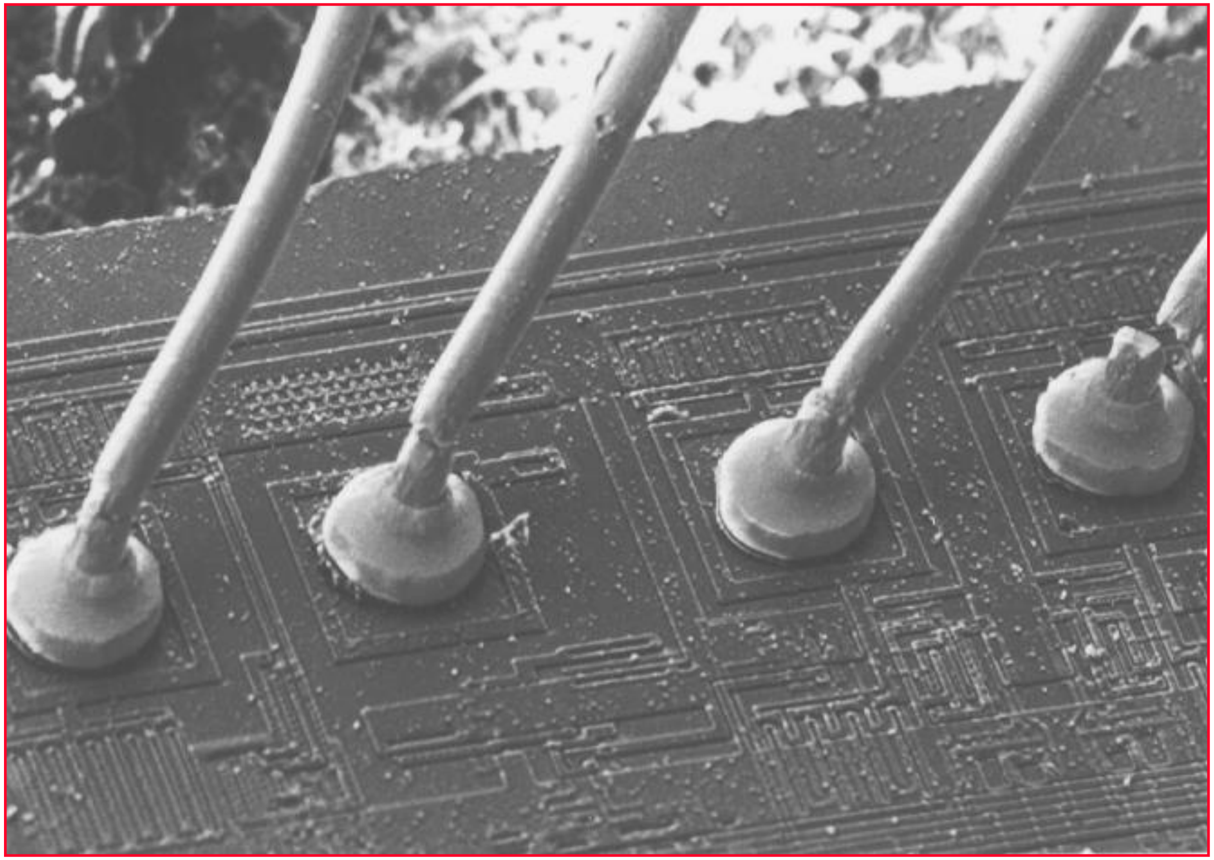
Unfailed Bond

20 μ

Die Corner →

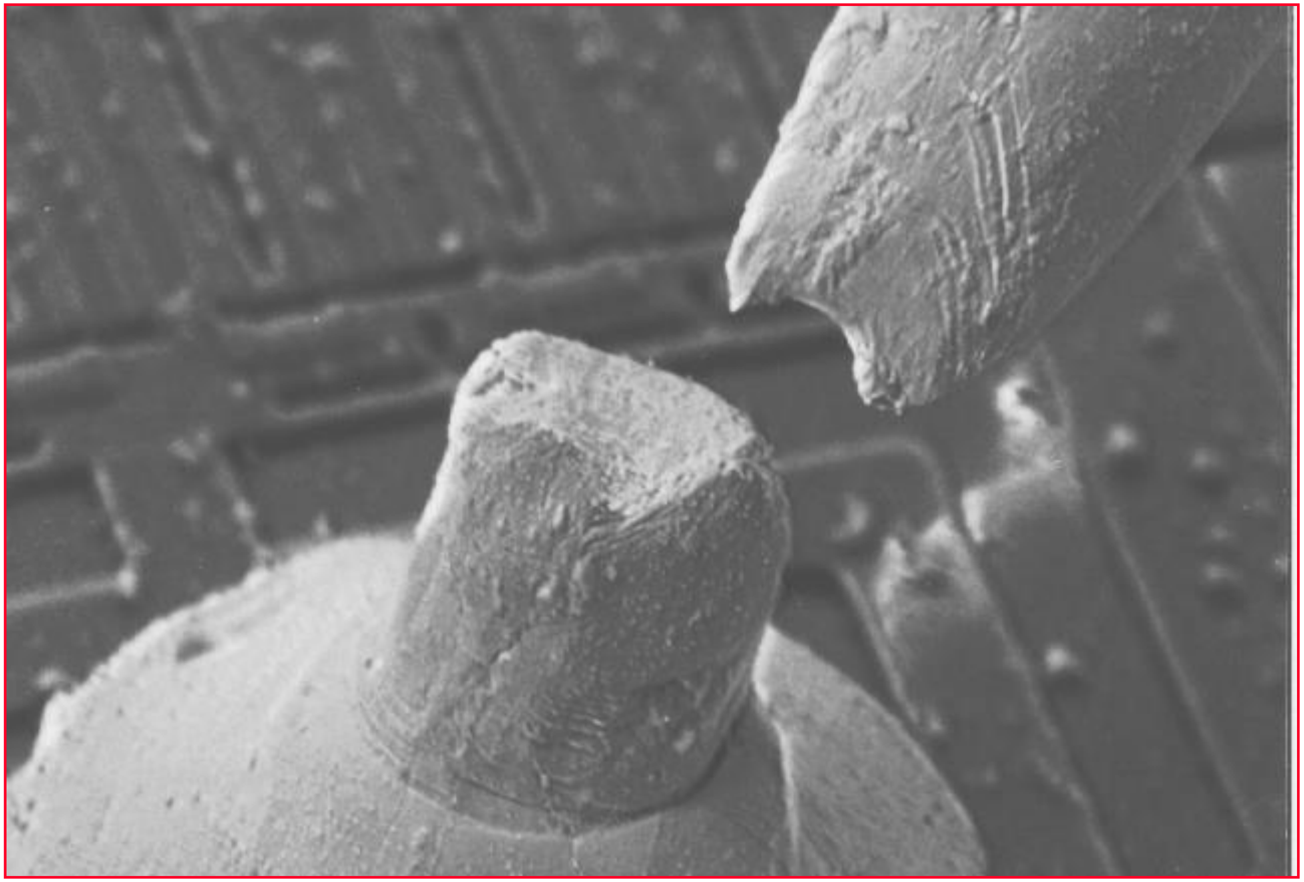
Ball bonds in plastic package after temperature cycle.

Bond Damage



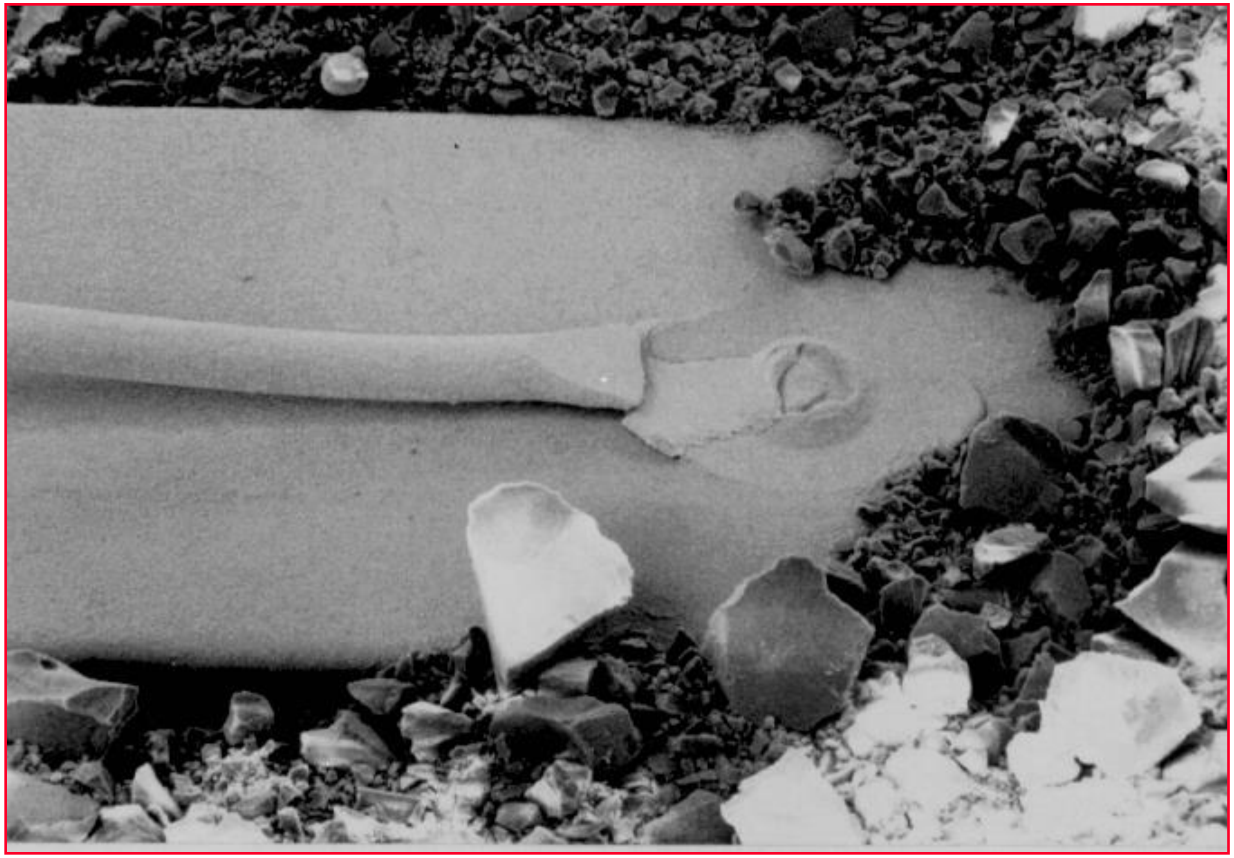
Necking Damage

Bond Damage



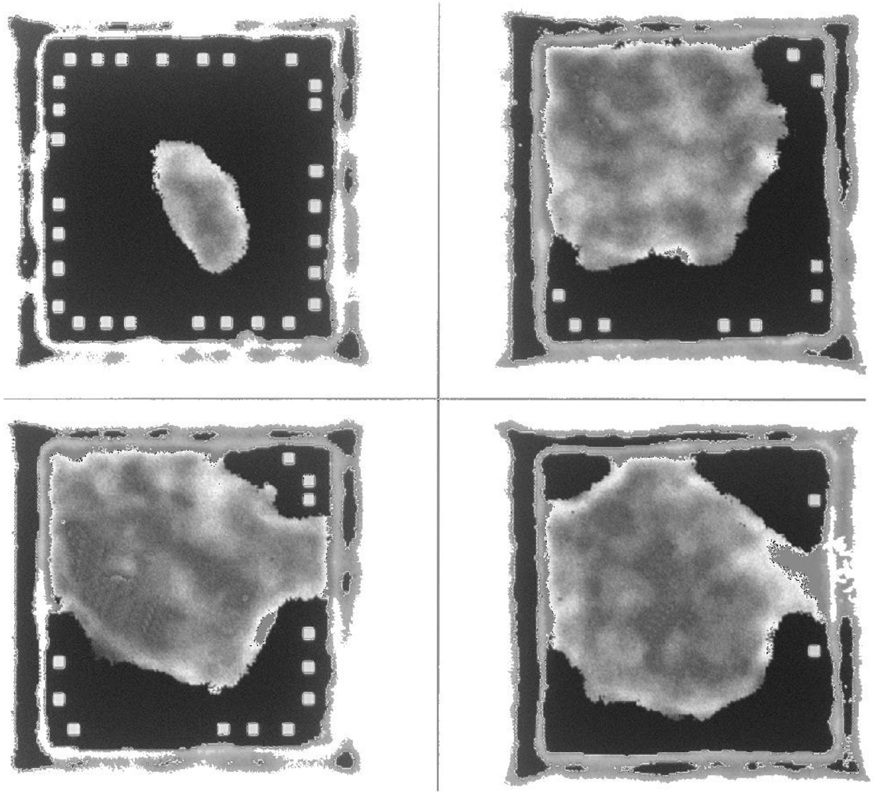
Necking fracture

Bond Damage

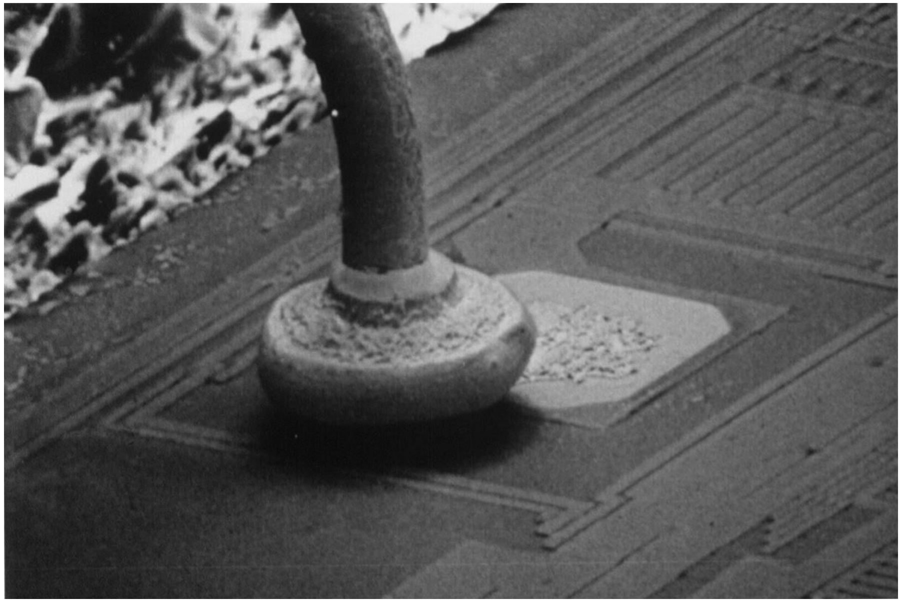


Delamination induced down bond fail after temperature cycle

Bond Damage and Delamination



Pulse-echo acoustic image of mold compound/ die interface in four devices. Delamination is shown in black. White boxes added to show locations of low bond wire pull strength results.

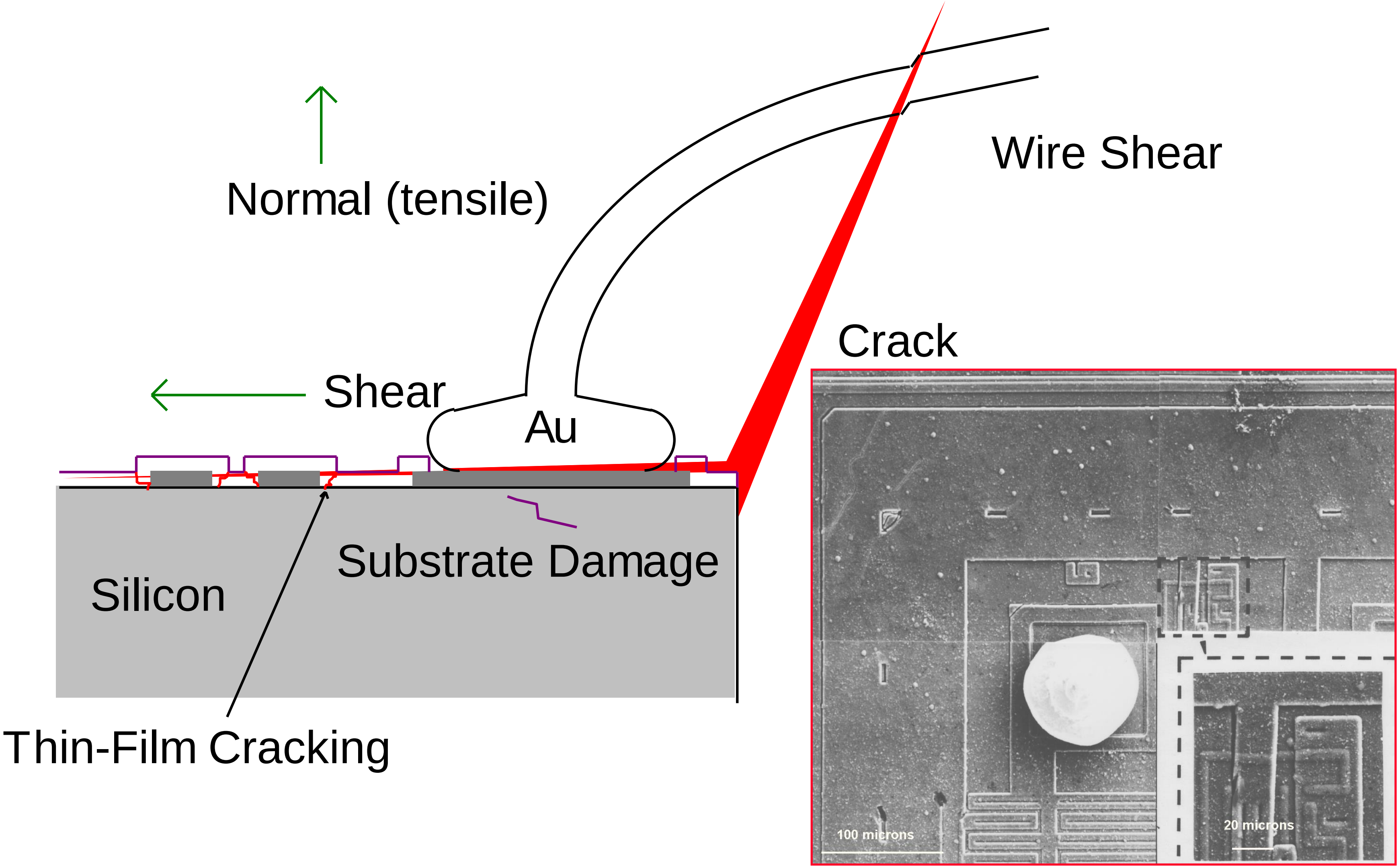


Intermetallic fracture at bond due to shear displacement.

44 PLCC devices that failed after solder reflow and 1000 cycles (-40 to 125C)

Source: T.M.Moore, R.G. McKenna and S.J. Kelsall, IRPS 1991, 160-166.

Thin-Film Cracking (TFC)



Normal (tensile)

Wire Shear

Shear

Au

Crack

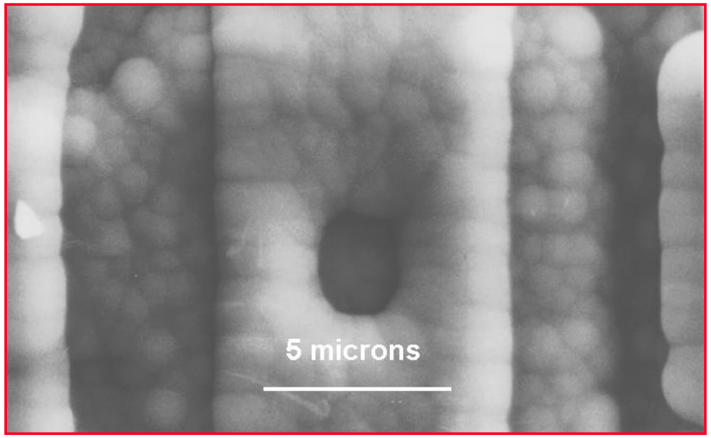
Silicon

Substrate Damage

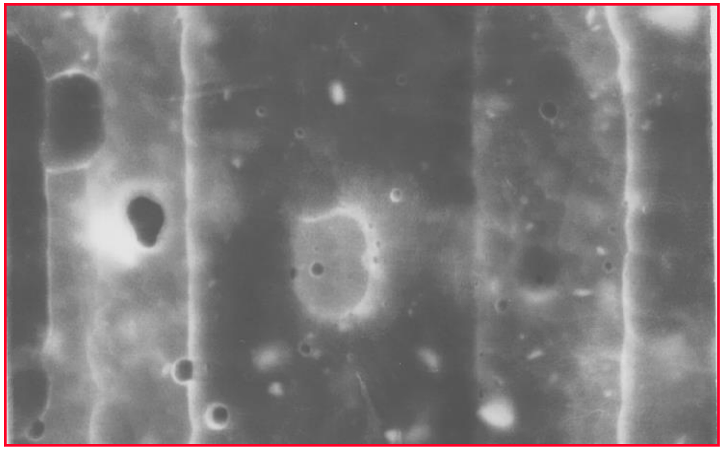
Thin-Film Cracking

TFC - Plastic Conforms to Die Surface

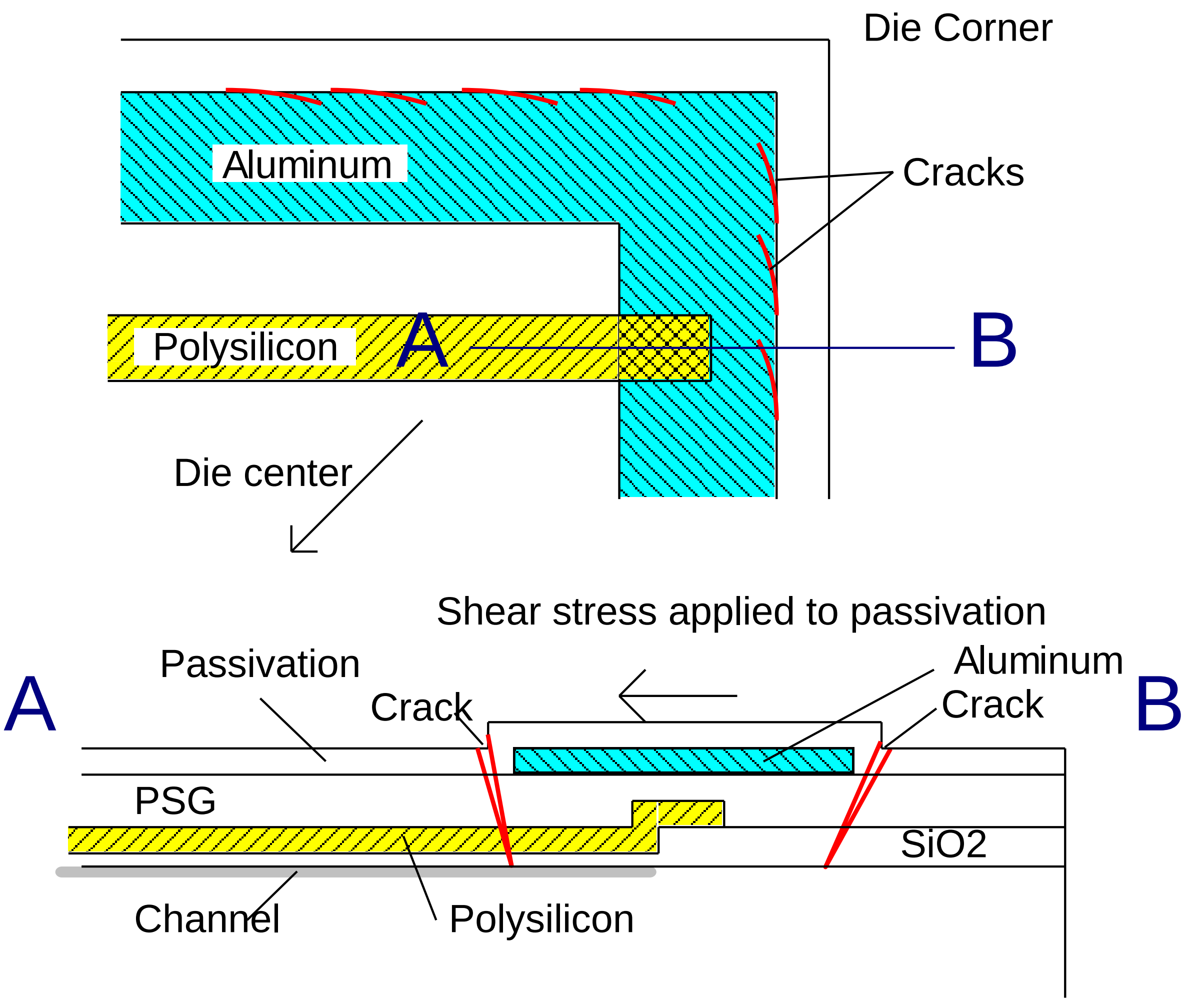
Die Surface



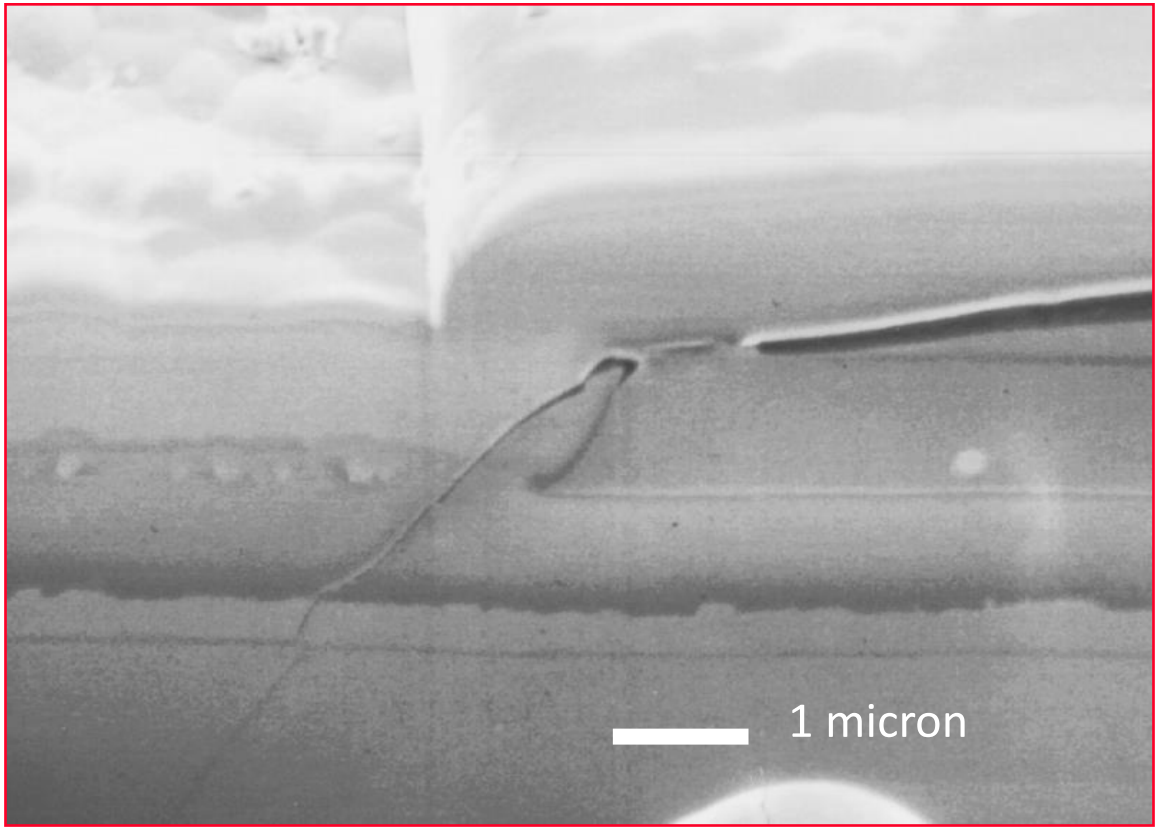
Replica in Plastic



TFC – Effect on Thin Films



Thin-Film Cracking (TFC)

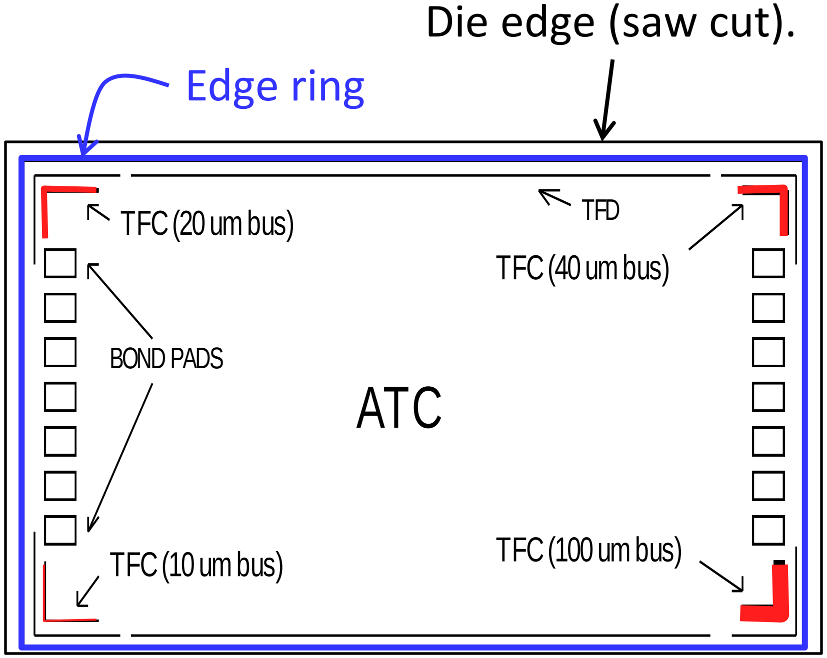


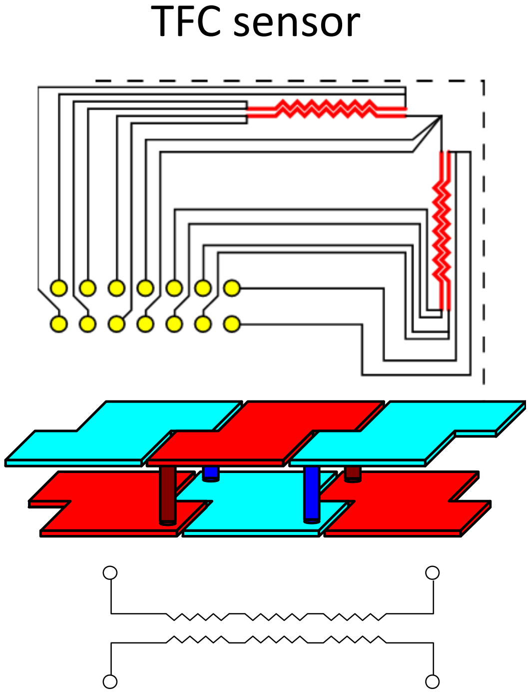
Source: K. Hayes, Intel

Passivation delamination crack propagates into substrate.

Test Chip - Thin Film Cracking

- Thin film cracking (TFC) can be detected electrically by test structures in the corner of the die.
  - Sensitive to opens and to shorts.
- Buss width is varied to determine design rule.

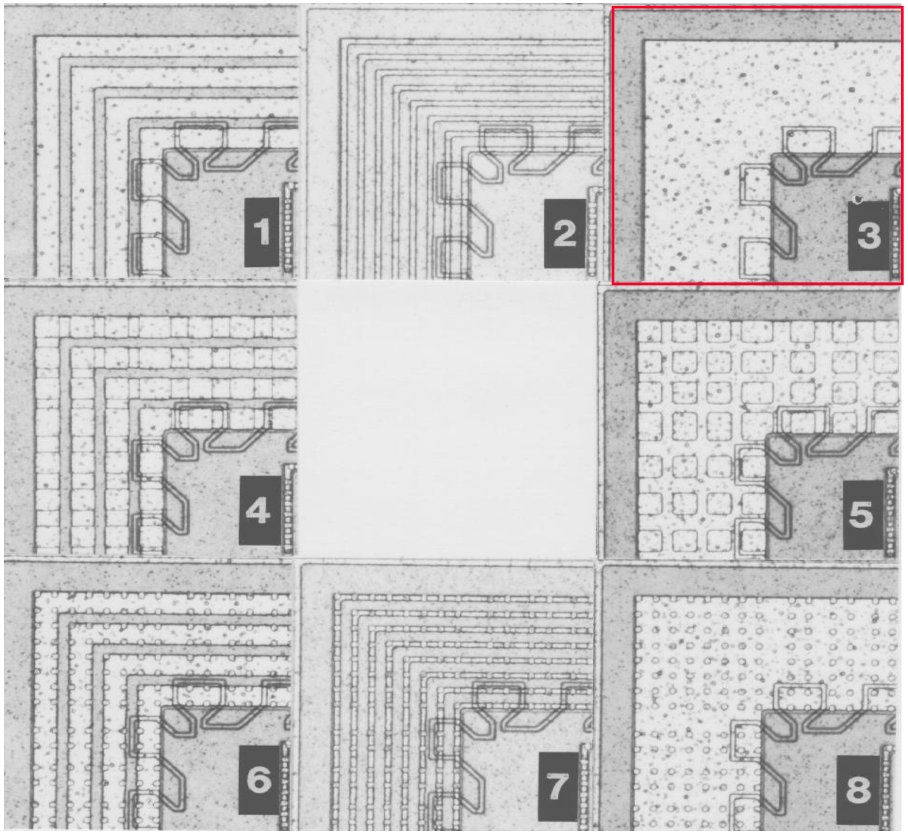




TFC – Effect of Buss Width

Factors Affecting TFC: Buss Width Effect

Polysilicon meanders under buss edge are vulnerable to crack-induced opens.



No Contacts

17 μ contacts

3 μ contacts

Buss Widths

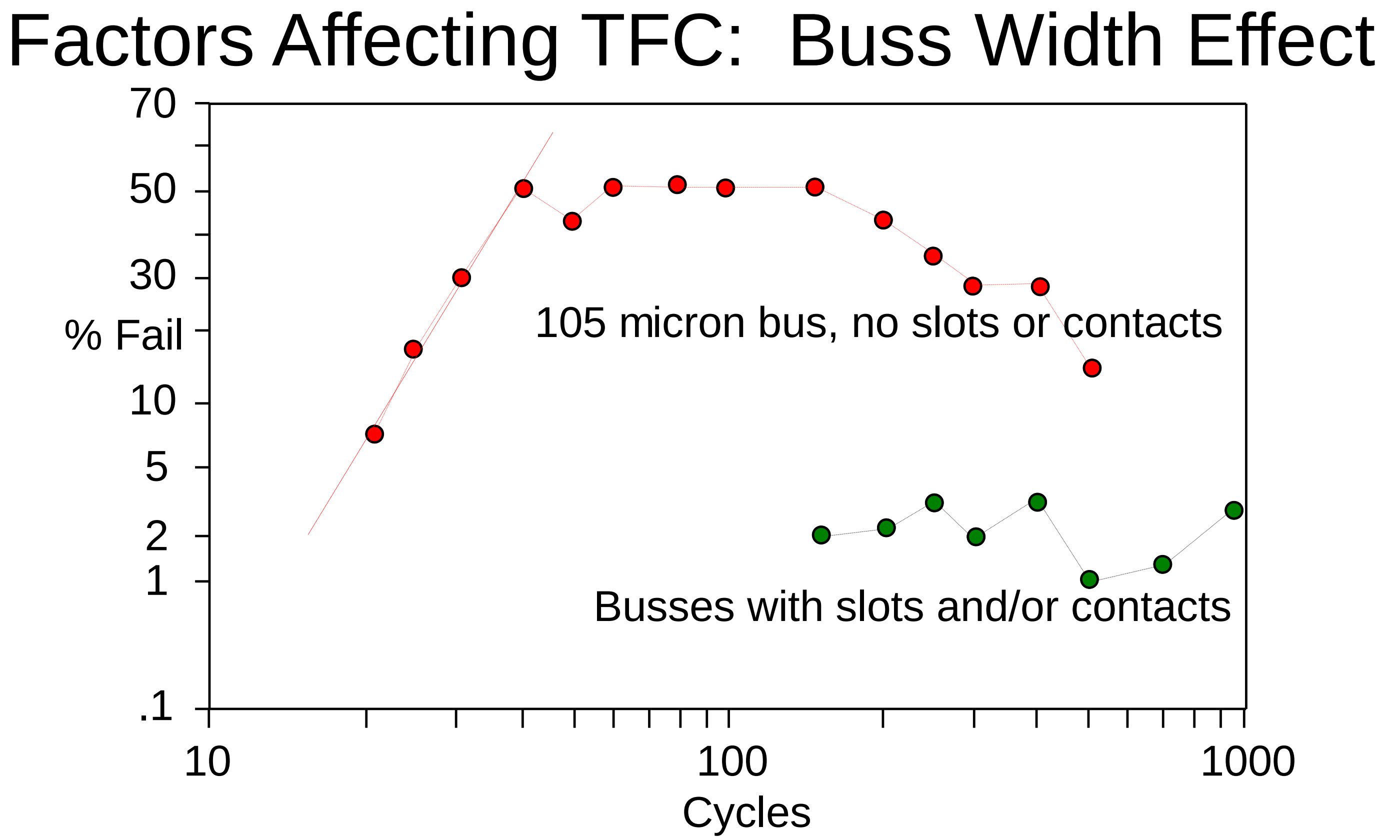
21 μ

7 μ

105 μ

Source: Shirley & Blish, "Thin Film Cracking and Wire Ball Shear...," IRPS 1987.

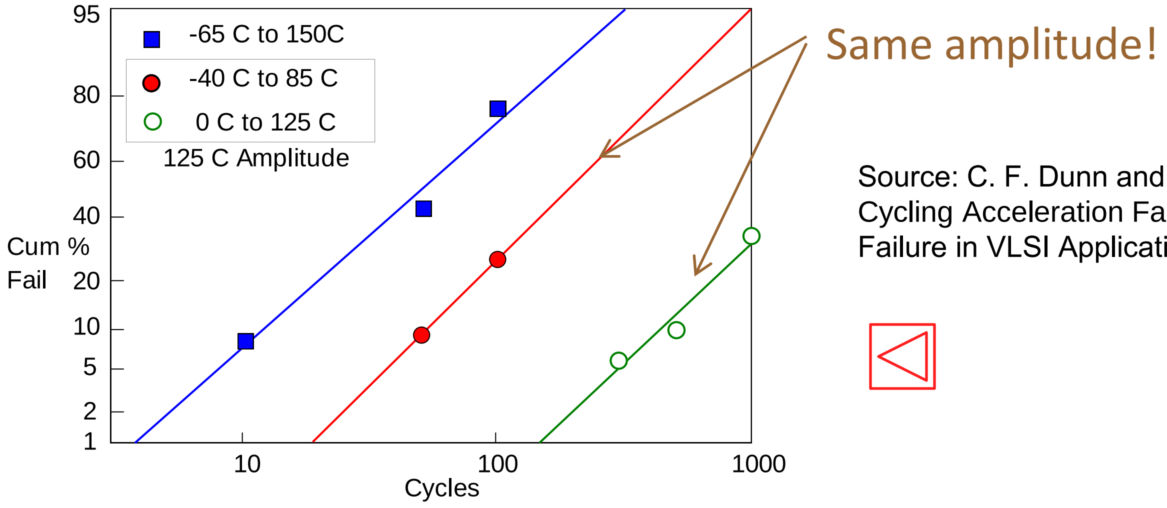
TFC – Effect of Buss Width, ct’d



Narrow buss, or contacts, stabilizes buss, reduces incidence of TFC. Leads to buss width design rules, and buss slotting in die corners.

TFC – Effect of Temperature Cycle

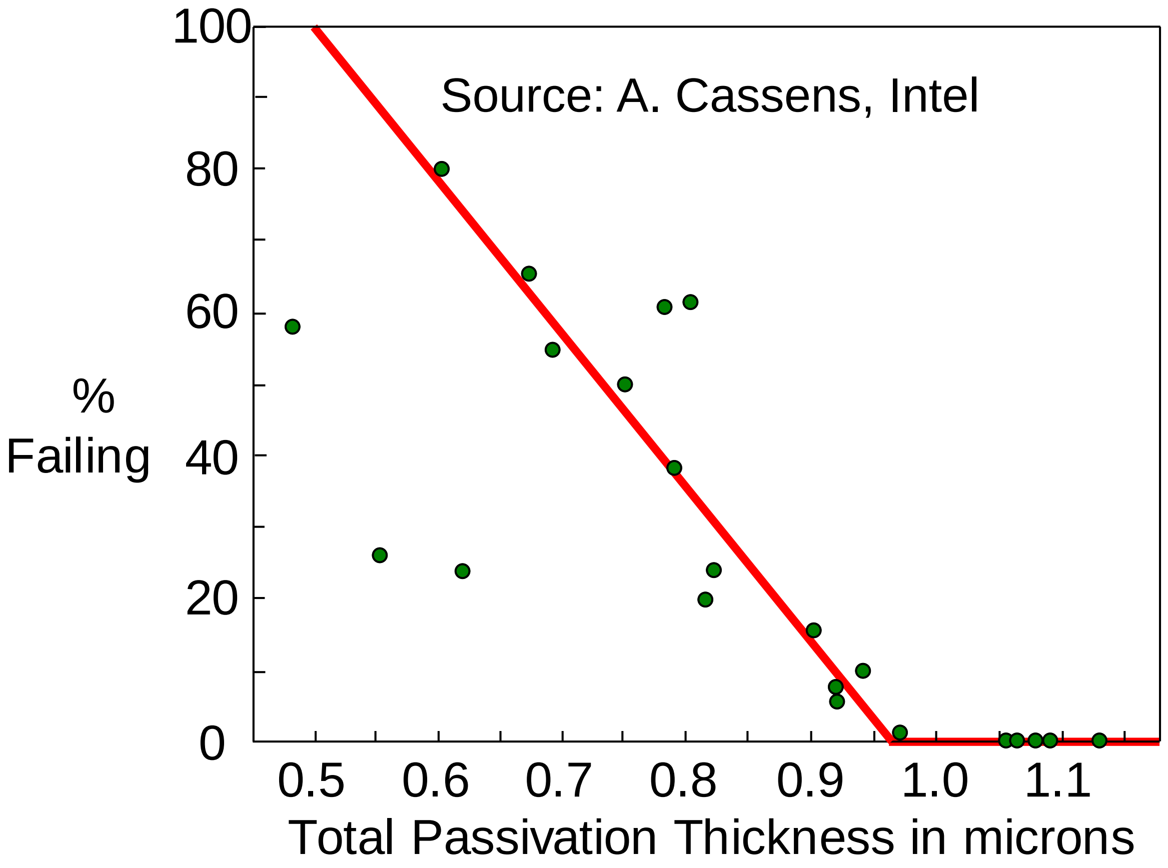
- Drivers: T/C conditions, and number of cycles.
- Mimimum T/C temperature, not amplitude, is key aspect of stress.
  - Stress depends on difference between cure temperature (neutral stress) and minimum stress temperature.



Source: C. F. Dunn and J. W. McPherson, “Temperature-Cycling Acceleration Factors for Aluminum Metallization Failure in VLSI Applications,” IRPS, 1990.

TFC – Effect of Passivation Thickness

- Fraction of PDIP-packaged SRAM failing.
- Post 1K cycle of T/C C.
- No Polyimide die coat.
- Thicker passivation is more robust.



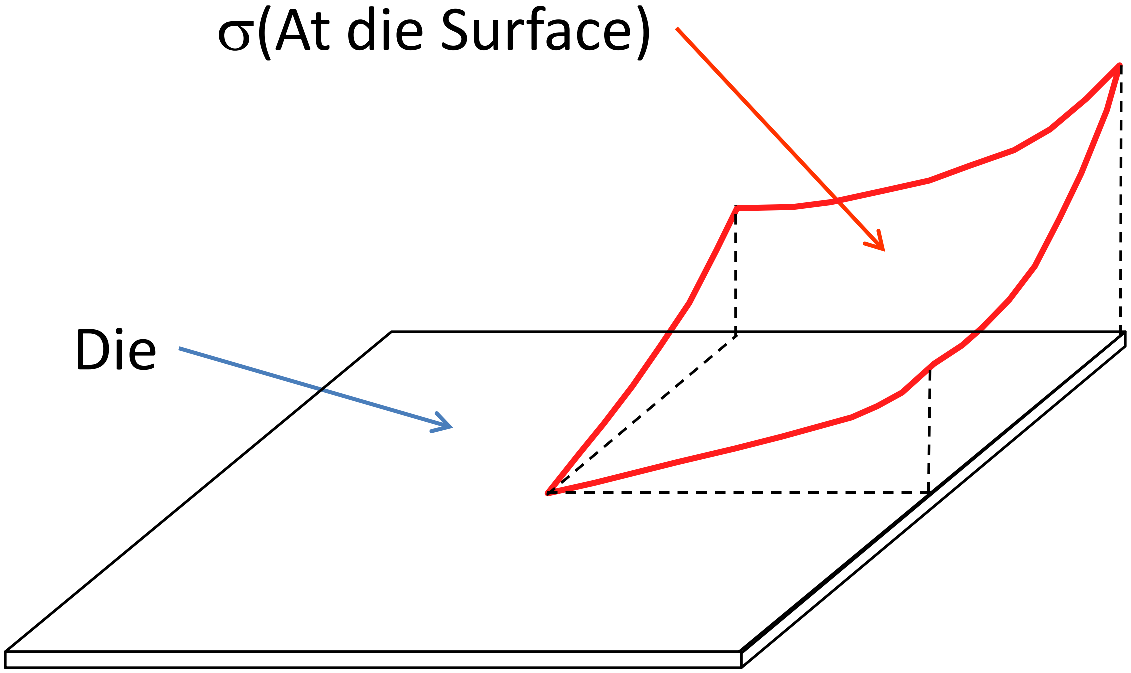
TFC – Effect of Compliant Overcoat

- SRAM in PDIP
- Temperature Cycle Condition C
- Polyimide Overcoat

	200 cycles	500 cycles	1000 cycles
No Polyimide	0/450	13/450	101/437
Polyimide	0/450	0/450	0/450

Theory of TFC

- Shear stress applied to die surface by MC
  - Is maximum at die corners
  - Zero at die center.



Theory of TFC, ct’d

- Buss width effect: Okikawa et. al.
- Passivation thickness effect: Edwards et al.
- TFC occurs when and where

$$\sigma(\text{Passivation Surface}) > \underbrace{K \times E \times \left(\frac{t}{L}\right)^2}_{\text{Local strength of passivation.}}$$

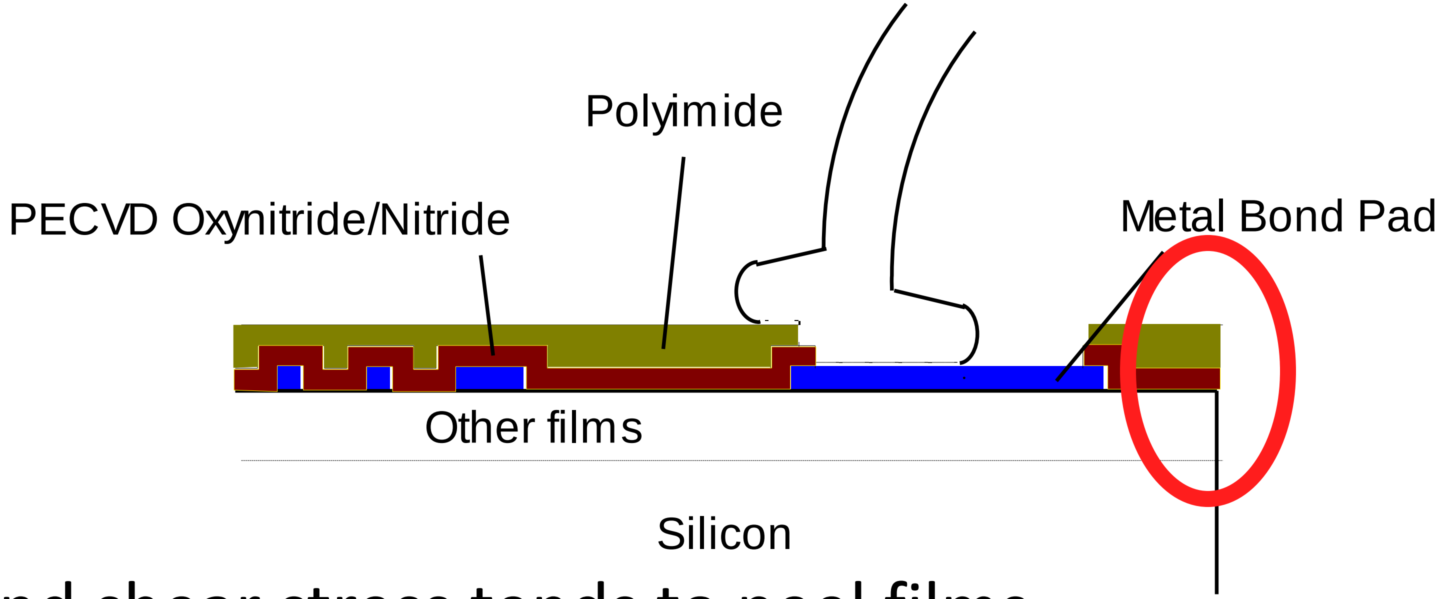
  - *K* = dimensionless constant
  - *E* = Young’s modulus of passivation
  - *t* = Passivation thickness
  - *L* = Buss width

Thicker passivation, and/or narrower busses implies less TFC.

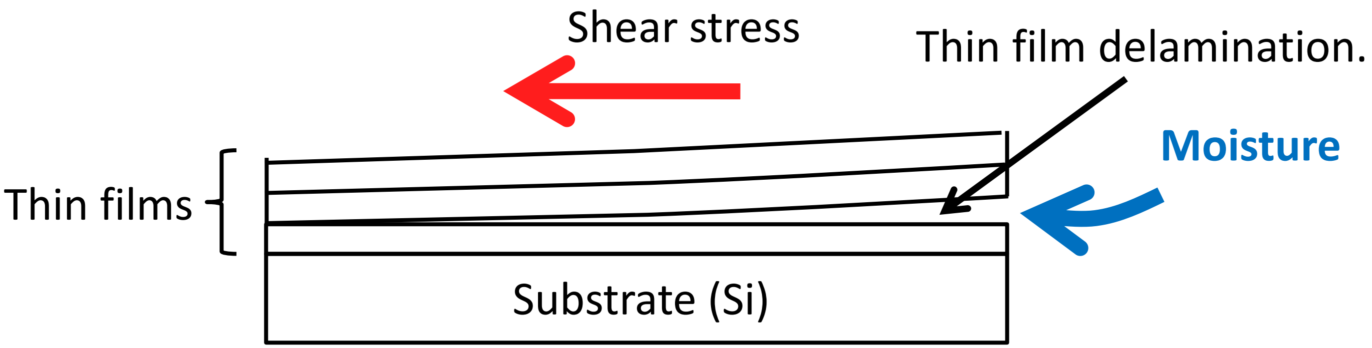
Sources: Okikawa, et al. ISTFA, Oct. 1983. Edwards, et al. IEEE-CHMT-12, p 618, 1987

Thin Film Moisture Delamination

- Saw cut exposes thin film edges to moisture..

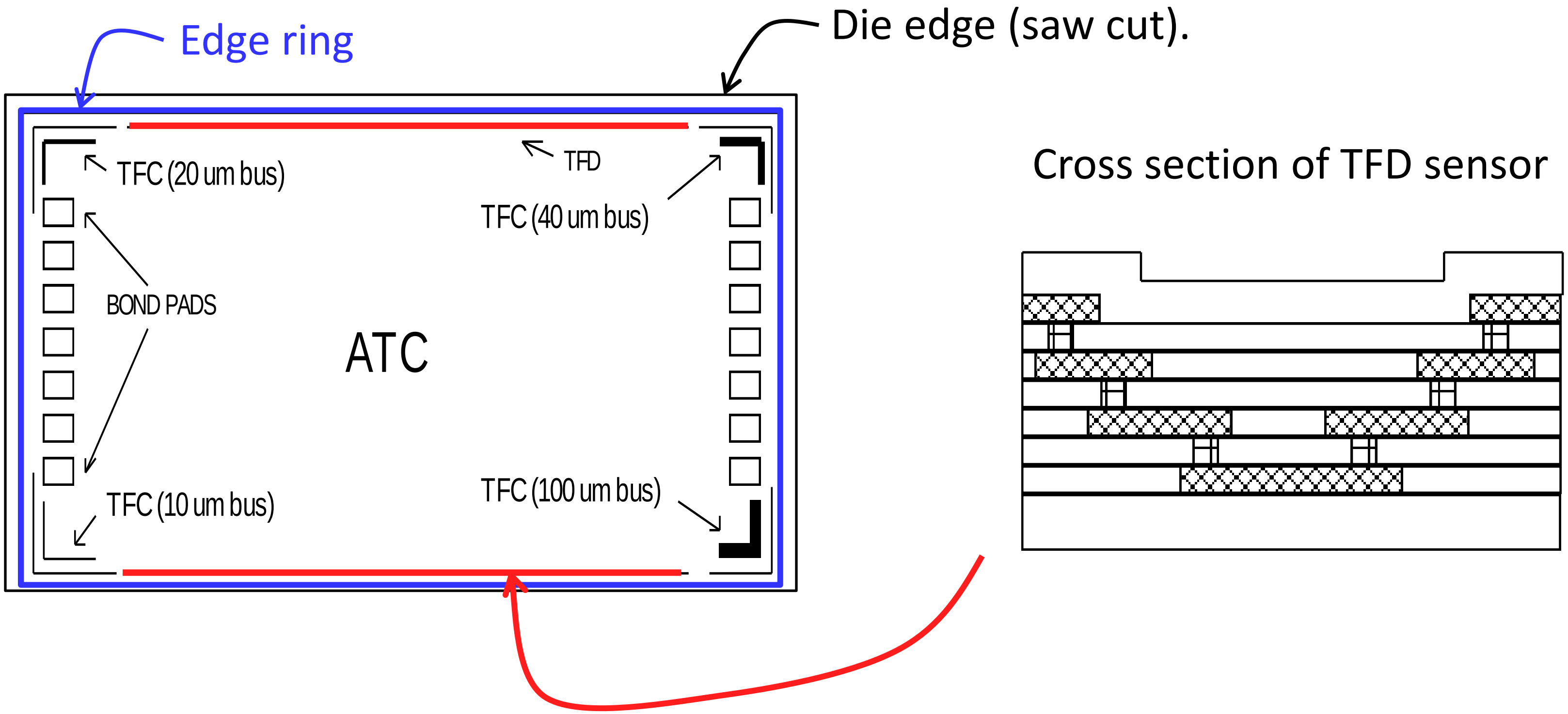


- And shear stress tends to peel films.

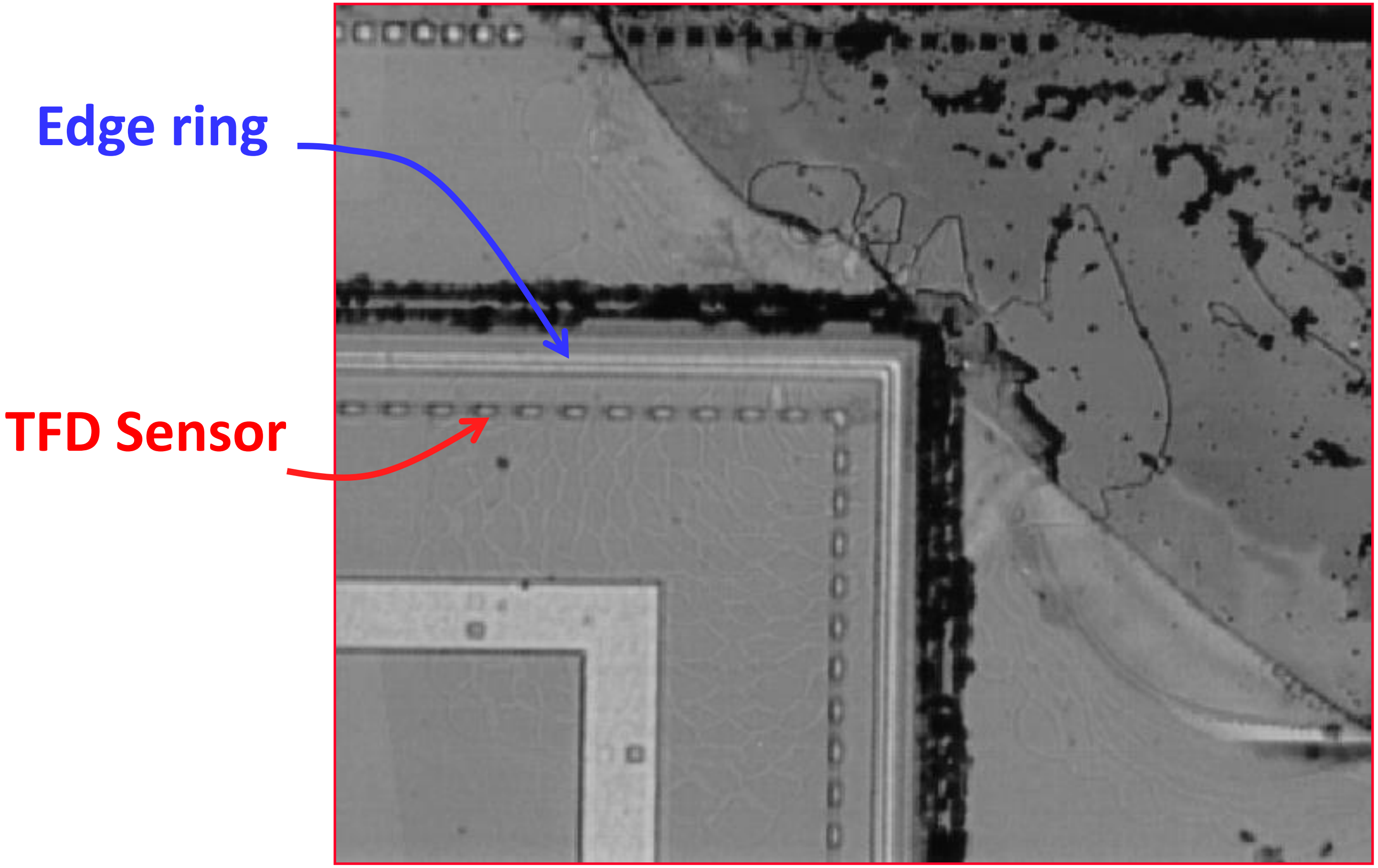


Test Chip – Thin Film Delamination

- “Edge rings” are lateral moisture barrier.
- Effectiveness of edge rings can be tested electrically by a thin-film delamination (TFD) sensor.



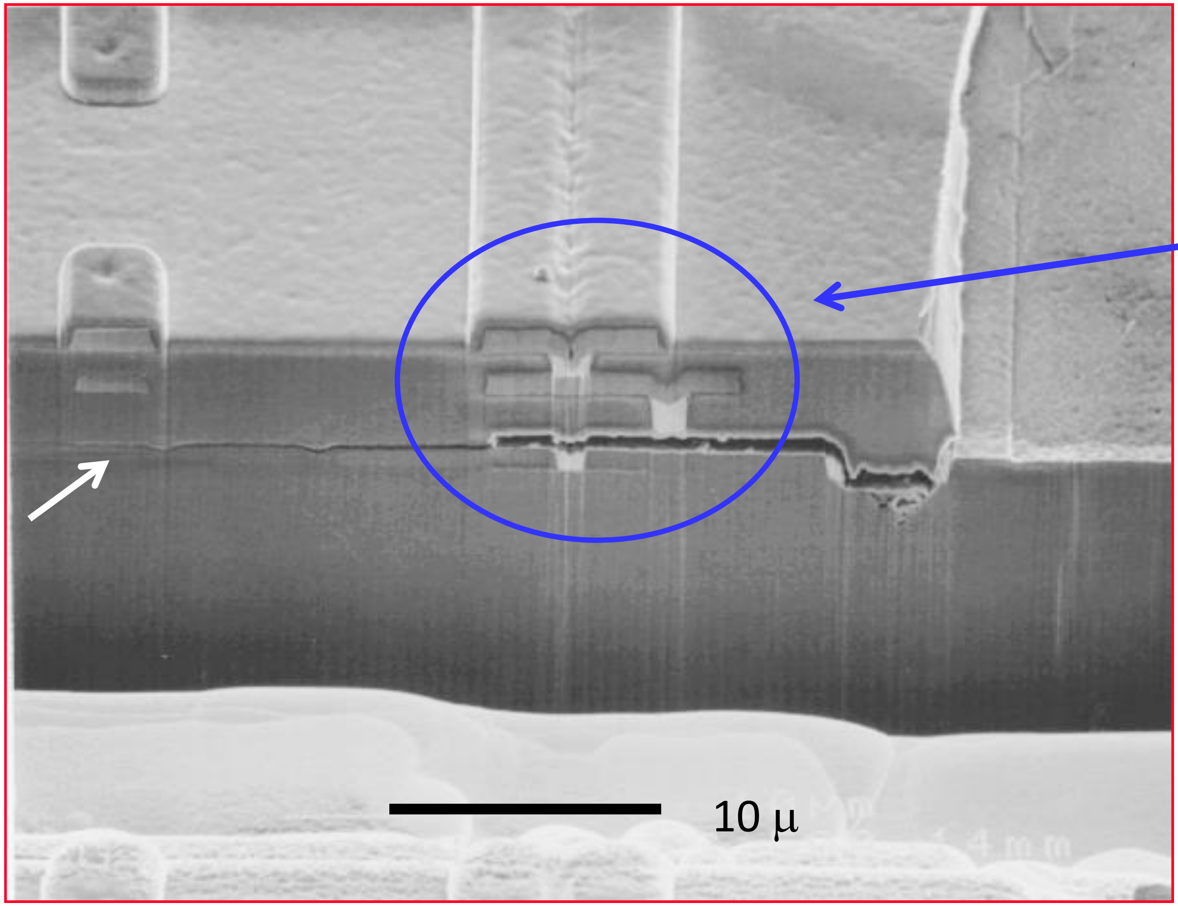
Thin-Film Delamination



Source: C. Hong
Intel

Delamination at die edge after 168 hours of steam.

Thin-Film Delamination



Edge Ring

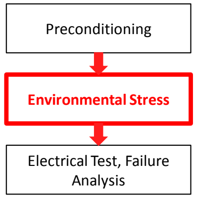
Crack breaks continuity of

TFD sensor

Source: C. Hong
Intel

Delamination at die edge after 168 hours of steam.

Backup


Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Reliability Goals from ITRS 2009

http://www.itrs.net/reports.html

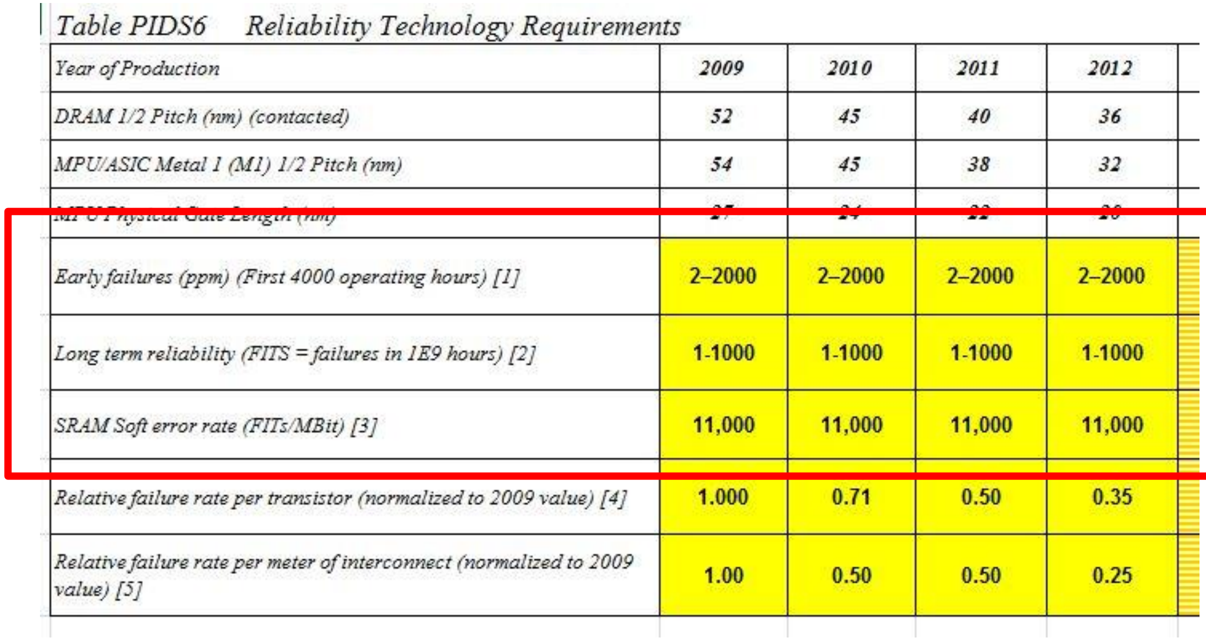


Table PIDS6 Reliability Technology Requirements

Year of Production	*2009*	*2010*	*2011*	*2012*
DRAM 1/2 Pitch (nm) (contacted)	*52*	*45*	*40*	*36*
MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)	*54*	*45*	*38*	*32*
MPU Physical Gate Length (nm)	*27*	*24*	*22*	*20*
Early failures (ppm) (First 4000 operating hours) [1]	2–2000	2–2000	2–2000	2–2000
Long term reliability (FITS = failures in 1E9 hours) [2]	1-1000	1-1000	1-1000	1-1000
SRAM Soft error rate (FITs/MBit) [3]	11,000	11,000	11,000	11,000
Relative failure rate per transistor (normalized to 2009 value) [4]	1.000	0.71	0.50	0.35
Relative failure rate per meter of interconnect (normalized to 2009 value) [5]	1.00	0.50	0.50	0.25

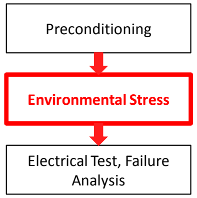
Infant Mortality

Wear-out

Constant fail rate

Sampling

- **JESD47** sample requirements are minimal.
  - Single "snapshot" is a crude validation of the reliability of the product.
  - Small SS does not generate failures to give clues to process weaknesses.
- Risks.
  - Qualification hinges on single failures.
    - Moral hazard to "invalidate" a failure is high.
  - Lot-to-lot variation, excursions.
    - Incoming materials, fab lots, assembly lots, test lots.



Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Sampling, ct’d

- Number of lots covers risks of machine-to machine, day-to-day, etc. variation.
- Often minimum SS to validate a goal is chosen.
  - Pro: Saves $, and there are no failures to explain.
  - Con: Pass/fail of the qual is at the mercy of a single failure.
    - Verrry tempting to invalidate a failure.
  - Con: No mechanism learning.

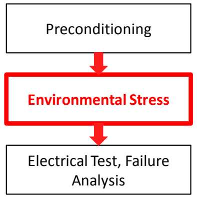
(Accept/Reject $\Rightarrow$ 0/1)

- eg. To validate 500 DPM at ELFR using minimum SS at 60% confidence, 1833 units are required.
  - 500 DPM is a typical goal (see ITRS)

$$SS = \frac{-\ln(1-cl)}{D}$$

Useful “mental furniture”

$$1833 = \frac{-\ln(1-0.6)}{500\times10^{-6}}$$


Preconditioning

Environmental Stress

Electrical Test, Failure Analysis

Sampling, ct'd

- For environmental stress, 77 is a typical SS, why?

$$SS=\frac{-\ln(1-cl)}{D};\quad \frac{-\ln(1-0.9)}{3\times10^{-2}}=\frac{-\ln(.1)\times100}{3}=\frac{230.26}{3}=76.7$$

  - So, 0/1 accept/reject validates, to 90% confidence, a failure rate less than 3% at the accelerated condition.

- If the stress corresponds to the lifetime (eg. 7 years) then the average wearout failure rate is

$$FR=\frac{3\times10^{-2}}{7\times365\times24}\times10^{9}=489\ \ Fits$$

  - This falls into the range of ITRS goals.

Example Data

- Additional attributes enhance value of data.
  - Device type
  - Date code
  - Package type
  - Readouts
  - Failure analysis

Maxim product reliability report RR-1H

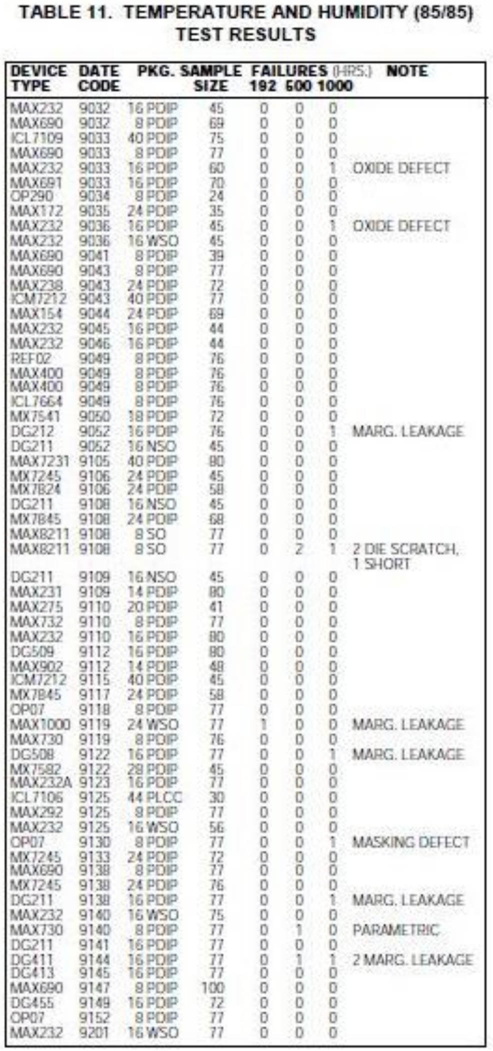


TABLE 11. TEMPERATURE AND HUMIDITY (85/85) TEST RESULTS

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS.)			NOTE
				192	500	1000	
MAX232	9032	16 PDIP	45	0	0	0	
MAX690	9032	8 PDIP	69	0	0	0	
ICL7109	9033	40 PDIP	75	0	0	0	
MAX690	9033	8 PDIP	77	0	0	0	
MAX232	9033	16 PDIP	60	0	0	1	OXIDE DEFECT
MAX691	9033	16 PDIP	70	0	0	0	
OP290	9034	8 PDIP	24	0	0	0	
MAX172	9035	24 PDIP	35	0	0	0	
MAX232	9036	16 PDIP	45	0	0	1	OXIDE DEFECT
MAX232	9036	16 WSO	45	0	0	0	
MAX690	9041	8 PDIP	39	0	0	0	
MAX690	9043	8 PDIP	77	0	0	0	
MAX238	9043	24 PDIP	72	0	0	0	
ICM7212	9043	40 PDIP	77	0	0	0	
MAX154	9044	24 PDIP	69	0	0	0	
MAX232	9045	16 PDIP	44	0	0	0	
MAX232	9046	16 PDIP	44	0	0	0	
REF02	9049	8 PDIP	76	0	0	0	
MAX400	9049	8 PDIP	76	0	0	0	
MAX400	9049	8 PDIP	76	0	0	0	
ICL7664	9049	8 PDIP	76	0	0	0	
MX7541	9050	18 PDIP	72	0	0	0	
DG212	9052	16 PDIP	76	0	0	1	MARG. LEAKAGE
DG211	9052	16 NSO	45	0	0	0	
MAX7231	9105	40 PDIP	80	0	0	0	
MX7245	9106	24 PDIP	45	0	0	0	
MX7824	9106	24 PDIP	58	0	0	0	
DG211	9108	16 NSO	45	0	0	0	
MX7845	9108	24 PDIP	68	0	0	0	
MAX8211	9108	8 SO	77	0	0	0	
MAX8211	9108	8 SO	77	0	2	1	2 DIE SCRATCH, 1 SHORT
DG211	9109	16 NSO	45	0	0	0	
MAX231	9109	14 PDIP	80	0	0	0	
MAX275	9110	20 PDIP	41	0	0	0	
MAX732	9110	8 PDIP	77	0	0	0	
MAX232	9110	16 PDIP	80	0	0	0	
DG509	9112	16 PDIP	80	0	0	0	
MAX902	9112	14 PDIP	48	0	0	0	
ICM7212	9115	40 PDIP	45	0	0	0	
MX7845	9117	24 PDIP	58	0	0	0	
OP07	9118	8 PDIP	77	0	0	0	
MAX1000	9119	24 WSO	77	1	0	0	MARG. LEAKAGE
MAX730	9119	8 PDIP	76	0	0	0	
DG508	9122	16 PDIP	77	0	0	1	MARG. LEAKAGE
MX7582	9122	28 PDIP	45	0	0	0	
MAX232A	9123	16 PDIP	77	0	0	0	
ICL7106	9125	44 PLCC	30	0	0	0	
MAX292	9125	8 PDIP	77	0	0	0	
MAX232	9125	16 WSO	56	0	0	0	
OP07	9130	8 PDIP	77	0	0	1	MASKING DEFECT
MX7245	9133	24 PDIP	72	0	0	0	
MAX690	9138	8 PDIP	77	0	0	0	
MX7245	9138	24 PDIP	76	0	0	0	
DG211	9138	16 PDIP	77	0	0	1	MARG. LEAKAGE
MAX232	9140	16 WSO	75	0	0	0	
MAX730	9140	8 PDIP	77	0	1	0	PARAMETRIC
DG211	9141	16 PDIP	77	0	0	0	
DG411	9144	16 PDIP	77	0	1	1	2 MARG. LEAKAGE
DG413	9145	16 PDIP	77	0	0	0	
MAX690	9147	8 PDIP	100	0	0	0	
DG455	9149	16 PDIP	72	0	0	0	
OP07	9152	8 PDIP	77	0	0	0	
MAX232	9201	16 WSO	77	0	0	0	

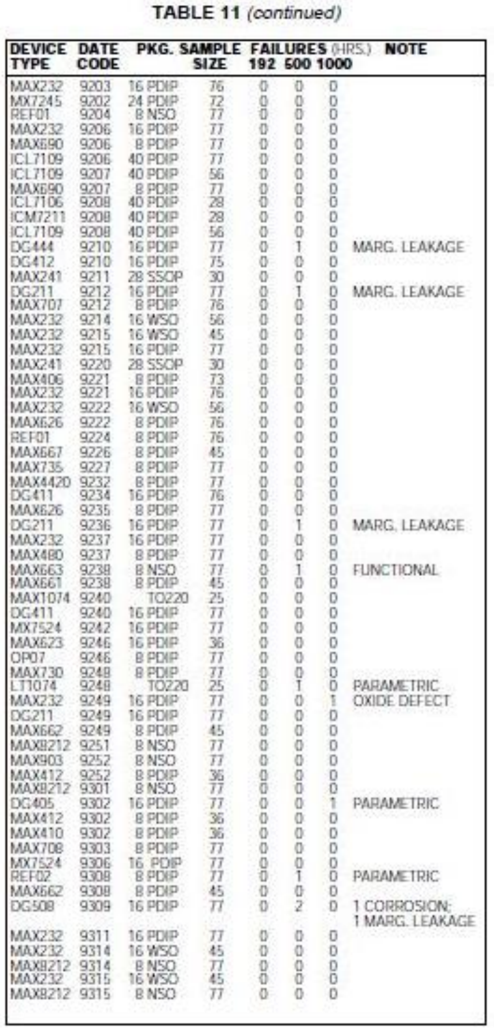


TABLE 11 *(continued)*

DEVICE TYPE	DATE CODE	PKG.	SAMPLE SIZE	FAILURES (HRS.)			NOTE
				192	500	1000	
MAX232	9203	16 PDIP	76	0	0	0	
MX7245	9202	24 PDIP	72	0	0	0	
REF01	9204	8 NSO	77	0	0	0	
MAX232	9206	16 PDIP	77	0	0	0	
MAX690	9206	8 PDIP	77	0	0	0	
ICL7109	9206	40 PDIP	77	0	0	0	
ICL7109	9207	40 PDIP	56	0	0	0	
MAX690	9207	8 PDIP	77	0	0	0	
ICL7106	9208	40 PDIP	28	0	0	0	
ICM7211	9208	40 PDIP	28	0	0	0	
ICL7109	9208	40 PDIP	56	0	0	0	
DG444	9210	16 PDIP	77	0	1	0	MARG. LEAKAGE
DG412	9210	16 PDIP	75	0	0	0	
MAX241	9211	28 SSOP	30	0	0	0	
DG211	9212	16 PDIP	77	0	1	0	MARG. LEAKAGE
MAX707	9212	8 PDIP	76	0	0	0	
MAX232	9214	16 WSO	56	0	0	0	
MAX232	9215	16 WSO	45	0	0	0	
MAX232	9215	16 PDIP	77	0	0	0	
MAX241	9220	28 SSOP	30	0	0	0	
MAX406	9221	8 PDIP	73	0	0	0	
MAX232	9221	16 PDIP	76	0	0	0	
MAX232	9222	16 WSO	56	0	0	0	
MAX626	9222	8 PDIP	76	0	0	0	
REF01	9224	8 PDIP	76	0	0	0	
MAX667	9226	8 PDIP	45	0	0	0	
MAX735	9227	8 PDIP	77	0	0	0	
MAX4420	9232	8 PDIP	77	0	0	0	
DG411	9234	16 PDIP	76	0	0	0	
MAX626	9235	8 PDIP	77	0	0	0	
DG211	9236	16 PDIP	77	0	1	0	MARG. LEAKAGE
MAX232	9237	16 PDIP	77	0	0	0	
MAX480	9237	8 PDIP	77	0	0	0	
MAX663	9238	8 NSO	77	0	1	0	FUNCTIONAL
MAX661	9238	8 PDIP	45	0	0	0	
MAX1074	9240	TO220	25	0	0	0	
DG411	9240	16 PDIP	77	0	0	0	
MX7524	9242	16 PDIP	77	0	0	0	
MAX623	9246	16 PDIP	36	0	0	0	
OP07	9246	8 PDIP	77	0	0	0	
MAX730	9248	8 PDIP	77	0	0	0	
LT1074	9248	TO220	25	0	1	0	PARAMETRIC
MAX232	9249	16 PDIP	77	0	0	1	OXIDE DEFECT
DG211	9249	16 PDIP	77	0	0	0	
MAX662	9249	8 PDIP	45	0	0	0	
MAX8212	9251	8 NSO	77	0	0	0	
MAX903	9252	8 NSO	77	0	0	0	
MAX412	9252	8 PDIP	36	0	0	0	
MAX8212	9301	8 NSO	77	0	0	0	
DG405	9302	16 PDIP	77	0	0	1	PARAMETRIC
MAX412	9302	8 PDIP	36	0	0	0	
MAX410	9302	8 PDIP	36	0	0	0	
MAX708	9303	8 PDIP	77	0	0	0	
MX7524	9306	16 PDIP	77	0	0	0	
REF02	9308	8 PDIP	77	0	1	0	PARAMETRIC
MAX662	9308	8 PDIP	45	0	0	0	
DG508	9309	16 PDIP	77	0	2	0	1 CORROSION; 1 MARG. LEAKAGE
MAX232	9311	16 PDIP	77	0	0	0	
MAX232	9314	16 WSO	45	0	0	0	
MAX8212	9314	8 NSO	77	0	0	0	
MAX232	9315	16 WSO	45	0	0	0	
MAX8212	9315	8 NSO	77	0	0	0	

Vapor Pressure and Relative Humidity

$$H = \frac{\text{Actual water vapor pressure at temperature } T}{\text{Saturated water vapor pressure at temperature } T}$$

or $$P_{\mathrm{H_2O}} = H \times P_{\mathrm{sat}}(T)$$

What is P_{sat}?

Important.

$$P_{\mathrm{sat}}(T) = P_0 \exp\left(-\frac{\lambda M}{RT}\right) = P_0 \exp\left(-\frac{Q_P}{kT}\right) \quad Q_P = \frac{k\lambda M}{R} = 0.42 \text{ eV}$$

Where

λ = 2262.6 joule/gm (latent heat of vaporization)

M = 18.015 gm/mole, R = 8.32 joules/(mole K), k = $8.617\text{x}10^{-5}$ eV/K

This is a fair approximation. The main benefit is physical insight.

Vapor Pressure and Relative Humidity

An accurate formula for $\mathrm{P_{sat}}$ (in Pascals) is

$$P_{sat}(T) = 1000 \times \exp\left(\sum_{n=0}^{3} a_n \times x^n\right), \quad x = \frac{1}{273 + T(^\circ \mathrm{C})}$$

$$a_0 = 16.033225, \quad a_1 = -3.5151386 \times 10^3,$$

$$a_2 = -2.9085058 \times 10^5, \quad a_3 = 5.0972361 \times 10^6$$

which is accurate to better than 0.15% in the range 5 C< T < 240 C.

1 atm = 101325 pascals

This is an accurate formula.

Vapor Pressure and Relative Humidity

- Relative humidity at "hot" die in steady state.
  - Partial pressure of water vapor is the same everywhere:

$$P_{\mathrm{H_2O}}(\mathrm{die}) = P_{\mathrm{H_2O}}(\mathrm{ambient})$$

  - So RH at die is given by:

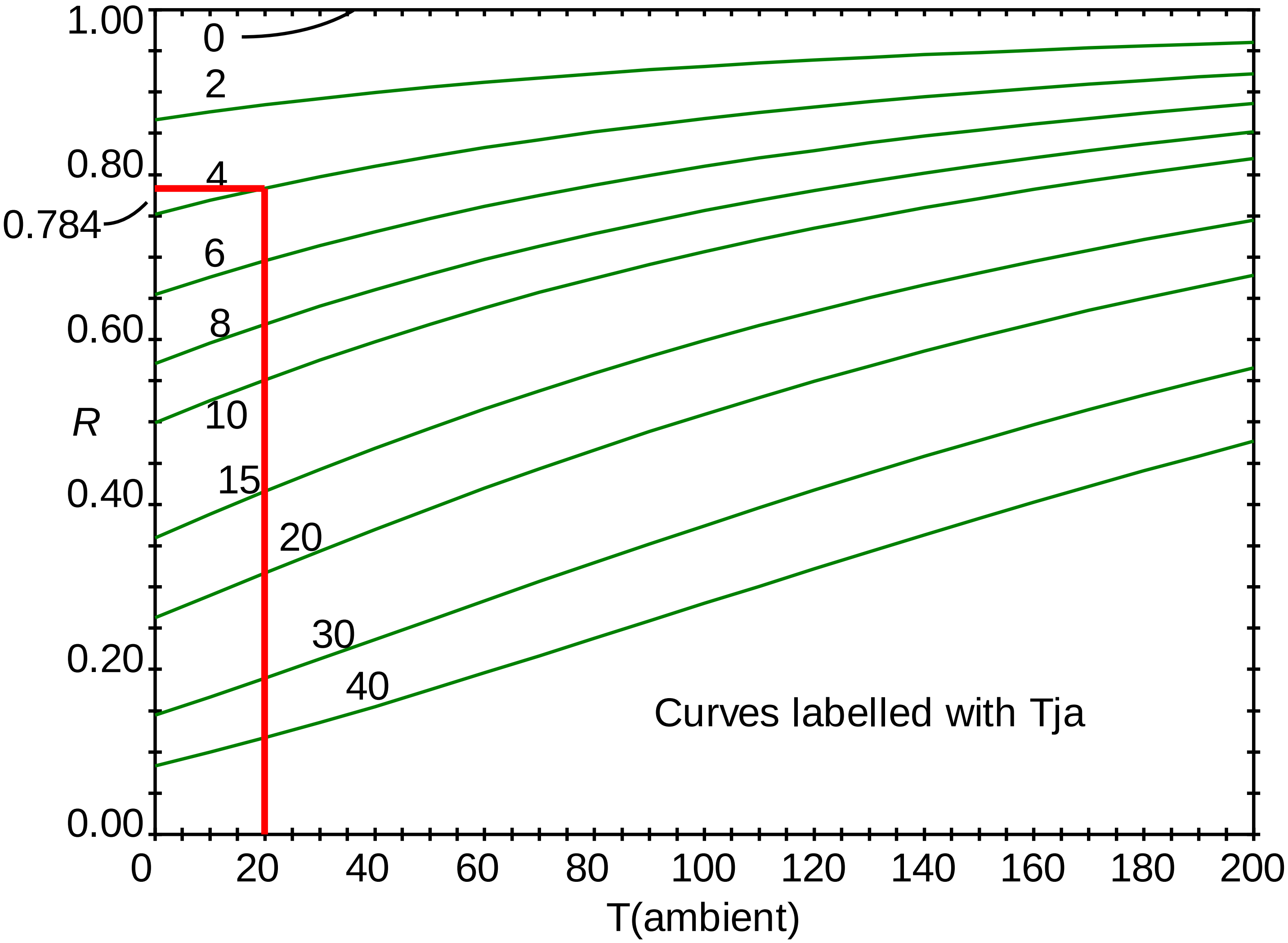
$$H(\mathrm{die}) \times P_{\mathrm{sat}}(T_{\mathrm{ambient}} + \Delta T_{\mathrm{ja}}) = H(\mathrm{ambient}) \times P_{\mathrm{sat}}(T_{\mathrm{ambient}})$$

  - Where the ratio, *h* is defined as:

$$H(\mathrm{die}) = h \times H(\mathrm{ambient})$$

$$h = \frac{P_{\mathrm{sat}}(T_{\mathrm{ambient}})}{P_{\mathrm{sat}}(T_{\mathrm{ambient}} + \Delta T_{\mathrm{ja}})}$$

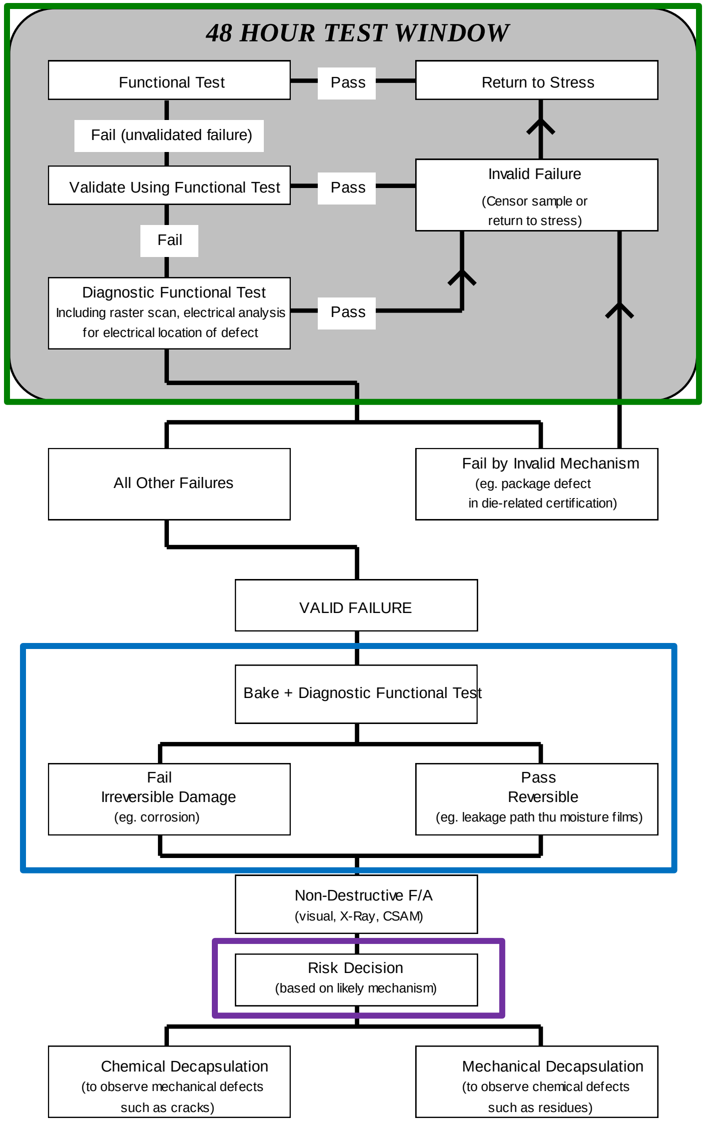
Vapor Pressure and Relative Humidity



Example: At 20/85 and Tja = 4 C, the die is at 24/(0.784x85) = 24/67.

Test and Failure Analysis

- Moisture-related tests (85/85, HAST, Steam) have specific test/FA reqt's.
  - Test must be done while unit contains moisture.
    - Within 48 hr.
  - Units must not be "wet".
    - Wet = liquid water.
- Diagnostic Bake.
- Risk decision before destructive analysis.

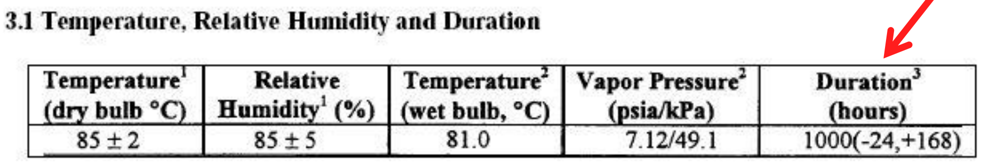


48 HOUR TEST WINDOW

Functional Test
Pass
Return to Stress
Fail (unvalidated failure)
Validate Using Functional Test
Pass
Invalid Failure
(Censor sample or return to stress)
Fail
Diagnostic Functional Test
Including raster scan, electrical analysis for electrical location of defect
Pass
All Other Failures
Fail by Invalid Mechanism
(eg. package defect in die-related certification)
VALID FAILURE
Bake + Diagnostic Functional Test
Fail
Irreversible Damage
(eg. corrosion)
Pass
Reversible
(eg. leakage path thu moisture films)
Non-Destructive F/A
(visual, X-Ray, CSAM)
Risk Decision
(based on likely mechanism)
Chemical Decapsulation
(to observe mechanical defects such as cracks)
Mechanical Decapsulation
(to observe chemical defects such as residues)

HAST versus 85/85

- Moisture MUST be non-condensing. (RH < 100%).
- Both require about < 1% fail. Typical SS ~ 100.
- 130/85 HAST duration is 10x less than 85/85 duration. We'll see how this was justified.
- 85/85 (**JESD22-A101**)

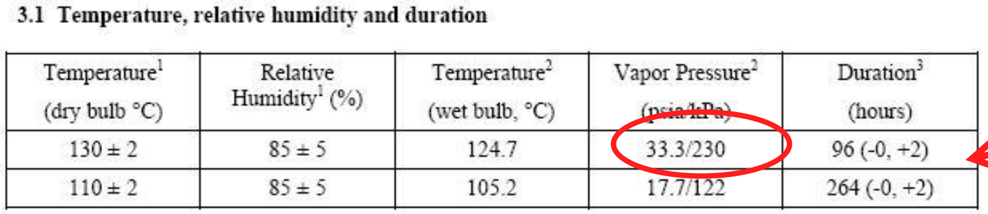


3.1 Temperature, Relative Humidity and Duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
85 ± 2	85 ± 5	81.0	7.12/49.1	1000(-24,+168)

6 week bottleneck in information turns.

- HAST (**JESD22-A110**)



3.1 Temperature, relative humidity and duration

Temperature[1] (dry bulb °C)	Relative Humidity[1] (%)	Temperature[2] (wet bulb, °C)	Vapor Pressure[2] (psia/kPa)	Duration[3] (hours)
130 ± 2	85 ± 5	124.7	33.3/230	96 (-0, +2)
110 ± 2	85 ± 5	105.2	17.7/122	264 (-0, +2)

10x less time

1 atm = 14.2 psi

$$\frac{33.3-14.2}{14.2}=1.34\text{ atmospheres}\Rightarrow\quad\text{Pressure vessel required.}$$

Example: Comparison of HAST Stds

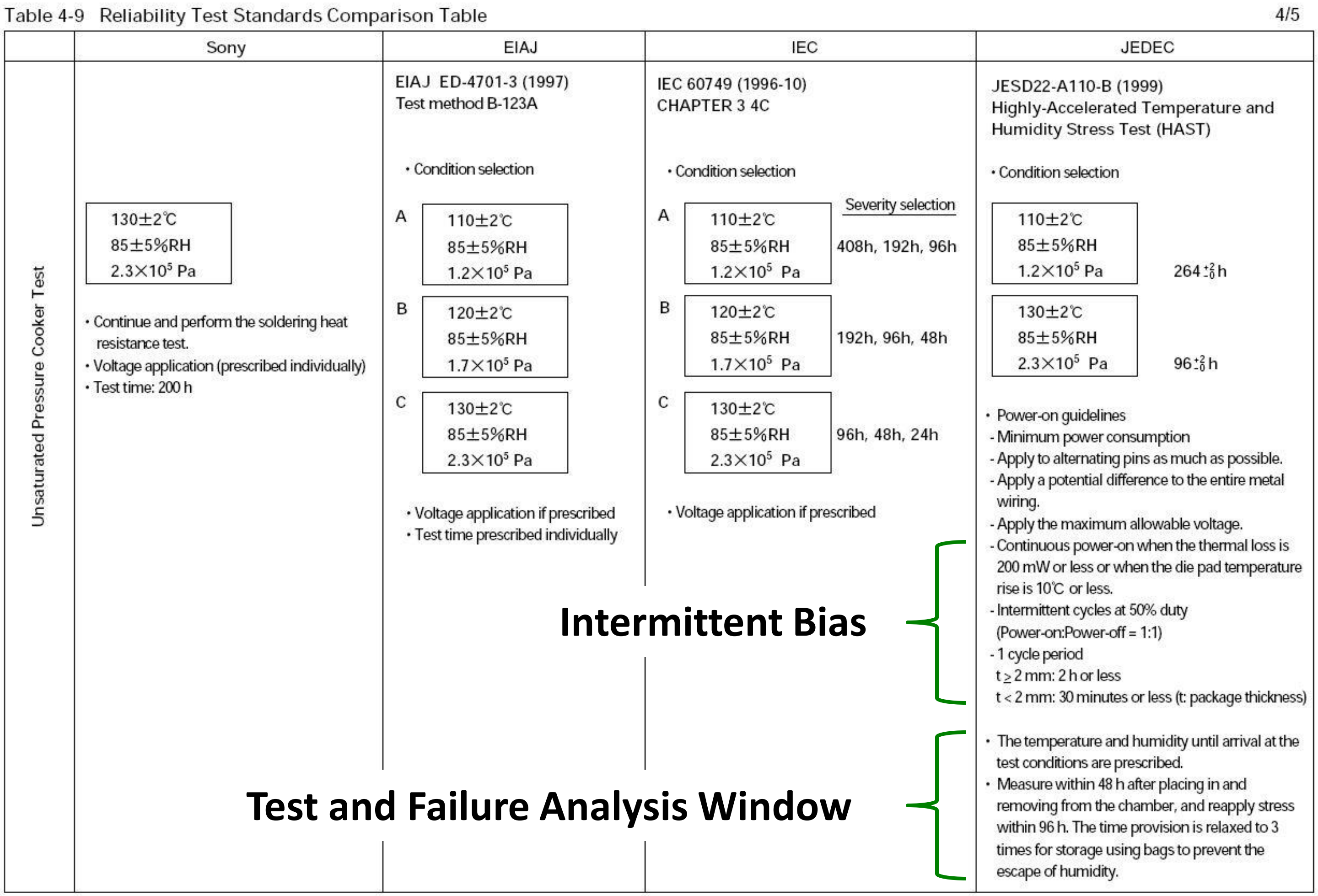


Table 4-9 Reliability Test Standards Comparison Table 4/5

	Sony	EIAJ	IEC	JEDEC
Unsaturated Pressure Cooker Test	130±2℃ 85±5%RH 2.3×10^5 Pa • Continue and perform the soldering heat resistance test. • Voltage application (prescribed individually) • Test time: 200 h	EIAJ ED-4701-3 (1997) Test method B-123A • Condition selection A: 110±2℃, 85±5%RH, 1.2×10^5 Pa B: 120±2℃, 85±5%RH, 1.7×10^5 Pa C: 130±2℃, 85±5%RH, 2.3×10^5 Pa • Voltage application if prescribed • Test time prescribed individually	IEC 60749 (1996-10) CHAPTER 3 4C • Condition selection (Severity selection) A: 110±2℃, 85±5%RH, 1.2×10^5 Pa — 408h, 192h, 96h B: 120±2℃, 85±5%RH, 1.7×10^5 Pa — 192h, 96h, 48h C: 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96h, 48h, 24h • Voltage application if prescribed	JESD22-A110-B (1999) Highly-Accelerated Temperature and Humidity Stress Test (HAST) • Condition selection 110±2℃, 85±5%RH, 1.2×10^5 Pa — 264^{+2}_{-0} h 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96^{+2}_{-0} h • Power-on guidelines - Minimum power consumption - Apply to alternating pins as much as possible. - Apply a potential difference to the entire metal wiring. - Apply the maximum allowable voltage. - Continuous power-on when the thermal loss is 200 mW or less or when the die pad temperature rise is 10℃ or less. - Intermittent cycles at 50% duty (Power-on:Power-off = 1:1) - 1 cycle period t ≥ 2 mm: 2 h or less t < 2 mm: 30 minutes or less (t: package thickness) • The temperature and humidity until arrival at the test conditions are prescribed. • Measure within 48 h after placing in and removing from the chamber, and reapply stress within 96 h. The time provision is relaxed to 3 times for storage using bags to prevent the escape of humidity.

Intermittent Bias

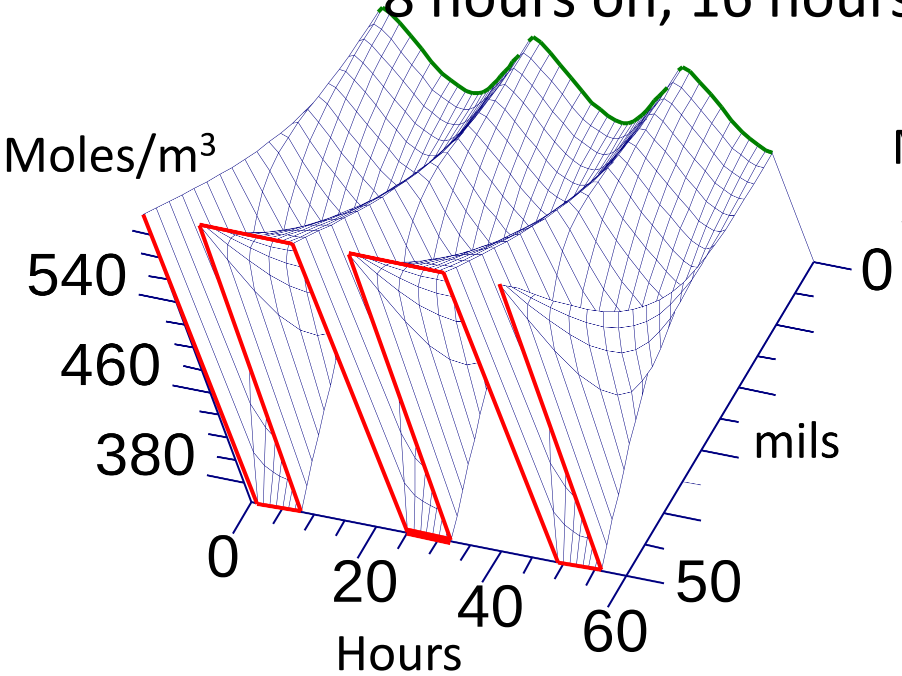
Test and Failure Analysis Window

From Sony Quality and Reliability Handbook http://www.sony.net/Products/SC-HP/tec/catalog/qr.html

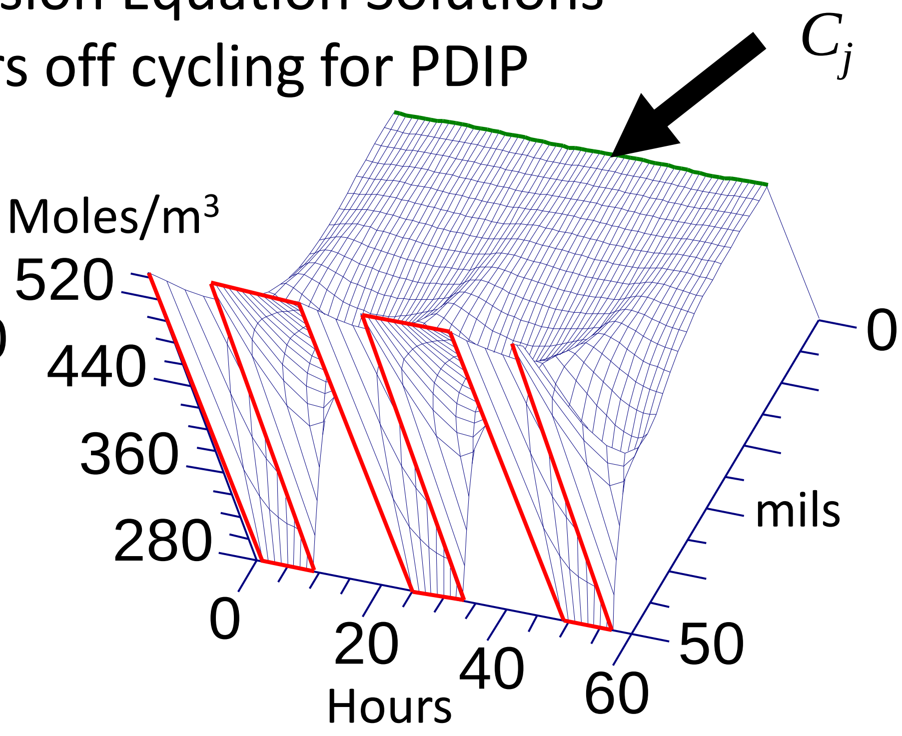
Cyclical Stress

One-Dimensional Diffusion Equation Solutions

8 hours on, 16 hours off cycling for PDIP



T(ambient) = 100 C
t(sat) = 28 hours



T(ambient) = 60 C
t(sat) = 153 hours

Moisture concentration at the die is constant if Period << t(sat)

Time-Varying Power Dissipation

- Most moisture-related mechanisms..
  - Have slow or zero rates at zero bias (V=0). $AF = V \times H_j^m \times \exp(-Q/kT_j)$
  - Have $Q/m < 0.42$ eV so, in steady-state, depressed die humidity due to power dissipation slows the rate.
- There is an optimum duty cycle which maximizes the effective acceleration.

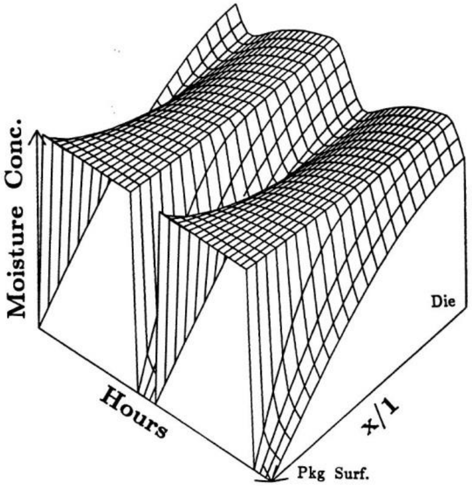
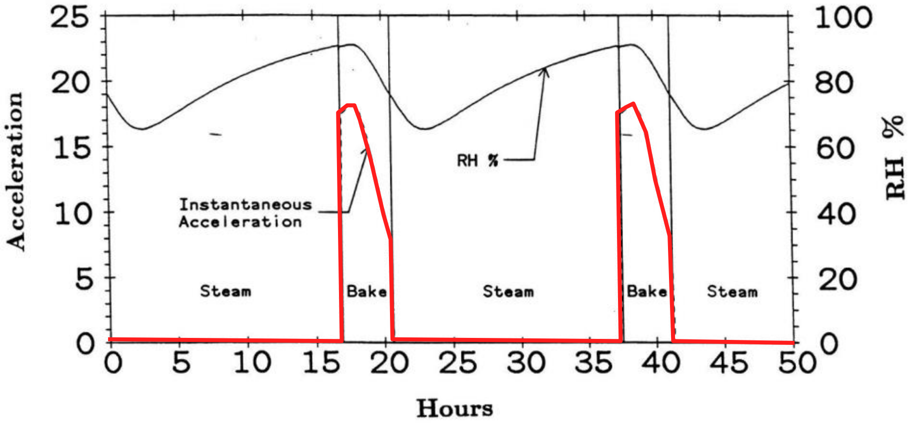
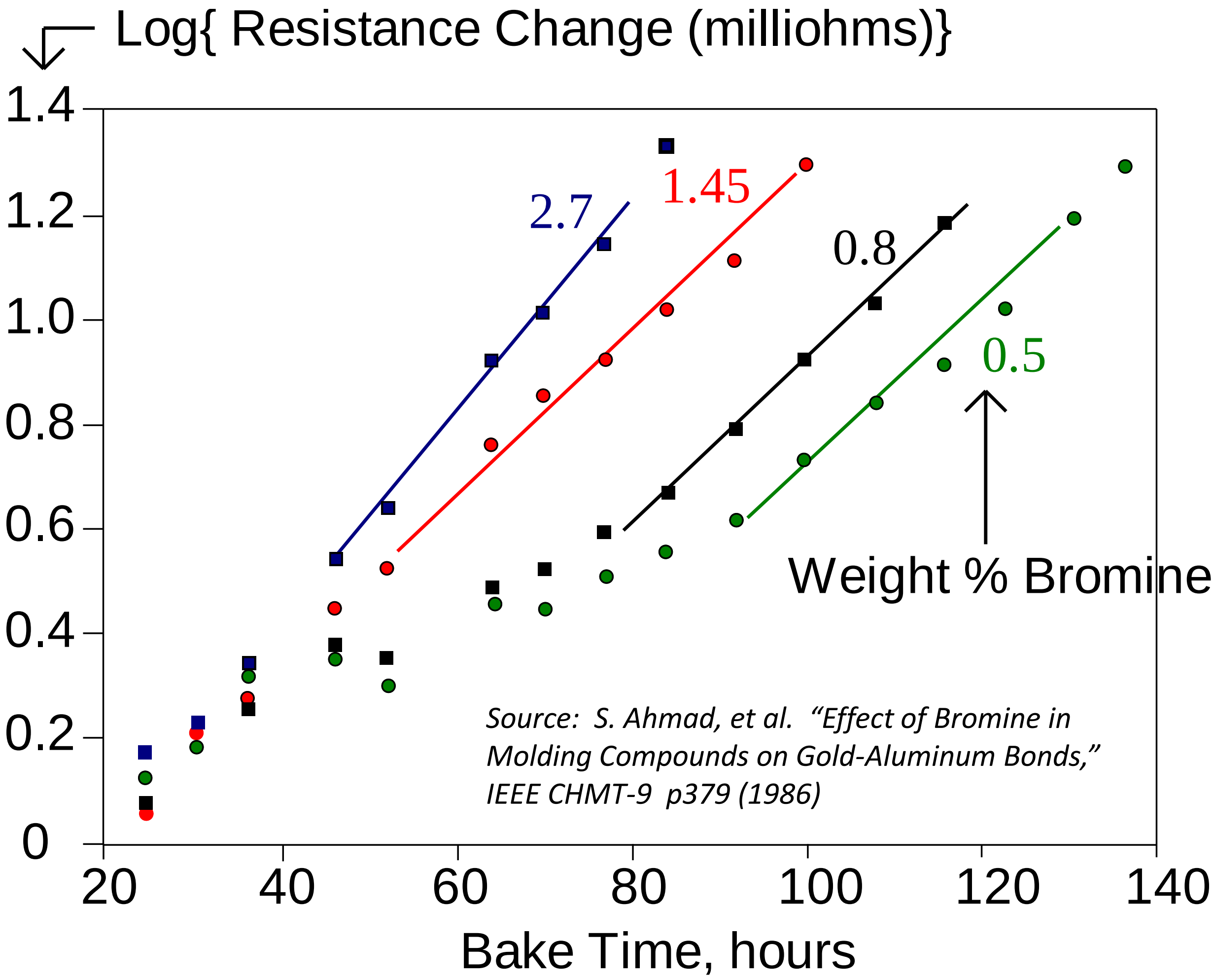


Fig. 2 Variation of the relative humidity at the die and instantaneous acceleration factor for the same stress cycle as shown in Fig. 1. During steam stress the instantaneous acceleration is zero because no bias is applied. The acceleration factor model in Eqs. (26), with Q = 0.79 eV, and b = 4.64 was used to evaluate the acceleration.



Gold-Aluminum Bond Failure

- Kelvin resistance measurements.
- Resistance increase of Au bonds to Al pads vs bake time.
- Bake at 200 °C.
- Various levels of Br flame-retardant in molding compound.
- Br catalyzes Au-Al intermetallic growth.
- Br flame retardants are being phased out today.



Source: S. Ahmad, et al. "Effect of Bromine in Molding Compounds on Gold-Aluminum Bonds," IEEE CHMT-9 p379 (1986)

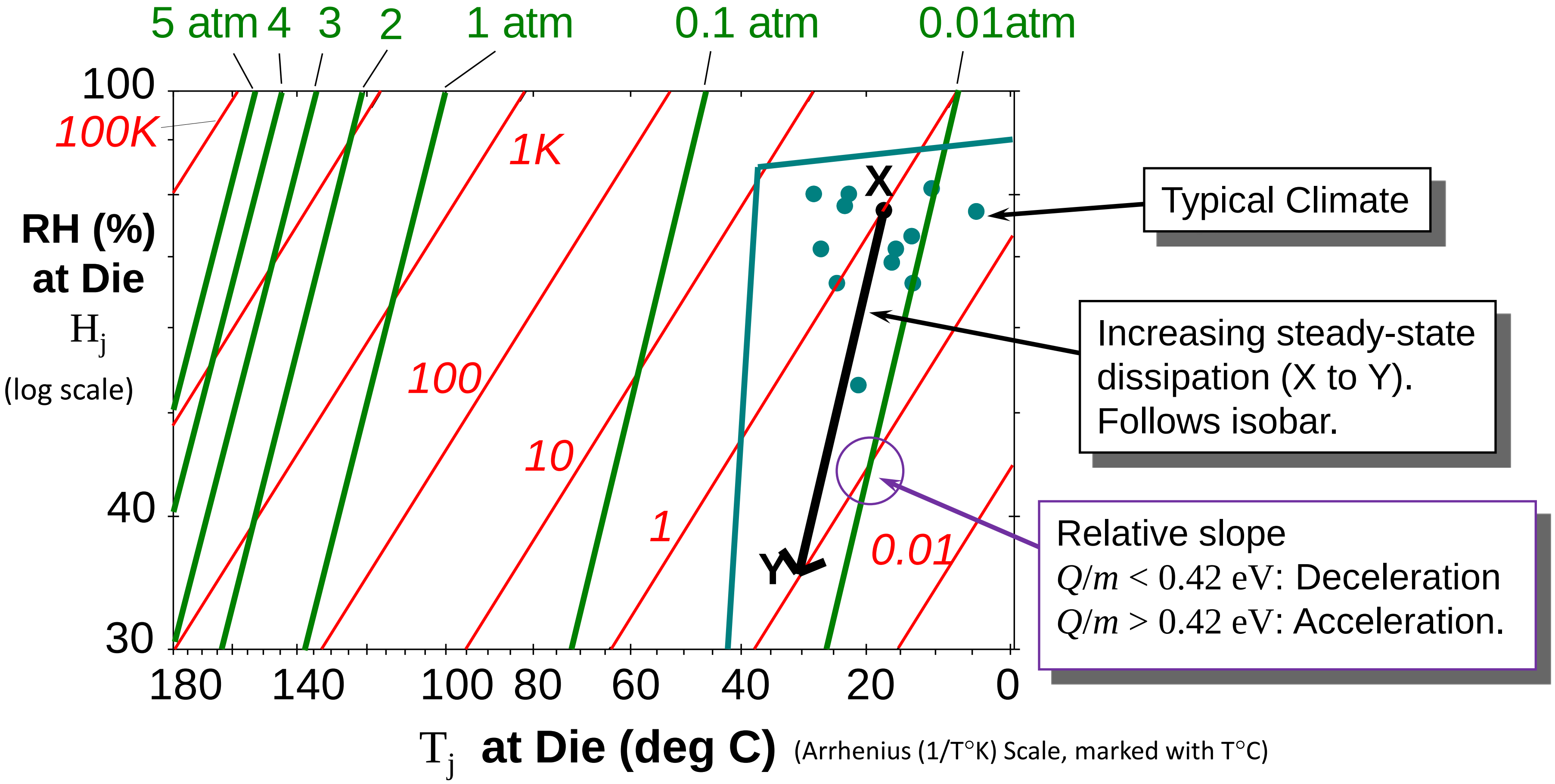
Steady Power Dissipation

- Superimpose log(H) vs 1/T contour plots of
  - Peck model for THB acceleration factor.
  - Partial pressure of water vapor, Psat.
- Contours are straight lines:
  - Peck model: Iso-acceleration contours with slope proportional to Q/m.
  - Psat: Isobars with slope proportional to $Q_p = 0.42$ eV.
- Assumption: In steady state, the partial pressure of H_2O is the same in the ambient and at the die.

Reference: C. G. Shirley, "THB Reliability Models and Life Prediction for Intermittently-Powered Non-Hermetic Components", IRPS 1994

Steady Power Dissipation

Iso-acceleration contours for example mechanism
($m = 4.6$, $Q = 0.8$ eV) superimposed on water vapor pressure isobars.



Typical Climate

Increasing steady-state dissipation (X to Y). Follows isobar.

Relative slope
$Q/m < 0.42$ eV: Deceleration
$Q/m > 0.42$ eV: Acceleration.

Example: Comparison of HAST Stds

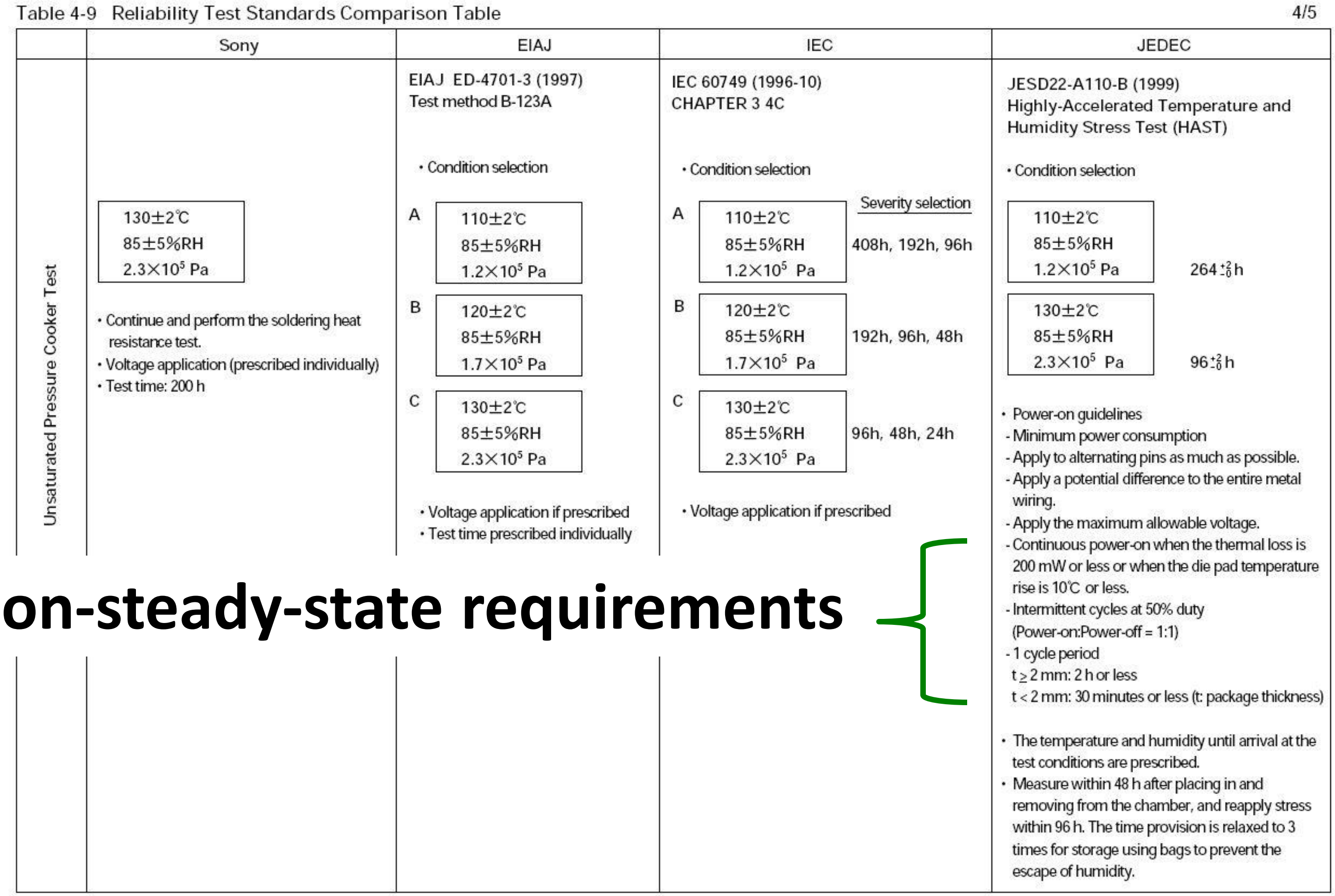


Table 4-9 Reliability Test Standards Comparison Table 4/5

	Sony	EIAJ	IEC	JEDEC
Unsaturated Pressure Cooker Test	130±2℃ 85±5%RH 2.3×10^5 Pa • Continue and perform the soldering heat resistance test. • Voltage application (prescribed individually) • Test time: 200 h	EIAJ ED-4701-3 (1997) Test method B-123A • Condition selection A 110±2℃ 85±5%RH 1.2×10^5 Pa B 120±2℃ 85±5%RH 1.7×10^5 Pa C 130±2℃ 85±5%RH 2.3×10^5 Pa • Voltage application if prescribed • Test time prescribed individually	IEC 60749 (1996-10) CHAPTER 3 4C • Condition selection Severity selection A 110±2℃ 85±5%RH 1.2×10^5 Pa — 408h, 192h, 96h B 120±2℃ 85±5%RH 1.7×10^5 Pa — 192h, 96h, 48h C 130±2℃ 85±5%RH 2.3×10^5 Pa — 96h, 48h, 24h • Voltage application if prescribed	JESD22-A110-B (1999) Highly-Accelerated Temperature and Humidity Stress Test (HAST) • Condition selection 110±2℃ 85±5%RH 1.2×10^5 Pa — 264^{+2}_{-0} h 130±2℃ 85±5%RH 2.3×10^5 Pa — 96^{+2}_{-0} h • Power-on guidelines - Minimum power consumption - Apply to alternating pins as much as possible. - Apply a potential difference to the entire metal wiring. - Apply the maximum allowable voltage. - Continuous power-on when the thermal loss is 200 mW or less or when the die pad temperature rise is 10℃ or less. - Intermittent cycles at 50% duty (Power-on:Power-off = 1:1) - 1 cycle period $t \geq 2$ mm: 2 h or less $t < 2$ mm: 30 minutes or less (t: package thickness) • The temperature and humidity until arrival at the test conditions are prescribed. • Measure within 48 h after placing in and removing from the chamber, and reapply stress within 96 h. The time provision is relaxed to 3 times for storage using bags to prevent the escape of humidity.

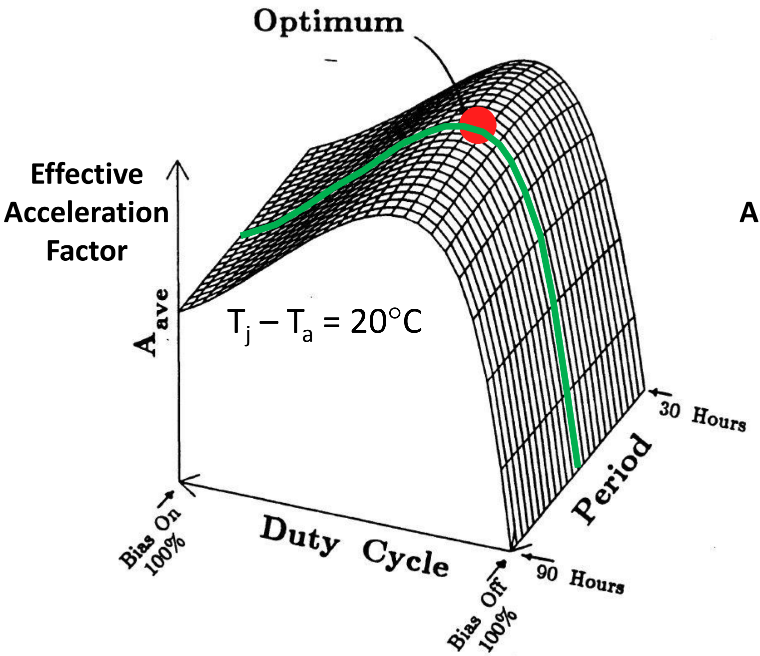
Non-steady-state requirements

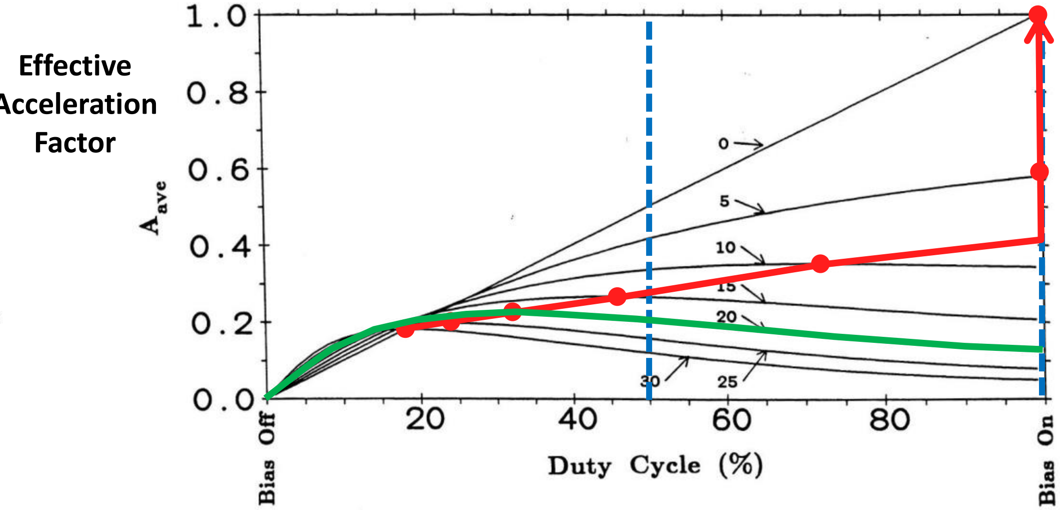
From Sony Quality and Reliability Handbook http://www.sony.net/Products/SC-HP/tec/catalog/qr.html

JEDEC 85/85 and HAST Req’ts

- T_j-T_a ≤10°C: 100% duty cycle.
- T_j-T_a > 10°C, 50% duty cycle.

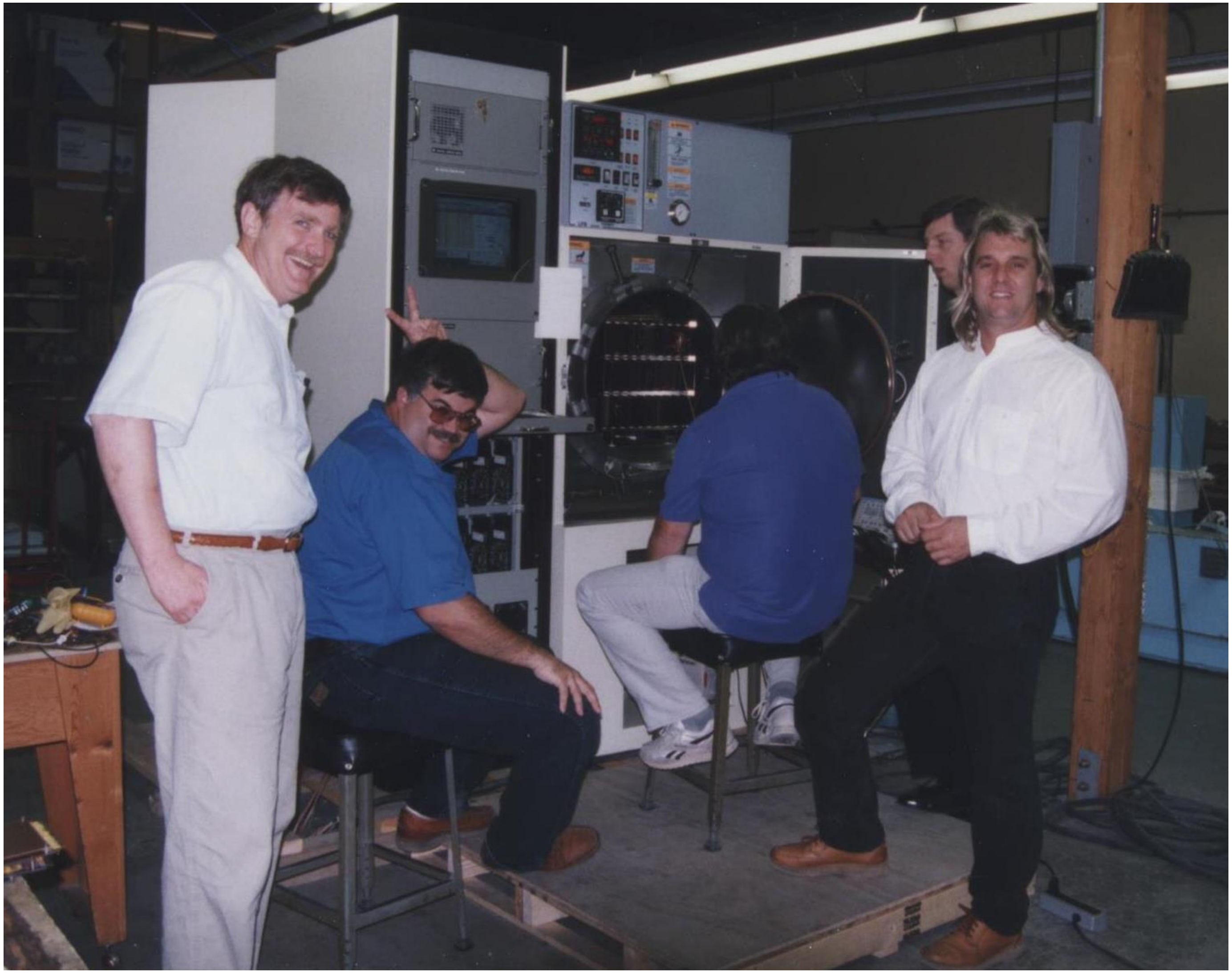
Assumptions:
- 85/85
- Peck Model *m* = 4.64, *Q* = 0.79 eV
- AF = 0 for V = 0.
- MC thickness 50 mils
- Kitano et. al MC properties.



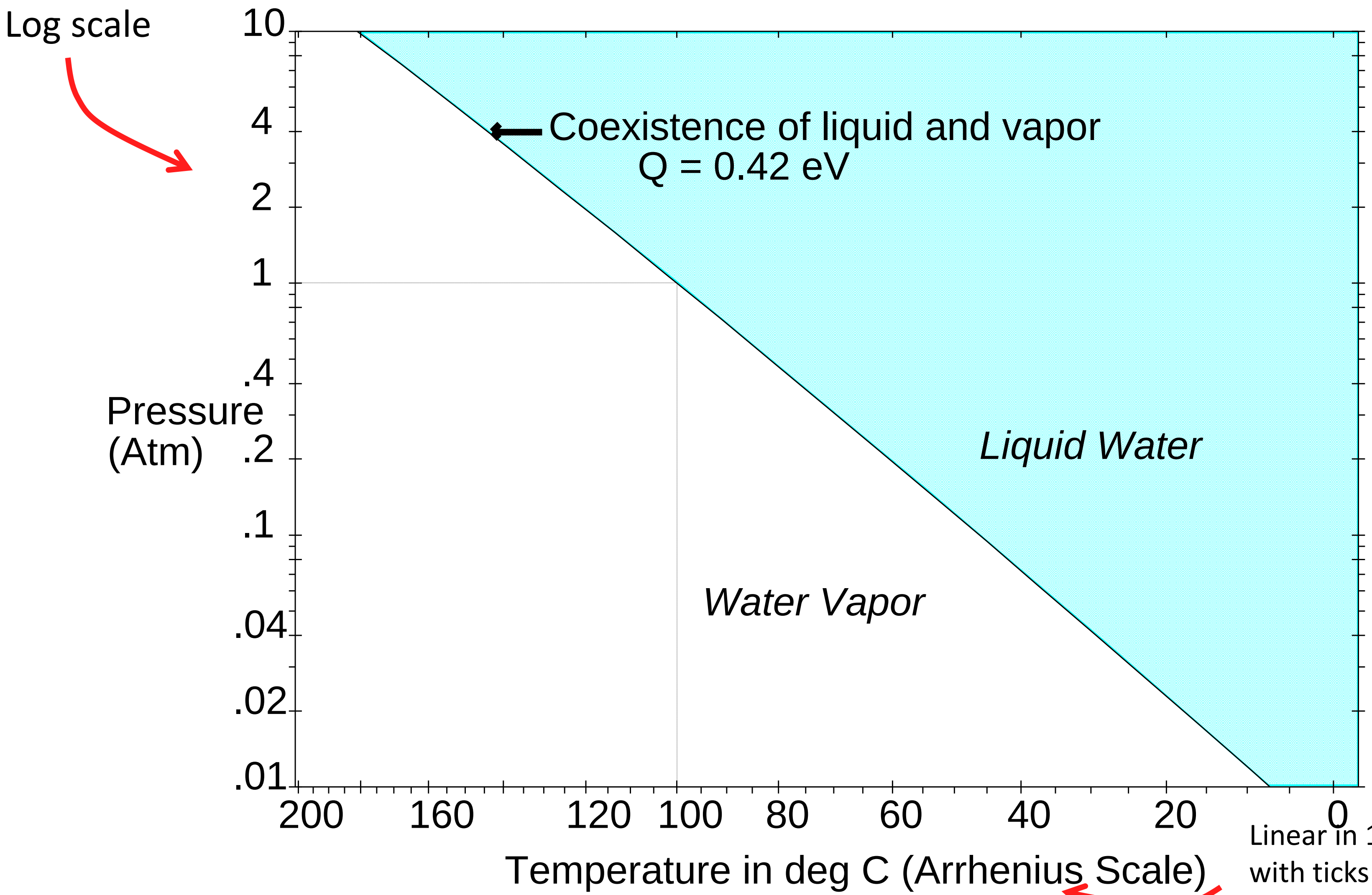


G. Shirley and C. Hong, "Optimal Acceleration of Cyclic THB Tests for Plastic-Packaged Devices," in Proc. 29th Ann. Int'l Reliability Physics Symposium, pp12-21 (1991)

HAST Development Team

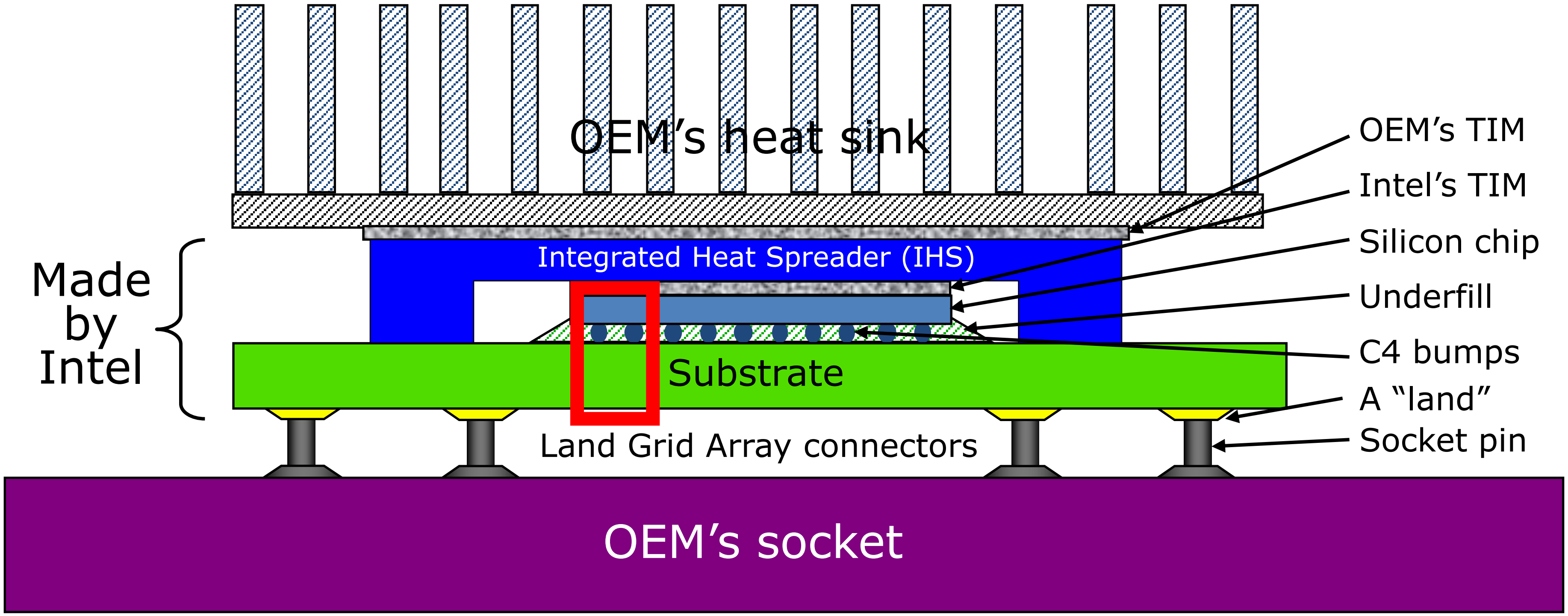


Vapor Pressure and Relative Humidity



Linear in 1/T (°K), with ticks placed at T (°C).

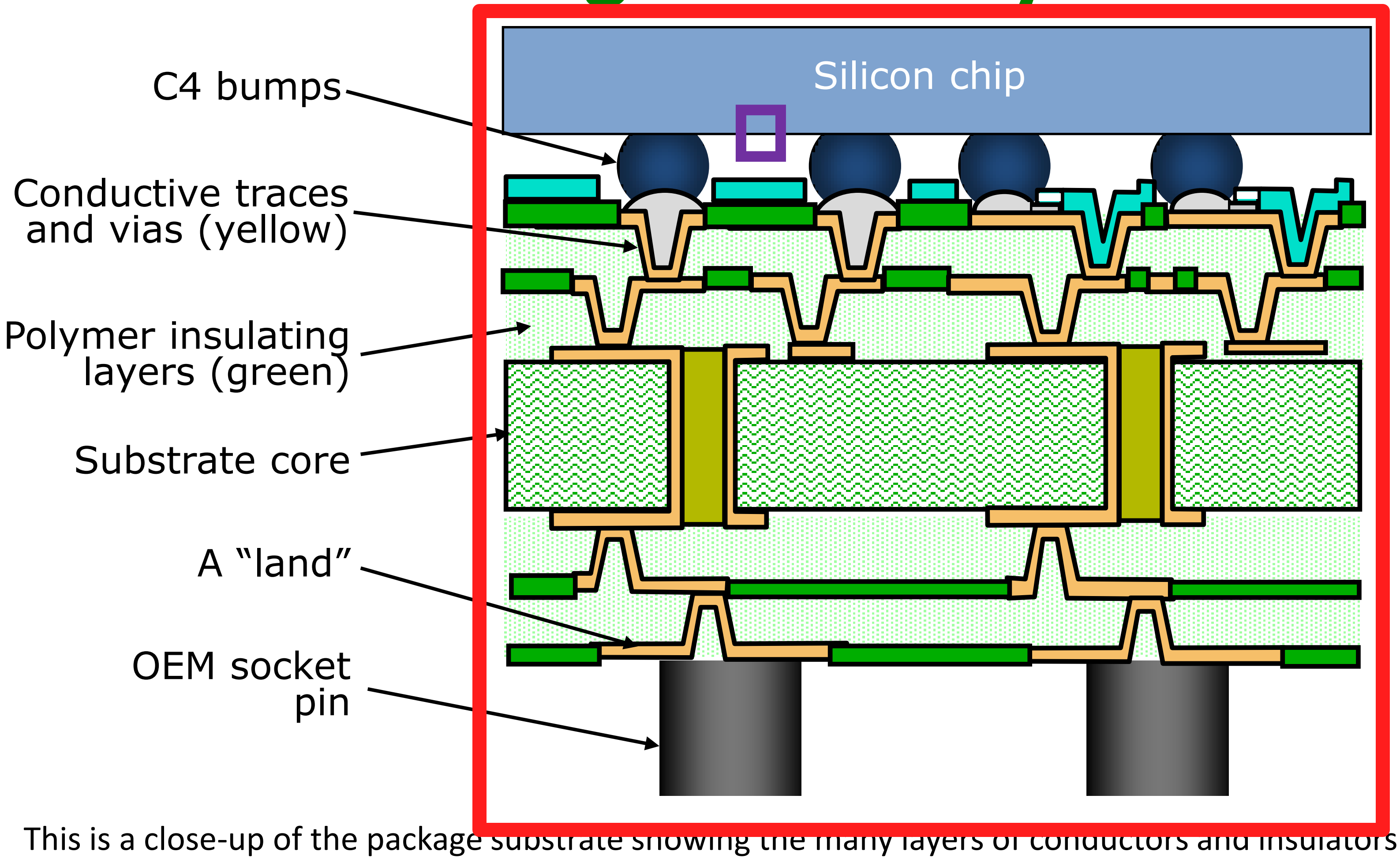
Package Anatomy



- This is an example of a packaged part as it might be used in a product

Slide: Scott C. Johnson

Package Anatomy



C4 bumps

Conductive traces and vias (yellow)

Polymer insulating layers (green)

Substrate core

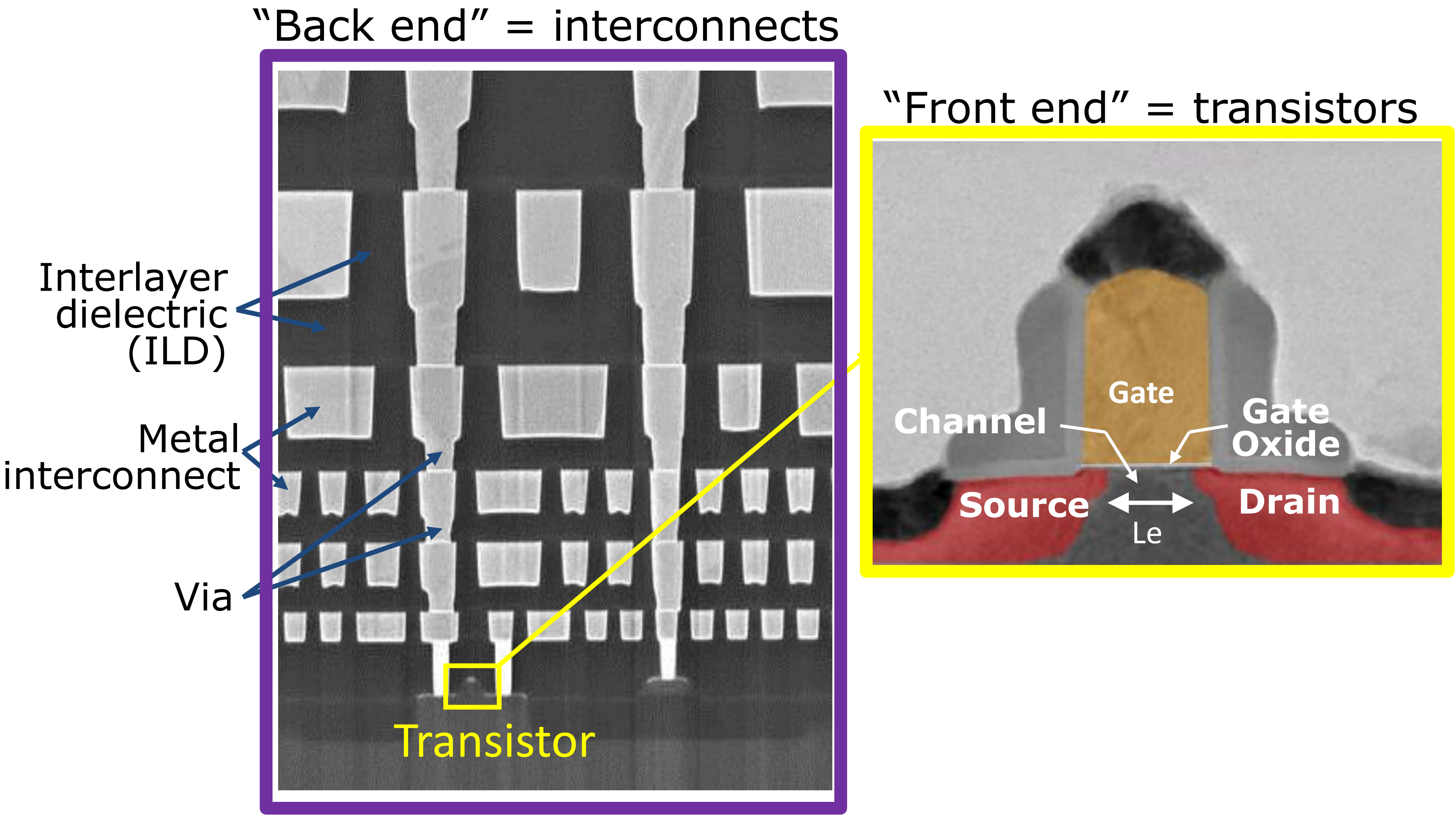
A “land”

OEM socket pin

- This is a close-up of the package substrate showing the many layers of conductors and insulators

Slide: Scott C. Johnson

Location: Silicon (vs. Package)

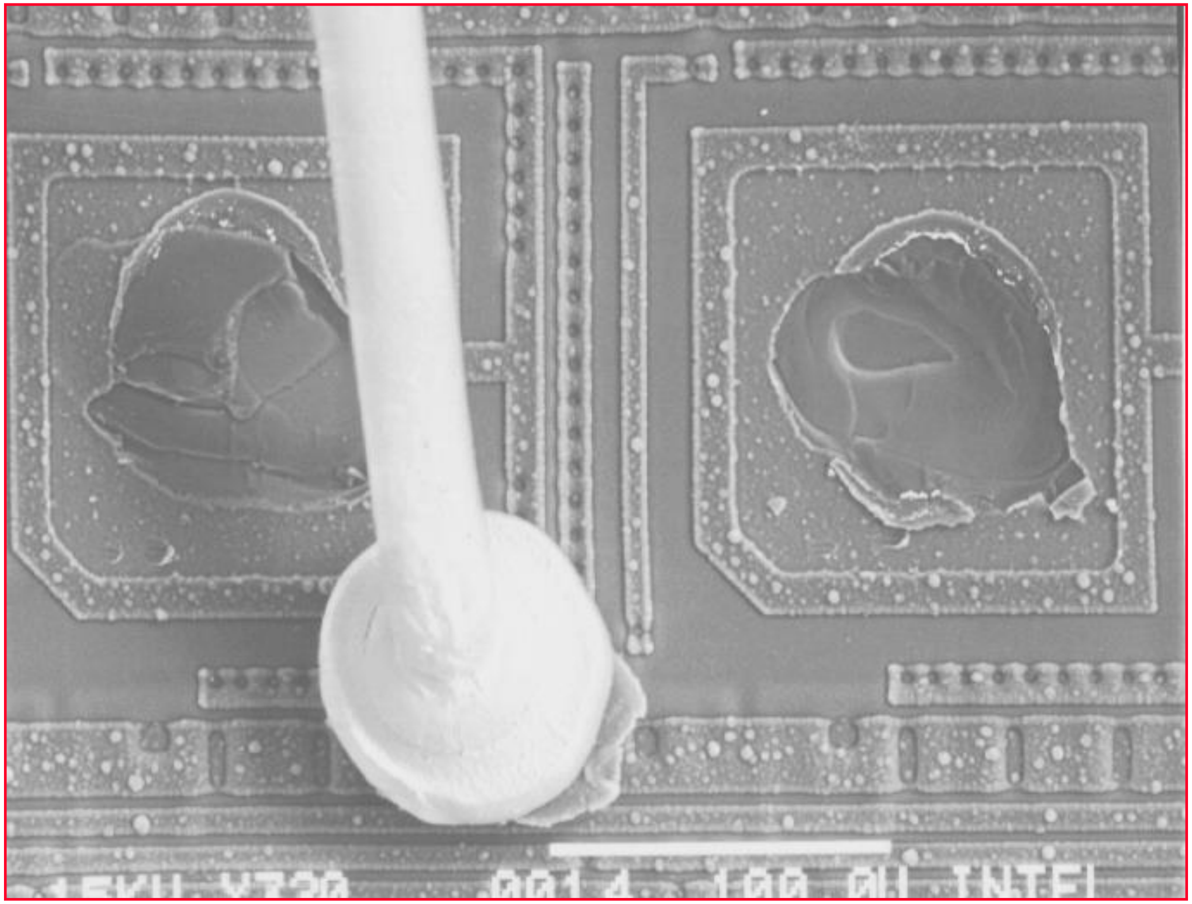


“Back end” = interconnects

“Front end” = transistors

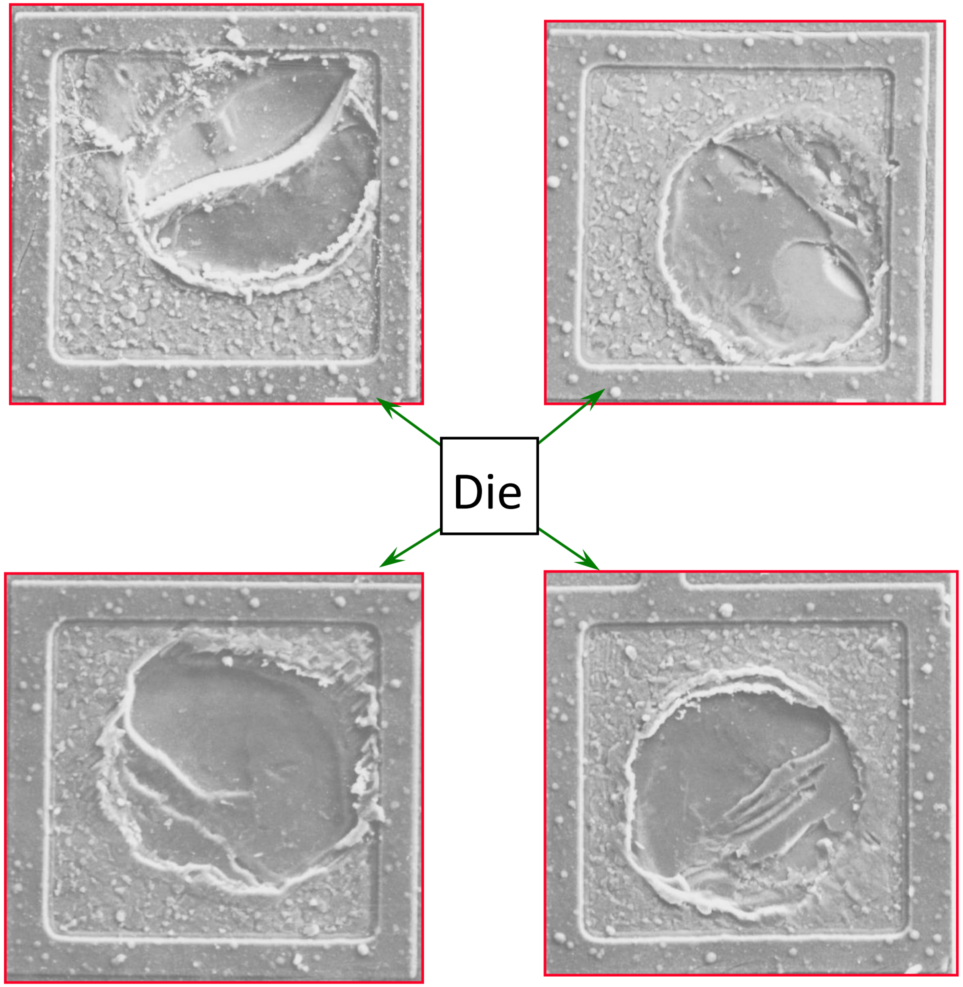
Slide: Scott C. Johnson

Bond Damage



Cratering damage on bond pads

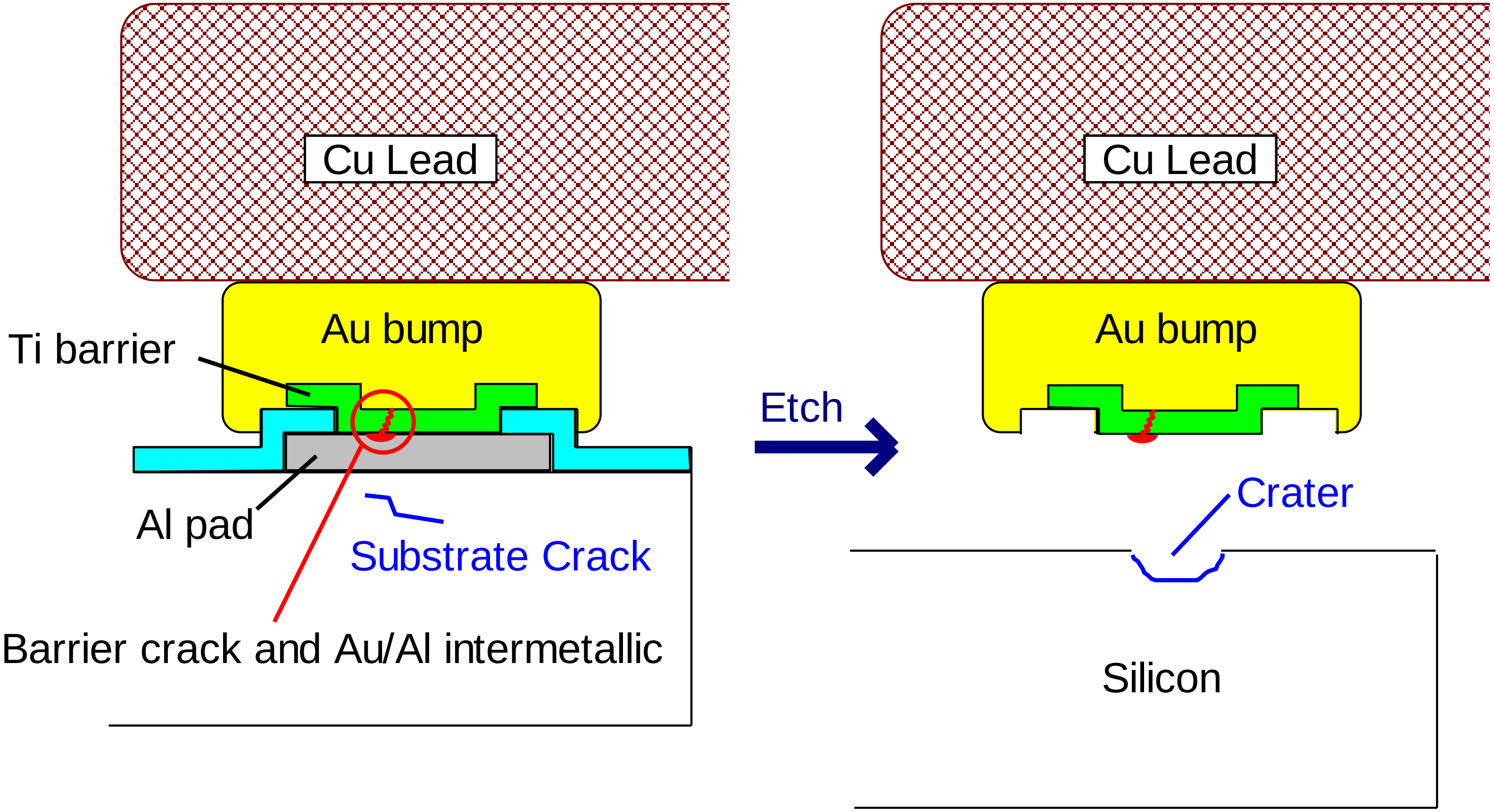
Bond Damage



Die

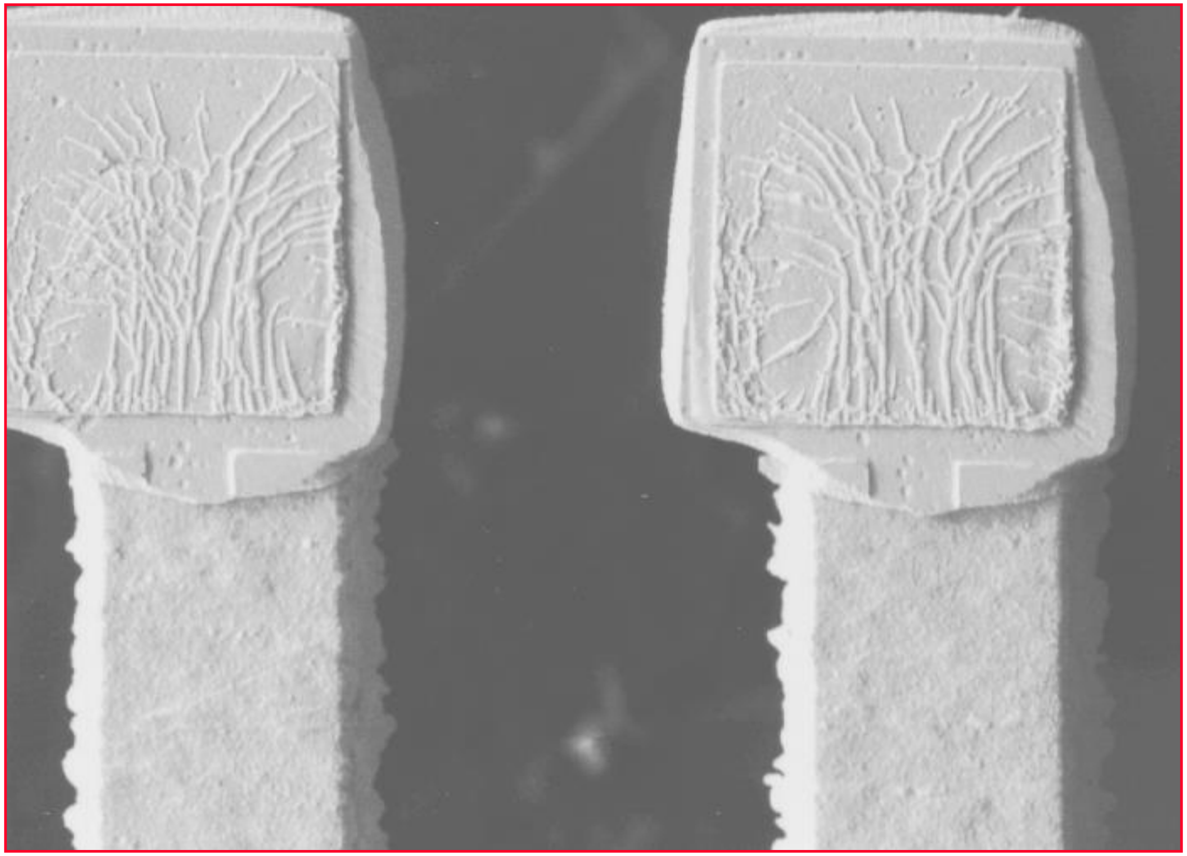
Bond shear at die corners after temperature cycle

Bond Damage (TAB)



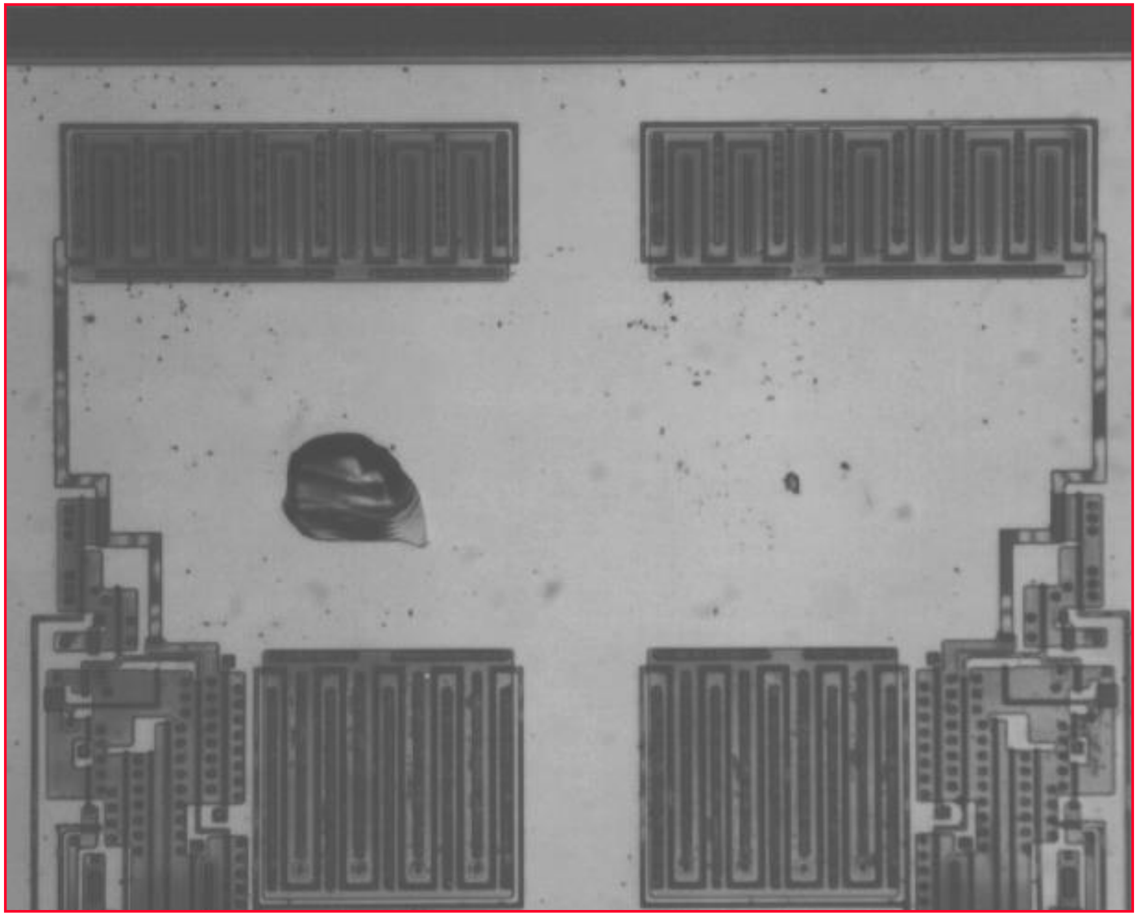
TAB cratering and diffusion barrier damage revealed by wet etch.

Bond Damage (TAB)



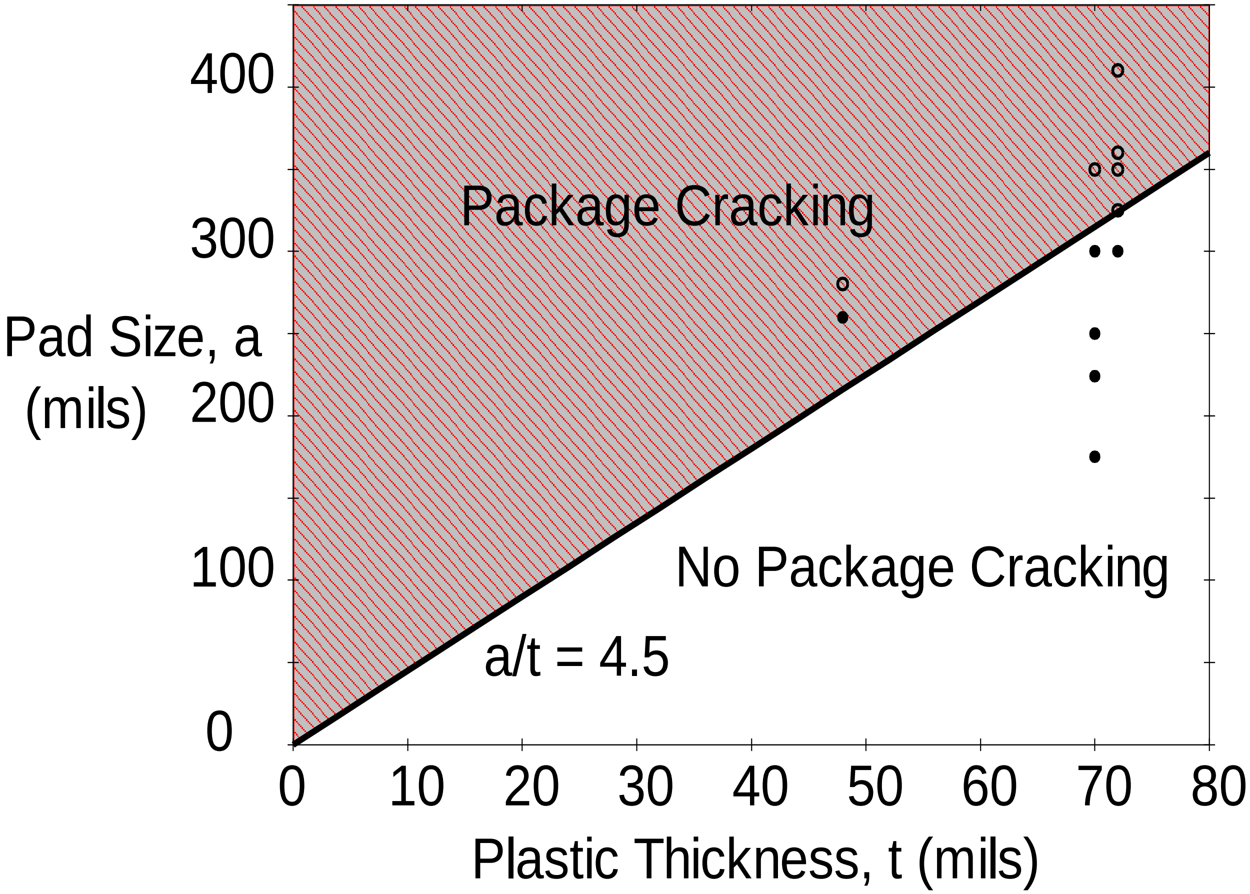
TAB bonds Au/Al intermetallic formed at cracks in Ti barrier

Bond Damage (TAB)



Crater under TAB bonds

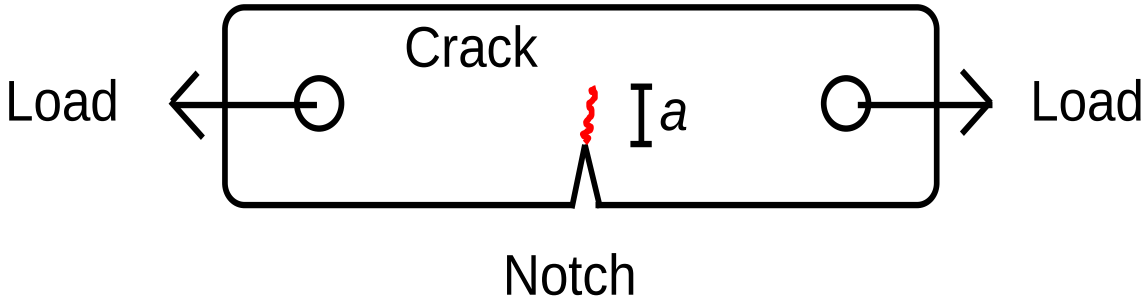
“Popcorn” Design Rules



Cracking sensitivity of PLCC packages after saturation in 85/85 followed by vapor-phase reflow soldering at 215 °C

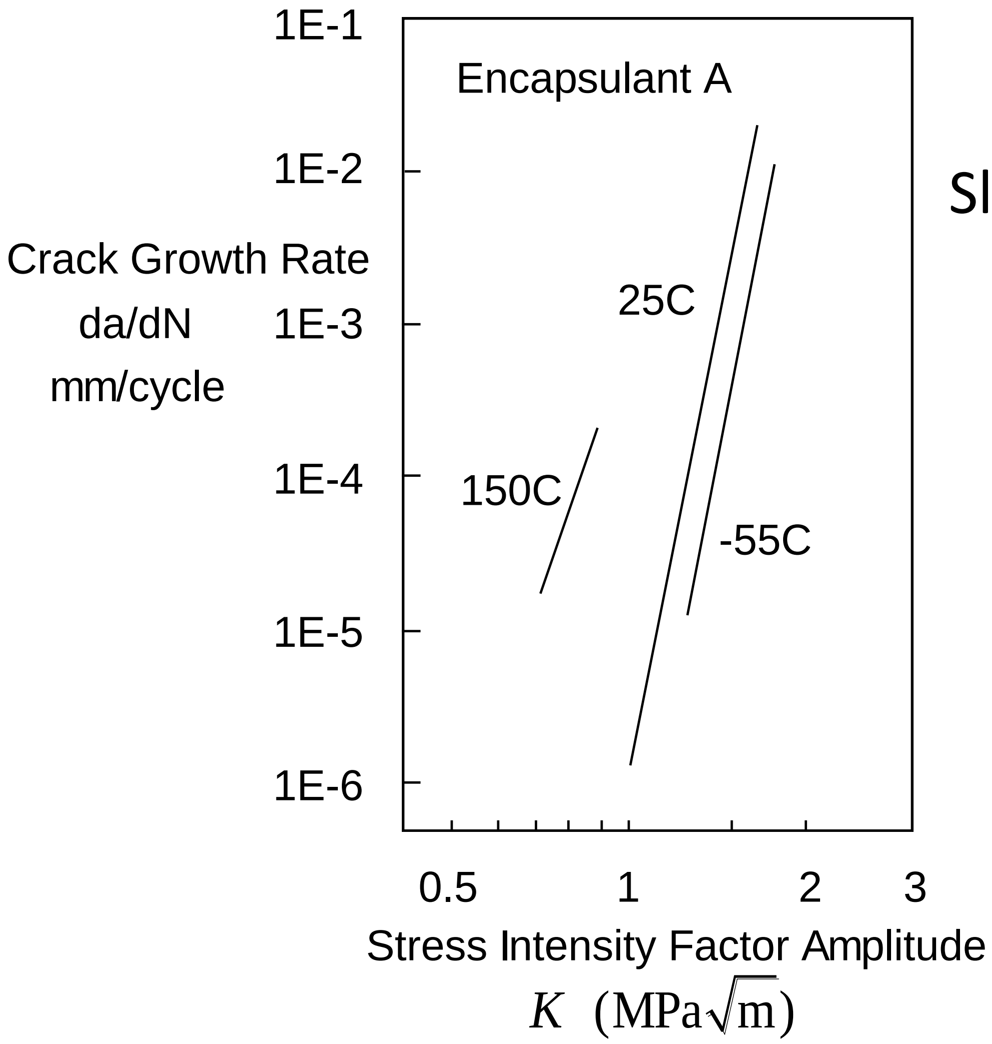
Crack Propagation in Test Conditions

- Tensile Test of Notched Samples
  - Measure crack growth rate for sinusoidal load:



  - Sample geometry and load determine stress intensity factor, *K*.
  - Plot crack growth rate da/dN versus *K* on log-log plot to determine Coffin-Manson exponent, *m*:

Crack Propagation in Test Conditions



Slope of lines on log-log plot

$$\frac{da}{dN} = Const \times (\Delta K)^m$$

$$m \approx 20$$

Source: A. Nishimura, et. al. “Life Estimation for IC Packages Under Temperature Cycling Based on Fracture Mechanics,” IEEE Trans. CHMT, Vol. 10, p637 (1987).