The next Step in Assembly and Packaging:

System Level Integration in the package (SiP)

Our intent is that this paper will be a living document that is kept up to date as System in Package progresses and the technology evolves. We would like to ask the readers to send any suggestions and/or corrections to bill_bottoms@3mts.com. This will assist us in keeping the document up to date and accurate so that it can be a continuing reference to the state of the art in SiP and a guide to developments critical to meeting future market requirements.

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1. Executive Summary

Predictions that Moore's Law has reached it limits have been heard for years and have proven to be premature. We are now nearing the basic physical limits to CMOS scaling and the continuation of the price elastic growth of the industry cannot continue based on Moore's law scaling alone. This will require "More than Moore" through the tighter integration of system level components at the package level. In the past scaling geometries enabled improved performance, less power, smaller size and lower cost. Today scaling alone does not ensure improvement of all four items.

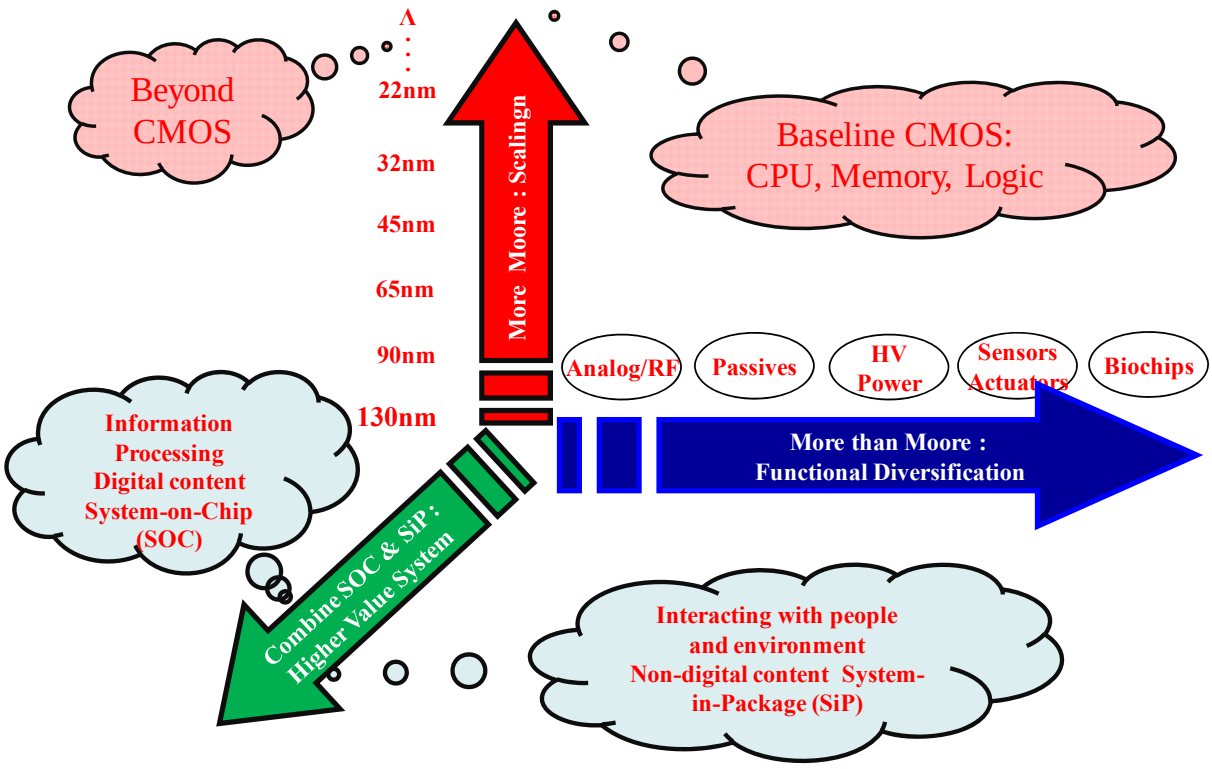


Figure 1: Beyond CMOS scaling

System on Chip (SoC) and System in Package (SiP) technologies provide a path for continued improvement in performance, power, cost and size at the system level without relying upon conventional CMOS scaling alone.

System in Package (SiP) technology is rapidly evolved from specialty technology used in a narrow set of applications to a high volume technology with wide ranging impact on electronics markets. The broadest adoption of SiP to date has been for stacked memory/logic devices and small modules (used to integrate mixed signal devices and passives) for mobile phone applications. Both these applications are driving high volume and a very cost competitive market with a broad base of suppliers has developed. Numerous concepts for three dimensional (3D) SiP packaging are now emerging driven largely by the demands of portable consumer products.

SiP has evolved as an alternative approach to System on Chip (SoC) for electronics integration because this technology provides advantages over SoC in many market segments. In particular SiP provides more integration flexibility, faster time to market, lower R&D cost, lower NRE cost, and lower product cost than SoC for many applications. SiP is not a replacement for high level, single chip, silicon integration but should be viewed as complementary to SoC. For some very high volume applications SoC will be the preferred approach. Some complex SiP products will contain SoC components.

As with most emerging markets, there remain a number of critical infrastructure issues to be resolved to improve time to market, cost structure, reliability, and performance. These include the need for low cost, higher density substrates, high speed co-design and simulation tools for electrical and mechanical design and analysis, wafer level packaging, lower cost assembly equipment, and improved materials.

This white paper addresses the requirements, challenges and potential solutions required for continued improvement in cost and performance of electronics through systems level integration at the packaging level. The objectives are to:

- disseminate information on the current state of the art,
- foster formation of a consensus on the “best” SiP solutions
- identify the areas where research is needed
- encourage focus and industry wide cooperation to minimize technology development risks

Background

The market demand for increased performance, smaller size, lower power and lower cost cannot be met with conventional packaging and interconnect technologies. There are limitations in interconnect density, thermal management, bandwidth and signal integrity that cannot be addressed with conventional technology. System in Package technology is perhaps the most important technology to address these limitations

The overall performance, cost, size, and functionally of a SiP will be limited by both on-chip interconnects of the individual microchips as well as by off-chip interconnects. Today, microprocessor performance, cost, fabrication

complexity, power dissipation, and size are driven by on-chip interconnects. At the off-chip level, lack of high input/output bandwidth and inability to deliver hundreds of amperes of supply current has limited performance below the "intrinsic limits" of each generation of technology.

Inferior thermal dissipation imposes the most serious bottleneck for the realization of ultimate performance SiP. Not only does the thermal dissipation technology dictate the chip junction temperature and subsequently its performance, but the size and cost of the thermal technology will limit the packing density, size, cost, and performance of SiP. Thermal dissipation is also the key limiter to 3D stacking of microprocessors and other high power density integrated circuits.

Even though IO bandwidth is often better than for single chip packages, inadequate chip input/output (I/O) bandwidth is the second most serious challenge to the realization of ultimate performance. Low-density electrical signal I/Os limit the aggregate off-chip bandwidth while losses due to the organic substrate, cross-talk, and impedance mismatches are exacerbated as off-chip bandwidth per channel increases and signal noise budget decreases. The impact of inadequate number of power and ground I/Os on the on-chip IR drop on the power distribution network, on-chip simultaneous switching noise, and signaling integrity will increase with each technology generation unless scaled accordingly. Moreover, the inductance of chip I/O interconnects and the on-chip power distribution network will require large decoupling capacitors on the silicon and the SiP substrate. Perhaps the greatest issue is the inability of the small transistor to drive the off-chip impedance at high speed. SiP technologies can address these limitations but much development work remains to be done.

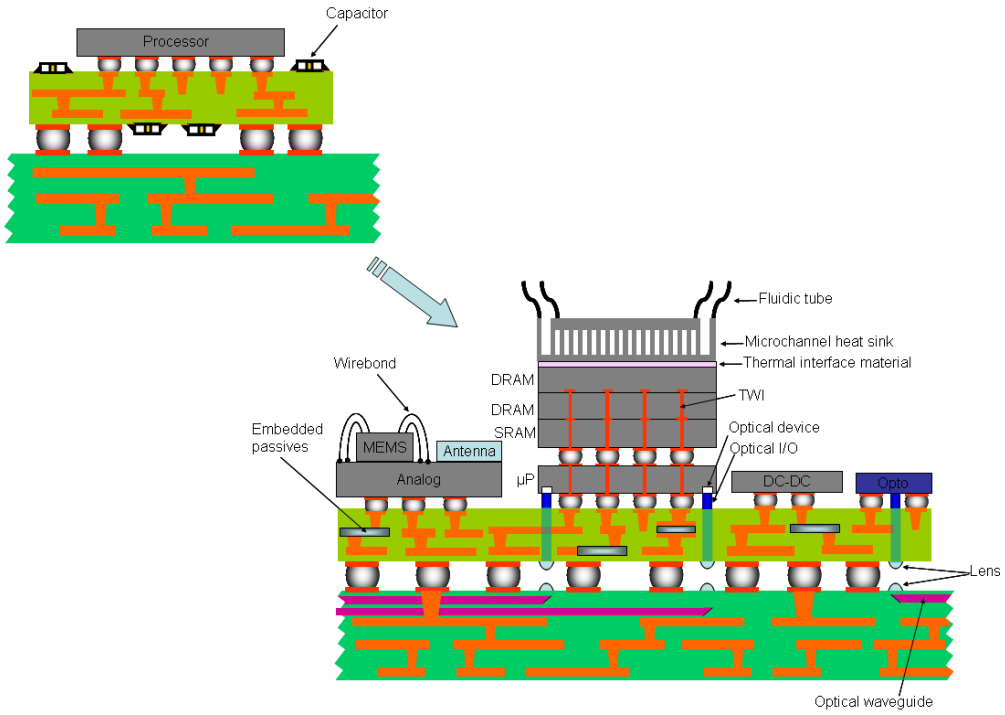


Figure 2: Evolutionary and revolutionary interconnect technologies are needed to enable migration of Microsystems from conventional state-of-art to 3D SiP.

Reliability, quality and manufacturing yield are key prerequisites for the development of complex innovative micro-/nanosystems. The challenges associated with meeting these prerequisites will require investment in the reliability research, diagnostics and failure analysis in addition to the development of new structures and processes.

Market demands will result in ever more components (e.g. passives, MEMS or optical components) being integrated into a single package. A long term vision for SiP is the optimized heterogeneous integration of wireless, optical, fluidic and bio elements/interfaces as well as integrated shielding and heat sinks. This goal requires the new materials and control of their interactions on the micro-/nanometer scale.

The microelectronic industry has to consider rapidly increasing reliability demands, e.g. for automotive, communication, or medical electronics applications as system complexity increases. These needs are another strong driving force for improved reliability concepts and failure analysis tools. Reliability models are needed to identify reliability problems during the product development phase ("design for reliability"). Such concepts gain increasing importance since they allow reduced time-to-market and reduced development cost for more complex systems.

Definition of SiP

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit that provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components and other packages and devices.

Level Structures

A definition of level structures for electronic systems is an important aid to description of existing systems, communication between user and supplier and identification of areas where development is required. The JISSO International Council has defined level structures for electronic systems. The term *JISSO* reflects the total packaging solution for electronic products. It includes interface and solution technology for Interconnecting, assembling, packaging, mounting and integrating system design. The functional building blocks or levels have two physical states. One represents the mechanical or physical description of the product such as size, weight, or shape; the other represents the interface of the product to its next level or to other products of the same level.

JISSO Level Concept

JISSO Level 0 – Intellectual Information

The intellectual information and/or proprietary information of an item pertaining the idea or intelligence imported or described in a formal document (protocol, standard, specification and/or patent disclosure) or design entity.

- The information may be in hard or soft copy and can include computer code or data format as a part of the description.
- The characteristics of the intellectual properties of an item are described as to their physical, chemical, thermal, electrical, mechanical, optical and/or environmental properties.

JISSO Level 1 – Electronic Element

A bare die/wafer or discrete component (resistor, capacitor, inductor, transistor, diode, fuse, etc.) with metalized terminals or termination ready for mounting.

- The element can be an IC, or discrete electrical, optical or MEMS element.
- Individual elements cannot be further reduced without destroying their stated function.

JISSO Product Level 2 – Electronic Package

An Individual Electronic Element or Elements in a container which protects the contents to assure the reliability and provides terminals to interconnect the container to an outer circuit.

- Package outline is generally standardized or meets guideline documents.
- A Package may function as electronic, optoelectronic, or MEMS, and may in the future include Bio-electronic elements including sensors.

JISSO Product Level 3 – Electronic Module

A functional block which contains Individual Electronic Elements and /or Electronic Packages, to be used in a next level assembly.

- An individual module having an application specific function, including Electronic, Optoelectronic, Mechanical or other elements.
- The module typically provides protection of its elements and packages to assure the required level of reliability.

JISSO Product Level 4 – Electronic Unit

A group of functional blocks that are designed to provide single or complex functions required by a system to implement the specified function.

- The Electronic unit may consist of Electronic Elements, Electronic Packages and/or Electronic Modules.
- The function of the Electronic unit may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof.
- The function may in the future include bio-electronic and chemical applications.

JISSO Level 5 – Electronic System

A completed, market ready and dedicated product combining and interconnecting functional block(s) to perform a designated function.

- The functional block(s) mainly consist of Electrotechnical Assemblies and may also include Electronic Units, Electronic Modules, Electronic Packages and/or Electronic Elements.
- The System Product may include cabinetry or a backplane into which mounted are assemblies, modules, packages or inserted elements, and the wiring (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system.

SiP may be classified as JISSO Product Level 2, 3 or 4 since it may include the functions of a complete system. Products in JISSO Product Level 2 can provide the complete function of an electronic system.

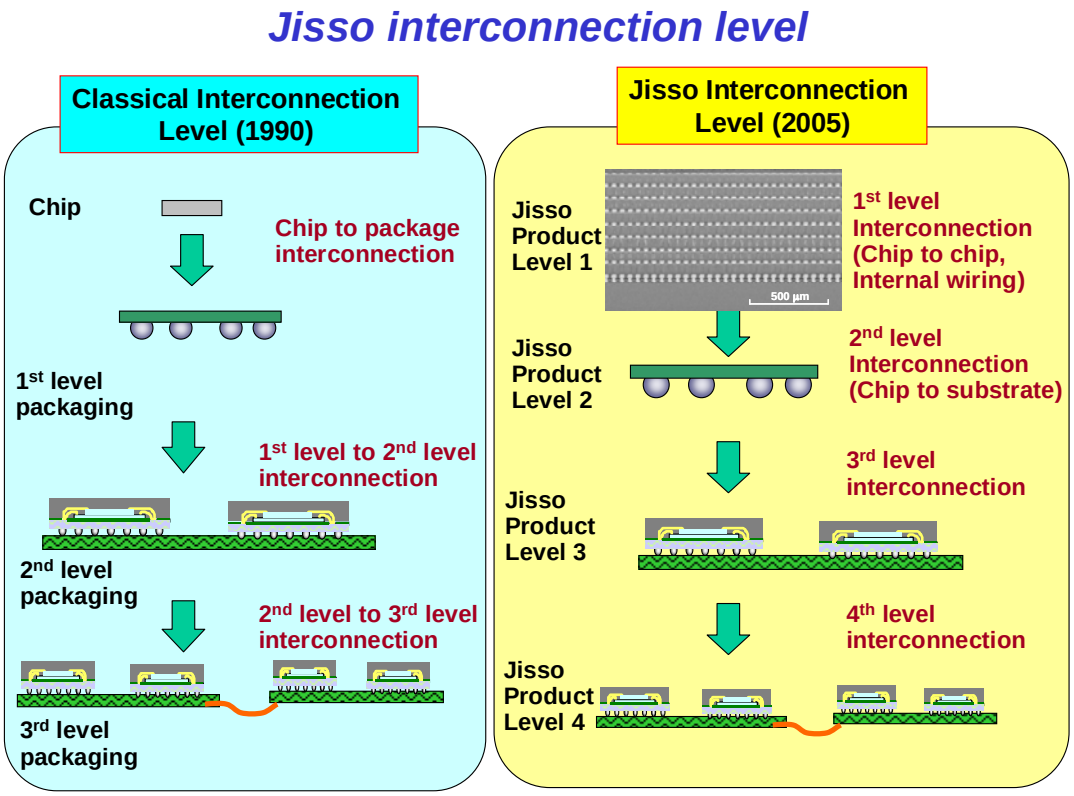


Figure 3: JISSO Interconnect Levels

SiP vs. SoC Comparison

The benefits of "more than Moore" can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future. The pros and cons for each architecture are outlined in Table 1 below.

Table 1: Comparison of SoC and SiP architecture

Market and Financial Issues		
Item	SiP	SoC
Relative NRE cost	1X	4-10X
Time to Market	3 – 6 months	6 – 24 months
Relative Unit Cost	1X	0.2 – 0.8X

Technical Features	
SiP	**SoC**
Pros	
Différent front end technologies; GaAs, InP, Si, SiGe, etc.	Better yields at maturity (this depends upon complexity)
Different device generations	Greater miniaturization
Re-use of common devices	Improved performance
Reduced size vs. conventional packaging	Lower cost in volume
Active & passive devices can be embedded	CAD systems automate interconnect design
Individual components can be upgraded	Higher interconnect density
Better yields for smaller chip sets	Higher reliability (not true for very large die)
Individual chips can be redesigned cheaper	Simple logistics
Noise & crosstalk can be isolated better	
Faster time to market	
SiP	**SoC**
Cons	
More complex assembly	Difficult to change
More complex procurement & logistics	Single source
Power density for stacked die may be too high	Product capabilities limited by chip technology selected
Design Tools may not be adequate	Yields limited in very complex, large chips
	High NRE cost

A SiP solution has the potential to reduce cost. However, only a careful calculation of all cost issues including chip areas, mask costs, yield costs, test costs, assembly and packaging costs can determine which solution offers the lowest cost. The implications of module size, substrate noise coupling and isolation issues must also be taken into account to determine which solution provides the form factor and performance required. This means a company must carefully consider their specific conditions in choosing between a SiP or SoC solution. Close interaction and alignment is necessary to understand the requirement.

Market Trends

SiP has rapidly penetrated most major market segments: consumer electronics, mobile, automotive, computing, networking, communications, medical electronics, etc. The benefits of SiP are for different market segments but the share some common elements. Time to market, size, power requirements and cost have resulted in the strongest initial penetration in mobile communications. The unit shipments are increasing at approximately 10% per year and this is forecast to continue.

2. System Level Requirements for SiP

2.1 General Requirements

The general requirements for SiP are many and the relative importance varies with the application. These requirements include:

- Small and specialized form factors
- High functional density
- High frequency operation
- Thermal dissipation
- Large memory capacity
- High reliability
- Low package cost
- Low development cost
- Rapid time-to-market
- Wireless connectivity (GPS, Bluetooth, cellular, etc.)

2.1.1 Consumer Markets drive Product Form Factors

The miniaturization of hand-held products has been ongoing at a very rapid pace and this trend to ever smaller products will continue. The size of digital video camera (DVC) was about 450 cm^3 in 2006 and is forecast to be 300 cm^3 in 2010. This is only 66 % of the current size and miniaturization will continue beyond 2010. When a body size of the hand-held product is downsized to a certain fraction, its printed wiring board (PWB) is empirically known to be downsized to the fraction raised to the second power, because the sizes of some components scarcely change, such as battery, optical lens, and LCD display. If the body size is downsized to 66 %, its PWB size will be 44 % in 2010.
To meet this target, both continued scaling of semiconductor devices and adoption of SiP packaging technology will be required. From the functional view point, many performance features such as data traffic between the processor chip and the memory chip in a SiP will have reduced noise due to the shorter path length enabled by SiP technology. Also, SiP's designs allow I/O driving forces between chips to be lower resulting in decreased power

consumption. Some digital still cameras have already shown a cut in power consumption by 50 % by incorporating SiP technology.

3. Reliability Challenges

There are many factors that determine the reliability of electronic components and systems. The factors that must be considered are similar for all systems but the relative importance changes for SiP technology. SiP products have higher thermal cycle count due to the use pattern of consumer electronics and greater mechanical stress due to vibrations and dropping for the same reason. The storage and use environments also have a wider range than many conventional electronic systems. Meeting the reliability requirements of future SiP components and systems will require tools and procedures that are not yet available. These include:

- Failure classification standards
- Identification of failure mechanisms
- Improved failure analyzing techniques and methods
- electrical/thermal/mechanical simulation
- Lifetime models with defined acceleration factor
- Test vehicles for specific reliability characterization

SiP has many applications: cell phone handsets, wireless base stations, PCs, servers, communication networks, opto-electronic links, automotives, and some are in the harsh environments. The reliability requirements for each product depend on its designed useful life and user tolerance of potential failures.

Servers, communication networks, and opto-electronic links often handle critical transactions, and all available means are deployed to recover from any temporary failures, e.g. soft-errors in memory due to cosmic ray impact, stuck-fault in memory through error correction code, check point restart or re-transmission of data packets. A common expectation in the telecom industry is a system availability of “five nines” (99.999%). This translates to only 5 minutes 15 seconds down time per year [2]. Clearly, this is a very stringent reliability requirement. As a result, hardware redundancy has also been implemented to avert system shut-down due to hardware failure. Any SiP for these applications needs to meet a commensurate reliability requirement similar to other hardware used in these systems for the product life cycle. The typical life cycle is seven to ten years for products and may be up to 20 years for infrastructure.

3.1.1 Complexity vs. Reliability

A reliability challenge inherent to the design of a SiP module is the cumulative reliability of all its constituent components. The more complex the SiP, the higher the reliability requirement of each individual component, particularly if they are all connected in series – a single point of failure could result in a failure of the entire module. As a result, redundancies are needed within the SiP module to meet its reliability requirements.

Moreover, increased complexity also means more second order effects. The interactions between the different constituent components become more pronounced and are more challenging to characterize. For example, consider a SiP with 8 memories connected to a single processor. The memory BGA interconnects will be closely coupled with those of the whole module. Strengthening one could degrade the other. Consequently, primary and secondary effects become even more critical in SiP modules.

3.1.2 Miniaturization vs. Reliability

The need for higher speed is a key driver for even more miniaturization of SiP modules; the closer the memory is to the processor, the less the delay. As a result, next generation SiPs will tend to be even smaller, with more memory and processors squeezed in as close together as possible. Moreover, the dimensional increase in processor sizes will pose additional, unique challenges for SiP module reliability.

3.1.3 Power vs. Reliability

Increased miniaturization means increased heat density (W/m2). Aside from the pure thermal challenges of cooling the SiP, the increased heat flux has a direct impact on the reliability of the interconnects. As the components run hotter, the stress fluctuations are higher as the device is power cycled, resulting in degraded reliability. In additional, the coupling of devices together means there are additional local self-heating effects. For instance, if a lower power memory is placed very close to a high heat dissipating processor, the temperature excursions that the memory will be subjected to will be higher regardless of its own power dissipation values.

Another thermal driven factor that will impact long term reliability is the thermal cooling solution implemented. If a heatsink is used, the way the heatsink is attached (in a space constrained system) could also impart mechanical stresses to the module, which would further degrade field reliability.

Finally, depending on the end use application, the overall height of the SiP could be a critical limiting factor. Due to the several levels of interconnects; SiP modules could have a higher overall height, which in turn can limit the overall height of heatsinks that could be used in a given constrained space to cool the SiP.

3.1.4 Yield vs. Reliability

SiP modules may require large area due to the potentially large number of components. Another consequence of increased complexity is more process variation and consequently, more variations in assembly parameters such as warpage, solder joint shape and standoff height. These factors in turn will impact the long term reliability of the SiP module, and need to be better characterized. In other words, there would be increased coupling between assembly yield, process variation and long term reliability. Final assembly conditions such as handling and test during final product level assembly would also play a critical role in limiting the desired field reliability of the SiP module.

3.1.5 Materials Selection vs. Reliability

The materials used in SiP modules need to be carefully selected to ensure that they can meet the unique operating environment of a SiP module. For example, the adhesives (underfills, die attach, lid attach etc.) used in the SiP need to be such that they can survive the higher stresses (both thermal and mechanical) encountered in the SiP due its larger size, weight, operating temperature and warpage compared to most single chip packages).

Similarly, for example, the solder joint interconnects selected within the SiP need to be selected such that they can withstand multiple reflow cycles and warpage variations during the assembly process.

3.1.6 End Use Conditions vs. Reliability

A SiP in a wireless base station could be in a location difficult to access at an extreme temperature and high humidity outdoor environment for a typical life cycle of up to 20 years. Power amplifiers (PA) encounter frequently turning on and off causing thermal excursions constantly. Furthermore, replacement cost of any failed hardware is unacceptably high, placing an extremely stringent reliability requirement throughout the life cycle of ten years or more.

A cell phone handset may have a product life cycle time of three years or so. However, it is likely to be dropped to the ground, or to be sit upon unintentionally. A SiP plus its mounting on the motherboard for such an application would have to meet the drop-test and other mechanical stress reliability requirement. It also has to meet high temperature and high humidity environment during its relatively short product life cycle time. The PA also encounters frequent thermal excursions between talking and listening time slots.

[1] Erico Guizzo and Harry Goldstein, “Expressway To Your Skull”, IEEE Spectrum, August 2006.

[2] Gary Audin, “Reality Check On Five-Nines”, Network Intelligence, Business Communications Review, May 2002, pp. 22-27.

3.2 Interconnect Reliability

The use of low-k ILD to reduce on-chip interconnect parasitic capacitance has exacerbated the difficultly of maintaining high thermomechanical reliability of dice assembled on organic substrates [1, 2]. Due to the fragile nature of low-k ILDs and their relatively poor adhesion to the surrounding materials, it is becoming progressively critical to minimize stresses imparted on the chip during thermal cycling and wafer-level probing. The large CTE mismatch between the Si die (3 ppm/°C) and the organic substrate (17 ppm/°C) have been shown to be destructive for ILD materials and their interfaces. Thus, this has motivated the investigation of new I/O interconnect technologies that minimize mechanical stresses on the chip. To this end, new under fill materials are being investigated. In addition, the use of solder bumps augmented with mechanically flexible electrical leads to replace under fill is also currently being investigated both in academia and industry. While compliant leads promise to fulfill the mechanical needs, their relatively high inductance, relative complexity in fabrication, compatibility with flip-chip assembly, and reliability are issues yet to be fully addressed and investigated. There are several wafer-level compliant I/O interconnection technologies that span a wide range of design, dimensions, fabrication and material requirements, electrical and mechanical characteristics, and I/O density. In most cases, the compliant interconnections are fabricated using standard microfabrication techniques and are defined using photolithography. The change in the electrical parasitics during strain and thermal cycling is yet another issue to be fully addressed and developed for the various compliant I/O technologies. For example, the loop inductance is expected to change as the leads undergo strain.

1. C. J. Uchibori, X. Zhang, P. S. Ho, and T. Nakamura, "Effects of chip-package interaction on mechanical reliability of Cu interconnects for 65nm technology node and beyond," *IEEE Int. Technol. Conf.*, 2006, pp. 196-198.
2. L. L. Mercado, C. Goldberg, S.-M. Kuo, T.-Y. Lee, and S. K. Pozder, "Analysis of flip-chip packaging challenges on copper/low-k interconnects," *IEEE Trans. Device and Materials Reliability*, vol. 3, no. 4, pp. 111- 118, Dec. 2003.

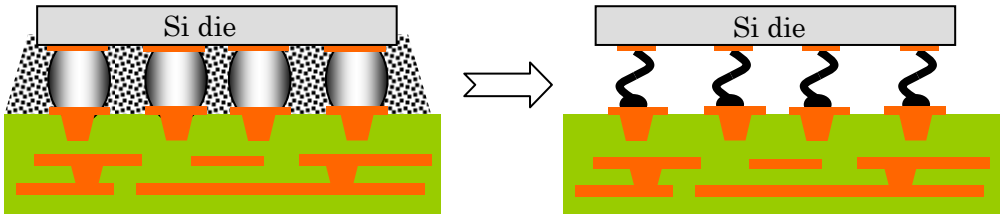


Figure 4: The use of compliant electrical I/O can potentially eliminate the need for underfill.

3.3 Interconnect Reliability of PoP

The demand for multiple features and bandwidth in today's networking products resulted in increasing needs for higher density memory components. One of the methods to address the density challenges is package on package (PoP) for Flash and DRAM. PoP has been used over stacked die packages in high end networking products mainly due to reliability and testability concerns. Driving factors for using stacked packages:

- Space constraints on PCB
- Customer can use top die package, which is typically memory from different suppliers (also ensures 2nd source).
- Shorter development cycle time using existing Si technology versus higher density memory using next gen Si node
- Use known good die with better yield and reliability

PoP configurations include stacked leaded or stacked BGA packages on flexible and rigid substrates. Some of the examples are illustrated below.

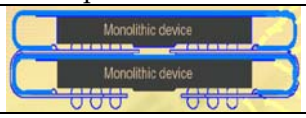
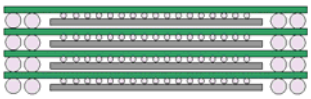
Configurations	Examples
BGA on flex substrate	
BGA on rigid substrate	
Flip Chip on ceramic substrate	
Top/bottom devices mirrored	

Figure 5: Examples of PoP Stacked Packages

Several key factors that impact PoP reliability:

- PoP component handling during SMT assembly
- Voiding due to multiple high solder reflows
- PoP warpage
- Reduction of BGA solder joint fatigue life reduced due to mirrored BGA configuration

- BGA solder joint mechanical shock robustness
- Reduction of solder joint reliability to PCB
- Multiple reflows induced package substrate pad cratering
- Drop testing

Warpage for PoP

Today digital still cameras and mobile devices are main user for PoP packaging technology. PoP packaging has become an important platform mainly to integrate ASIC and memory in a mobile phone together. Typically the logic parts belong to the bottom package and the top package is the memory. This has the advantage, when needed, that the memory density can be varied by changing the top package. For PoP packages, besides connective reliabilities of solder bumps and reliability of low k ILD, warpage is the main challenge. The warpage is due to the different CTE of the materials involved. During the last year various papers where warpage of PoP has been investigated were published (see e.g. Refs. [1-6]).

For PoP set-up simultaneous reflow on board of the two package parts is required. During this reflow process warpage appears and needs to be understood. Typically warpage of the bottom package is smiling. Top packages can have from one die to 5 or even more. Warpage is only predictable based on a careful analysis and can vary significantly during reflow from smiling to frowning depending on die stack configuration, size, and materials. Material selection is key to reach the required warpage behavior. In Ref. [3] a wide selection of die attach material and mold compound to study material effects have been investigated. In addition effects of thickness of laminate substrate and silicon ratio on package warpage have been studied. The authors found for epoxy mold compound that high Tg and lower CTE below and above Tg is required. For the die attach material higher modulus, higher CTE and low Tg is necessary. Moreover increasing the substrate thickness from 0.13mm to 0.18mm has impact on warpage. A 0.65 mm pitch for top package is required to secure enough ball stand-off. The I/Os are laid in a 2-row periphery to allow moulding of the package. Especially for high density PoP with 0.5mm top land pitch Solder on Pad (SoP) has been investigated and showed to be advantageous. For more memory stacking transfer from 0.65mm pitch to 0.5mm pitch is required. For finer pitches we require less standoff between the sub-packages. It has been found that package stacking yield is very much a factor of the materials. For top package dipping was investigated (3 materials were tested) and overall PoP design.

Poor joints occur mainly due to the warpage of the bottom logic package during reflow process, which generates gaps between solder balls of bottom package and PCB solder lands. By application of flux a warp can occur easily.

Therefore solder paste instead of flux has been used and showed improved results. Key advantage of solder paste was the ability to maintain metallic contact during reflow and accompanied warp. This was achieved by adjustment of paste viscosity and powder grain size compared to SMT solder paste.

The present results show that package design and material set must be controlled very carefully. But nevertheless warpage control needs to be investigated further. This is investigated presently when a PoP is assembled to a motherboard in single pass reflow without pre-stacking so that the connection between ASIC and memory package is formed at the same time. Here, solder paste dipping is better than flux dipping.

Another approach to manage warpage and standoff is development of MAPPoP (matrix PoP). After assembly of the die to the MAPBGA substrate strip, metal studs are formed on the top side of the substrates. Subsequently, the strip is overmolded and the studs are accessed by depth controlled grinding in connection area. The mold compound stiffens the substrate thereby reducing warpage. At the same time the standoff is reduced. This has the additional benefit that smaller solder ball can be used which in turn allows shrinkage of the top ball pitch and increasing top package density.
A third approach is the development of fan-in packages. Essentially these are package in package structures. In the simpler form, another substrate is stacked on the bottom substrate/die, wire bond connected and molded in place. The second substrate helps to balance the expansion / warpage. The biggest benefit is derived from the ball grid array pattern that the top substrate can have with pitches of 0.5 or 0.4 mm (or finer yet in the future) which allows much more freedom in package I/O density for the top package.

The present results show that for each PoP construction the set-up needs to be simulated and modelled in respect to warpage to achieve an optimum solution. But this also includes that logic and memory provider need to be closely work together to achieve a reliable PoP.
Because of this issue standardisation is not only required to combine devices from different suppliers but also to tackle the warpage problem. Standardisation that supports the warpage issue is pushed e.g. by JEITA, Japan, and JEDEC. The suggestion developed by the JEITA includes for example the area where the warpage is determined.

Two key infrastructures were developed before PoP adoption: Standardization (JC-63 and JC-11) and package stacking technology. Meanwhile a general design guide has been completed. A mold cap height of around 300um is typical. Advanced technologies like stacked die (e.g. allows 2 chips for the bottom package) and solder on pad (SOP) will lead to further growth of PoP.

Examples of Recent References:

[1] Development of thin Flip Chip BGA for PoP
Y. Suzuki, Y. Kayashima, T. Maeda, Y. Matsuura, T. Sekiguchi, A. Watanabe, Electronic Components Technology Conference (ECTC) 2007, Reno, Nv, June 2007, p.

8

[2] High Density PoP and Package Stacking Development
M. Dreiza, A. Yoshida, K. Ishibashi, Electronic Components Technology Conference (ECTC) 2007, Reno, Nevada, June 2007, p. 1397

[3] Controlling Top Package Warpage for PoP Applications
F. Carson , S.M. Lee, and N. Vijayaragavan, Electronic Components Technology Conference (ECTC) 2007, Reno, Nevada, June 2007, p. 737

[4] Platform for 3D Package Integration
W.C. Wang, F. Lee, GL Weng, W. Tai, M. Ju, R. Chuang, W. Fang, Electronic Components Technology Conference (ECTC) 2007, Reno, Nevada, June 2007, p. 743

5) PoP Requirements and Expectations
Kauppi Kujala, Semicon Japan, Symposium: "Packaging – Packaging Experts Update the Strategy of SiP, December 8th, 2006, Makuhari Messe, Chiba (Tokyo), Japan

6) PoP Assembly Technology
Yoshinori Takagi, Semicon Japan, Symposium: "Packaging – Packaging Experts Update the Strategy of SiP, December 8th, 2006, Makuhari Messe, Chiba (Tokyo), Japan

3.4 Interconnect Reliability of Stacked Die Packages

The widespread adoption and ready acceptance of stacked die package are based upon the same materials set, substrate and manufacturing infrastructure and reliability qualification methodology and criteria as the single die packages. Stacked packages substrates are based upon leadframes, rigid laminate substrates, and flex substrates. Most of the stacked die package applications today use wire bond interconnects with wirebond / flip chip hybrid emerging.

A clear advantage of the stacked die package, compared to other SiP packages, is that it has similar, if not the same, reliability performance as their corresponding single die packages, with the same standard package outline, material set, and manufactured from the same production line.

One of the most critical factors in stacked die packages is the continued reduction in overall package thickness. In order to get two, three to six die assembled into a single stacked die package with a mounted height less than 1.2 mm or less, the manufacturer is motivated to look into thinner substrates, lower wire bond loop, lower mold cap height, and thinner die. Today standard wafer thinning process (back grind and polish) are able to reach 75 um wafer thickness for 300 mm wafers. At less than 75 um yield loss for wafer will become significant. Beyond the yield loss and defect escape issues; there is no specific reliability failure mechanism specifically prominent to stacked die packages. SRAM and flash were the first circuits used in stacked die packages due to their high die yield providing known good die for stacking.

3.5 Failure classification and mechanisms

The failures in SiP are not unique to SiP technology but relative rate of occurrence may be influenced by the use cases and operational environment for SiP. Classification of failures and failure mechanism are listed in Table 2 below.

Table 2: Failure mechanisms for SiP

Basic failure mechanisms	#	Failure origins and driving forces	SiP-relevant failure examples	Fault isolation and failure analysis methods
A: Coherent crack formation	**1**	Thermomechanical mismatch	Chip solder fatigue BGA solder ball fatigue Fracture of an embedded passive component Die-to-die spacer crack Underfill crack IC metal line open	**Stress analysis** by Thermoire-Interferometry, Speckle-Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy, SEM or FIB/SEM
	2	Mechanical loading (application- or process-induced)	IC dielectric crack Organic substrate crack Solder ball crack (drop)	
	3	Hygroscopic swelling	Mold compound cracking, die cracking, substrate cracking	
	4	Reaction-induced volume shrink or expansion (e.g. curing)	Mold compound cracking, die cracking	
	5	Internal pressure (e.g. moisture vaporization at increased temperature)	Mold compound cracking, die cracking	
B: Interfacial delamination	**1-5**	Same as 1-5	IC dielectric delamination Underfill delamination Delamination between stacked dies Organic substrate delamination Mold compound delamination	**Stress analysis** by Thermoire-Interferometry, Speckle-Interferometry (ESPI), Deformation analysis by image correlation, x-ray diffraction **Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM
	6	Interface reactions causing loss of adhesion (e.g. moisture-, oxidation-, contamination- related)	Underfill delamination Mold compound delamination Organic substrate delamination	**Crack detection** by Scanning Acoustic Microscopy, Cross section analysis with light microscopy or SEM, FIB/SEM, FIB/TEM **Surface analysis** by TOF-SIMS, XPS, AES, TEM+EDX, TEM+EELS

Basic failure mechanisms	#	Failure origins and driving forces	SiP-relevant failure examples	Fault isolation and failure analysis methods
C: Void and pore formation	7	Mechanical creep	IC Solder ball fatigue BGA solder ball fatigue	**Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Void detection** by x-ray microscopy or x-ray tomography Cross section analysis with light microscopy, SEM or FIB/SEM (with EDX,WDX, EBSD and x-ray diffraction for analysis of intermetallics)
	8	Diffusion (Kirkendall void formation) and Intermetallics formation	IC UBM lift Void in IC interconnect or in via Wire bond lift BGA solder ball lift	
	9	Electromigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
	10	Thermomigration	Void in IC metal line or solder, Void in solder, metal line or via in the BGA substrate	
D: Material decomposition and bulk reactions	11	Chemical corrosion	Bond wire lift	**Fault isolation** by Magnetic microscopy, Time domain reflectance, Lock in thermography, TIVA, OBIRCH **Failure analysis** by Cross section analysis with light microscopy or based on FIB/SEM with EDX or WDX, TEM, TOF-SIMS, XPS, FTIR spectroscopy, , mechanical testing, TGA, DMA, DSC (ageing), EBSD (grain analysis)
	12	Galvanic corrosion	Bond wire lift	
	13	Ageing (UV, …)	Organic substrate cracking or delamination Underfill cracking or delamination	
	14	Grain coarsening, phase separation	Wire bond rupture IC solder ball fatigue BGA solder ball fatigue	

4. Simulation Tool Requirements

4.1 SiP Electrical Simulation Tools Requirements

With increasing frequency, and performance, it is necessary that chip, package and board should be co-designed to optimize the performance, increase the density and reduce the overall product cost.

Having separate tools for chip, package and board, today design methodologies are not consistent and therefore leading to higher design cycle time. In every design, the tool should be intelligent enough that can optimize the design at all levels. In such unified tool environment, the design flow should be consistent and efficient to reduce the design cycle time. For complex and high performance designs, it is necessary that the electrical modeling tools should be integrated with the physical design tools, so that the performance can be predicted while it is being co-designed.

Very often, the material and design rules from different suppliers are different and result in non-consistent characteristics of the components. Thus, it is important that a consistent material data base be generated and integrated with the co-design tools so that correct performance can be predicted.

The signal integrity tools are the critical analysis tools for predicting the performance for the given design. With the requirements of higher density and lower cost, the electrical tools can provide guidelines for selecting material and providing design trade-offs. Thus the integration of electrical modeling tools with the physical design tools is very important. Today we see several electrical modeling tools, each having unique capabilities, but lacking their integration to the co-design environment. Therefore, there is need to integrate the EM tools that can predict both the signal and power performance at the system level.

Every designer uses the tools to do electrical modeling in different way. What is right or wrong? The proper methodologies need to be developed and validated with measurements. During the system design cycle, signal integrity (SI) analysis is needed at different stages of the design:

- Early stage SI where the system is defined and components are selected
- Pre-layout SI where the design rules are generated to start the design
- Post-layout SI where the signal integrity analysis is performed on the entire designed system. Accuracy of the models becomes critical.

There is need to integrate such type of analysis capabilities within a signal

integrity tool. It should be user friendly to the level that even non-expert engineers can perform such analysis.

In the analog-digital mixed designs, the density at the chip or package level may cause crosstalk noise from digital to analog. The modeling tools should be capable of doing that analysis and help correct the design accordingly.

Current tools cannot handle large complexity of the model. As a result the models are simplified and therefore suffer poor accuracy. To handle the complex models, advanced computers and large memory are needed. The fast and efficient algorithms for EM tools need to be developed/optimized so that they can solve the complex problems in less time with less memory.

4.2 SiP Mechanical Simulation Tools Requirements

SiP presents new challenges for mechanical properties. The incorporation of different devices and materials which present varying heat load, unmatched CTE, different thermal conductivity and a variety of elastic properties results in a complex structure. These structures have dynamic response to mechanical stimuli which may come from changing temperature; vibration in the environment, externally applied forces, etc. Simulation tools that can predict SiP package mechanical behavior are essential to determine if the design requirements are met before fabricating a SiP. The requirements for these simulation tools include:

- Static stress simulation for SiP complex structures
- Dynamic stress simulation for SiP solder reflow undergoing power on-off cycles
- Mechanical properties of materials used in the SiP structures
- Interfacial adhesion properties

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4.3 Thermal Simulation Tools Requirements

SiP solutions will combine chips with different power density very close to each other and therefore these chips will heat each other. For good thermal design the power maps of all heat sources are needed in order to predict hotspots. Simulation tools should be able to read in power maps of active devices as well as trace layout details of interconnects to calculate additional resistive heating in substrates and other interconnect structures, where very fine and dense wiring might occur. As this often cannot be modeled in detail, a two step procedure should be incorporated in the tools.

First calculation of substrate thermal conductivity and resistive heating for selectable substrate patterns before adding the chips. To do that, simulation tools should be able to read in substrate layout data. After adding the chips with their power maps, locally distributed trace heating and thermal conductivity, the complete heat generation pattern is there and hot spots can be identified. However, that is only the first step.

Next is to optimize thermal design. Simulations should have the capability to shift heat sources around on a plane or in a stack in order to minimize peak temperatures. That requires parametric modeling and interlinking to optimization tools, open interfaces to external optimization tools. Depending on technology, active and passive components have specifications of lifetime or failure critical temperature. The ratio of temperatures to critical temperatures is needed, e.g. Simulation capabilities needed include:

- Simulation capabilities for advanced hot spot cooling solutions are needed, e.g. for thermo-electric cooling, spray cooling, phase change, etc.
- Time and temperature dependent modeling of diffusion and electro-migration is needed, especially with always smaller dimensions of features. Thin layers may disappear in processes.

- Multi-physics coupling like electro-thermal, thermo-electric, and thermo-mechanical should be as easy and fast as possible because most processes, stresses and failures are temperature dependent.

4.4 Lifetime Models and Acceleration Factors

Time to market is a parameter that determines success or failure in the consumer dominated electronics market today. The short product life cycles, cost sensitive markets and the requirement for timely market introduction limit the time available for product development. The product life/reliability must therefore be determined during the design cycle rather than through the traditional method of building prototypes and extensive testing. The use of lifetime models with appropriate acceleration factors defined will be required to meet these cost and time to market requirements. The parameters modeled may be product specific but will include some or all of the following.

- Mechanical shock
- Mechanical vibration
- High temperature storage
- Thermal cycle bias voltage stress
- High humidity bias voltage stress
- Bending
- Pull strength of bond wire or other joints
- Power cycling

5. Requirements for Performance

5.1. Electrical Performance Issues with SiP

System-in-Package (SiP) presents new design complexities over traditional single chip packages. The configuration of multiple dice connected at the package level, is essentially a subsystem, and as such, a SiP is expected to have interactions between different dice. Electrically, signal integrity and power integrity of the entire package must be maintained through careful design of the package.

In terms of signal integrity of a SiP, crosstalk is a very important issue due to the increase in signal count and reduction in physical spacing between traces connecting different dice at the package level.

Giga-Hertz signal transmission presents a challenge in a SiP, especially, in a thin film environment, where dielectric thickness may be restricted due to

materials and process limitations. For example, SiO_2 of several micrometers thickness as inter-metal dielectric is impractical from process point of view. And lossy transmission is a reality system designers may have to deal with due to decreased signal line widths resulting from increased signal densities. Signal integrity may be further degraded due to reflections at impedance discontinuities such as I/O pads to substrate interconnects or embedded vias.

In a mixed signal SiP, where digital and analog circuits may reside closely in a single module, sensitive analog traces must be properly isolated from fast digital traces. Circuits generate noise that can couple to other circuits on the same die or within the same SiP, also known as substrate coupling or substrate noise. High performance circuits, such as PLL or high-speed digital links, are more sensitive to electromagnetic interference noise. Electromagnetic interference remains a major challenge for SiP integration. Innovative designs are in need to enhance or replace the conventional approaches like physical separation and barriers.

Furthermore, timing skew and impedance matching may also be an issue due to the increases in signal count and operating frequency. Groups of traces need to meet timing constraints, which may require physical layout iteration due to signal crowding and trace impedance requirements.

Additionally, traces may be physically long causing unacceptable parasitic capacitance, resistance, and inductance values. The higher wiring density required for SiP forces narrower traces and therefore increases interconnection inductance. For example, the bond wire of a die that is stacked on 3 other dice will have higher inductance values than the bond wires of the 3rd die in the stack, which will in turn have higher inductance values than the bottom flip-chip as in the case of a hybrid stacked SiP. This will significantly affect signals waveform as they undergo transients. In terms of power integrity, SiP design also poses challenges. One technique is to share voltage supplies between different chips on the same plane. This reduces supply impedance that ameliorates the problem of simultaneous switched noise (SSN). However, sharing supplies could create a noise conduit between the different chips. Care must be taken to analyze effects at the IC level coupled through the package design. Yet if the supply noise is unacceptable, separate or split planes should be used for the different voltage supplies. These split planes need to be carefully planned so that return paths need to be minimized, which may be difficult because of die stacking. Overall, electrical design of SiPs becomes complex because of the interactions of different dice and connects to the IC design itself.

5.2 Electrical Performance - I/O Trends

SiP has broad applications with a wide range of performance requirements on operational environments. The electrical requirements depend on the signal

speeds and the active and passive components utilized in the SiP,

For servers and communication networks, a large processor with high I/O count and a large amount of memory may be implemented in a SiP. The die-to-die coupling among stacked-memory ICs and the coupling among bond wires should meet the operating requirement of the memory ICs. A large number of wiring nets with fast rise and fall times will be needed in the SiP substrate. And a large number of simultaneously switching off-SiP I/Os with fast transition time will also be needed. Impedance of all wiring nets, including vias and I/O leads to the motherboard, should be carefully matched throughout each wiring net. Cross-talk noises among adjacent wiring nets should meet the design specification needs. Voltage and ground planes in the SiP substrate and the leads to the motherboard should meet the simultaneous switching output requirements.

For opto-electronic links, the extremely fast transition time and high current from the laser driving circuits on the IC to the laser diodes are needed. On the receiver end, the fast transition time from each photo detector could be a very small signal. It cannot afford to pick up any noise from digital switching circuits. Careful electrical shielding for the receiver section is needed on the SiP substrate. The noise could come from signal wiring nets, including vias between voltage and ground planes. It could also come from the far-field radiation from other switching nets. Another factor which needs to be looked into for noise optimization is the number of different power rails. Adding more rails and keeping well isolated analog power supplies helps reduce noise but also adds a lot of complexity and cost.

The wireless base station could have a large number of power amplifiers (PA), one for each active user. The output power of each PA should be carefully regulated according to the distance to its user. When several PAs and the associated control ICs are placed on a SiP, interference among them should be controlled to within the required specification.

The SiP for a cell phone handset could integrate the baseband digital IC, the memory IC, the up- and down converters, the PA and associated diplexer and filters, plus other passive components. Some of the components could be surface-mounted or embedded in the SiP substrate. The reference planes and vias for the RF section should be carefully isolated from the digital section. The interference between the transmission and receiving paths, including the bond wires, has to meet the specification requirement. Some of the passive components and bond wires could be critical elements for the RF section or the phase-lock loop. Their values and placement and the bond wire profile should meet the overall design requirements.

Assigned budget for timing as well as noise variations is getting very tight for systems in general. With the standard materials available for die/package/board interface, the loss in the system will dictate SiP solutions. A less complex signal driver/receiver in SiP solution could potentially have benefits to a very complex driver/receiver in a single chip solution in terms of

die area, power etc. System in package greatly helps in this matter only if all the components are designed simultaneously with tradeoffs being considered at every step. If each of the components such as die/package/board is being designed separately, interactions between the components could ruin the design. For example the capacitance on the die along with the package/board inductance could excite resonances which could affect the die in consideration. In SiP, this situation only gets worse since couple of other devices could be sharing the same power supply. It is absolutely essential to perform system level simulations and tradeoffs integrating all the components.

The trend in the last couple of years has been high speed IO and significantly high speed core circuitry for the high end ASIC/uP applications. For designing a system with GHz signals, die-package, package-board, board-connector discontinuities are playing a major role.
It is easy to design controlled impedance traces which form the major part of the signal path in terms of electrical length. The impedance discontinuity at the interfaces between chip/package/board/connectors needs to be minimized. ESD capacitance, package features such as big pads which couple capacitively, vias with pads, return path for signals, etc need to be designed carefully to propagate multi-GHz signals.

With tighter bump pitch and package pin pitch, one of the advantages of SiP is to densely pack components. This and the trend towards differential signaling drive routing density in the packages. The crosstalk in the trace section as well as the via section could be a limiting factor. Adding layers is quite cost prohibitive in some packaging technologies, hence it requires a system level optimization of placing signals bumps/pins at the right place.

We are looking at potential IO solutions in the 10 - 15 Gbps regime. The total loss from driver to receiver is in the range of 10 - 15 dB. This type of budget makes it difficult to have large system buses. Loss in every part of the signal path must be modeled. These models will be accurate only if they are based on measurements. It is very crucial to characterize the material till 40 GHz or so to get good simulation parameters. Good test vehicles with appropriate standard structures as well as via transitions, variable antipad/pad dimensions etc in a material set have to be built and characterized for studying signal integrity.

6. Power Requirements

As silicon technology progress towards the 45 nm generation and beyond, the difficulty of power delivery becomes exacerbated. As chip power dissipation increases and supply voltage decreases, chip current drain increases. This leads to an increase in IR losses across the power distribution network. Moreover, increases in chip operating frequency lead to increases in Ldi/dt noise. Collectively, the IR-drop and Ldi/dt noise account for total on-chip supply noise. Given that the supply voltage is decreasing, the ratio of supply

noise to supply voltage is increasing with each technology. As a result, power delivery presents a grand challenge for overall SoC and SiP performance. Co-design of the SoC and SiP substrate in which the appropriately sized on-chip metal wires and area are allocated for the power distribution network and the appropriate number of power and ground pad are allocated is vital to SoC/SiP operation [1]. Too few power and ground pads will cause an increase in the on-chip IR-drop across the power distribution network, which increases power supply noise and increases gate delay variation. These effects consequently degrade SoC performance and cause the SoC to operate well below its intrinsic limits at each particular generation of technology. As a result, it is critical that the number of power and ground pads is scaled accordingly with each technology generation and appropriately sized on-chip wires and area are allocated for the power distribution network. The inductance of the chip/package I/Os and the on-chip power distribution network also contribute to the power supply noise. As a result, adequately large decoupling capacitors must be integrated both on the silicon die (SoC) and the package substrate. Hot spots, which are due to non-uniform power dissipation, exacerbate the above described challenges.

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6.1 Electrical Current Density

Transistor density on silicon devices will continue to follow Moore's law for at least the next 5 years. At the same time, gate thickness will continue to decrease with each new node of wafer fab technology, although this trend is starting to see signs of slowing.

Power leakage increases exponentially with gate length, caused by quantum tunneling through the gate oxide. For some of the new technology nodes this leakage is very high, in some cases accounting for nearly 50% of the power consumed on a chip.

These two factors (increased transistor density and increased leakage) combine to cause increased power consumption and therefore increased electrical current density on the silicon device. Typically static power dissipation contributes up to 30% of total power dissipation.

Note that core power and ground pins tend to have much higher current density than signal pins or their associated power/ground for the signal buffers. Therefore, core power and ground pins tend to have higher failure rates. These pins will typically be directly under the die shadow in a device.

Since the 1970's it has been understood that electromigration and thermomigration can affect the reliability of 1st level array interconnect (flip chip). There are dozens of papers in the literature on this topic. The

industry, particularly for high power consumption products, is rapidly approaching a cliff edge beyond which the bumps cannot carry sufficient current. The transition to lead-free bumps eased this a little, improving the current density limit by up to 3X or so relative to eutectic solder.

The problem with flip chip bumps is exacerbated by two additional problems. First, in conjunction with new silicon technology nodes, flip chip bump pitch is decreasing, leading to a decrease in bump diameter and effective area for electrical current flow. This alone causes increased current density at the bump.

Second, the current is not evenly distributed throughout a bump, but rather tends to crowd at one section as the current seeks the path of least resistance. This leads to joule heating at the current crowding region and the resulting increased temperature and current density at that point leads to early failure of the bump.

This problem is no longer confined to first level interconnect. Increased current, temperatures and decreasing metal feature sizes are leading to electromigration and thermomigration in other portions of the device. These include, but are not limited to:

- SMT solder balls on WL-CSP in which ball pitch is dropping to 0.3mm (250 micron diameter balls)
- Connector pins in array-type connectors
- Vias in Package Substrates
- Vias in Printed Wiring Boards

Increased system-level power and cooling problems also have a negative effect on the reliability of the above interconnections as temperature is a key input variable in Black's Equation (given below).

Black's Equation is a good predictor for electromigration in wires and thin traces, but is a poor predictor for bumps or other structures due to current crowding effects. Nevertheless, Black's equation is useful to understand the importance that temperature plays in the reliability of the interconnect. Increased temperature has three causes:

- System-level temperature
- Localized temperatures caused by variations in cooling efficiency within a system
- Joule heating of conductors due to high current density

There is no standard test methodology for electromigration and/or thermomigration in the industry today. In 2007 JEDEC started an activity to develop such a standard.

*Black's equation originates from the reference:
J.R. Black, Physics of Electromigration, IEEE Proceedings, 1983

One form of this Arrhenius-type equation is:

Nx= (A/J^n)e^(Ea/KT)

Where:

A = rate constant
J = current density
n = current density exponent
e = 2.718281828459
E_a = Activation Energy
K = Boltzman's Constant
T = temperature, K
N_x = time to x% failure

6.2 Voltage

SiP opens the door for system level integration. Unfortunately interfaces like USB, Display, PCMCIA and some memories still have the demand for a high supply voltage.
Also the efficient use of the present and future CMOS technology requires power and voltage management to control the analog dynamic range or the digital supplies in embedded solutions.
This will lead to multiple voltage domains in SiPs and power management will be an embedded function forcing more interactions and design emphasis on voltage regulators, power delivery and package design. Thus, we have to deal with different voltage domains with level shifters in between different subsystems and the challenge will be to guarantee the integrity of each domain.

On the other hand all interconnects like FC, Si Vias, etc. are scaling in an unfriendly manner increasing the resistance between the different subsystems. Thus, substrate noise and supply noise will increase requiring a well organized supply noise management.

Present and future CMOS technologies require a supply voltage below one volt to avoid gate-oxide reliability issues and device degradation due to hot carrier stress. SiP solutions are subject to increasing feature sets which leads to higher performance requirements along with higher power drain. Increased power consumption along with reduced core voltage leads to high current flow. A high current results in a voltage drop along power supply rails which further challenges the whole power supply concept and power management. Beside this, reduced supply voltages cause a limitation for signal swing. Keeping the same signal to noise ratio demands a further reduction of noise power. That means that any noise on the power supply must be below a certain limit to not compromise the product specification. This issue requires more stabilized and lower noise power management systems.

6.3 Power Integrity

The continuous scaling of feature size drives a similar decrease in the operating voltage of integrated circuits. At the same time there is a continued increase in the number of transistors per IC and an increase in switching speed. The result of these trends is an increasing difficulty to ensure power integrity. The decoupling capacitance needed to ensure power integrity for digital ICs is linearly proportional to “power”, inversely proportional to “square of voltage”, and inversely proportional to “switching frequency”. The inductance between the power supply and the transistors must be decoupled with adequate capacitance to avoid fluctuations in power supply voltage at the transistor level.

The inductance associated with the package, particularly for wire bonded die, may be such that decoupling capacitance is required on the die itself. This has been utilized by DEC’s alpha microprocessor IC for example. In the 45 nm generation and beyond, it is better to utilize the decap integrated in the IC. Even though the embedded memory may offer de-coupling for the digital section, the inductance of the metal lines between memory and digital sections could become excessive. It may be necessary to embed the decap for the digital section inside or next to the digital section.

There are a number of approaches to improve power integrity as feature size and power supply voltage continue to drop. These include:

- Flip chip die attach can be used to reduce inductance.
- TSV based interconnect can provide a major reduction in inductance
- Ground and Power planes in the package substrate will help minimize power line droop and ground bounce.

6.3.1 Power Delivery

Power Integrity issues have become a more important factor in proper electronic circuit behavior as feature sizes and operating voltages shrink and electrical currents increase. Many elements in concert amplify the effects of the power delivery network on the performance of both discrete semiconductor devices and SiP products. Among the most important of these are the faster switching speeds of each generation due in part to the continued miniaturization (scaling) of device transistors, the reduction of power supply voltages to 1.0 volt and lower, the greater number of simultaneously switched outputs on each chip, and the increasing density of package designs. These issues are most important for SiP architectures which contain multiple chips and other components in a single package.

Faster switched currents generate increased voltage drops (noise**)** independent of the power supply potential due to power supply and package interconnect inductive elements. This circuit noise becomes a larger percent of the power rail as the operating voltage is decreased and currents increasing

the probability of false switching somewhere in the circuit. The package power supply conductor structure may also exhibit a resonant behavior due to distributed capacitive and inductive elements which can further interfere with the operation.

In general, core logic elements internal to a chip have a separate power supply from the I/O driver supply. However, it is common that the core and driver elements have the same ground supply leading to possible mutual interaction. In the case of a SIP containing digital and analog components, this common ground supply can result in significant circuit performance problems since the noise tolerance of the analog devices are generally low [1].

The I/O drivers themselves connect to package conductor paths for transmitting information to and from the SiP components. This signal delivery network has a unique set of issues that must be controlled to operate properly such as impedance control and delay. This is especially true for single ended wide buss drivers where many outputs may switch at the same instant in time causing ground bounce and voltage droop due to the high current being drawn in a short time. The instantaneous collapsing rail voltage can then cause slower switching speeds at the output drivers that will result in jitter and timing problems.

The power delivery network operating characteristics are further complicated by the type of output drivers used. In standard CMOS drivers employing P and N channel transistors for instance, the current driven in and out of the signal port is sourced from the power or ground supplies depending on the state transition direction. There is the possibility that both output transistors could have a momentary overlap in their “on” states giving rise to the so-called “crowbar” current flowing from the power port through the ground port directly. This effect can generate significant additional noise in the power and ground circuits.

Differential I/O schemes use two signal paths driven out of phase. The receiver end amplifies the difference in the two signals so significant coupled noise cancelling results. Since the sum of the current in the two branches is near zero, little noise is generated in the power supply circuit as well. However, any imbalance in the driver circuit will result in some power delivery noise.

Measurement of noise is sometimes achieved by observing the voltage on a “quiet line” at an output port with the associated driver held in a low (or high) state while other drivers are allowed to switch continuously. This is called Simultaneous Switching Noise.

All of these noise sources provide many opportunities for failure of an integrated circuit. In more complicated SiP structures more conditions for failure may exist. The power density can be higher in SIP formats [3] and the proximity of signal paths will be closer. However, there are also power integrity advantages associated with the SIP architecture. Signals transferred

between devices internal to the SIP have much shorter path lengths as compared systems implemented with traditional system architecture. This reduces power required for output drivers, leading to lower power consumption for the SIP design. Further, SIP architectures provide opportunities to use more advanced off-chip interconnect schemes such as Through Silicon Vias (TSV). The TSV's provide much shorter path lengths and lower resistance and inductance than bond wire structures for signal and power delivery [4].

The addition of passive elements, such as capacitors, resistors, and inductors, is also incorporated in the SIP format [5]. The judicious placement of decoupling capacitors in the SIP is an effective remedy for power and ground resonance issues. The implementation of a Balun device into a SIP interposer layer has been demonstrated in an RF application [6]. In this application, a via fence and planes were added for shielding the radiation from the balun to other components.

In the future, several areas of SIP design will need improvement to optimize power delivery. The guarantee of Power Integrity in the design phase of a complex SIP will require advancements in CAD tool capabilities to include:

- multiple stacked devices overlaid with power delivery components
- Integral Interposer design including interconnect via features
- Passive elements on defined nets
- Descriptors to reveal 3D properties of features (i.e. bond wires, etc.).

Co-design discipline is needed early in the design phase of SIP packages [7]. Chip and package design flows need to be integrated to allow this. Defining the electrical representation of package elements is required in a fast and efficient way. This package model can then be combined with model of the active components to provide a system simulation file. The level of power integrity can then be observed by computer simulation. This requires a common data base and fast modeling processes for an acceptable system.

These models and tools are needed to analyze the impact of the power delivery variations on circuit performance (both analog, RF and digital circuits), as well as to calculate the necessary countermeasures at the design stage. This implies finding techniques to determine the location and the magnitude of decoupling capacitance, the amount of guarding, etc. Note that this requires chip-package co-design in an early design stage, since the actual SiP package configuration has a large impact.

Validation methods are also necessary. Structures that have classical solutions or well-known test formats can serve as benchmarks for the industry. These are not defined at this time. Measurement efforts using test chips or laboratory signal sources can also provide data to evaluate the accuracy of the modeling methods.

6.3.2 Electromagnetic Compatibility

The increase of electronic and wireless appliances as well as the required coexistence between various communication systems which are now often integrated in the same SiP makes Electromagnetic Compatibility (EMC) an important design parameter that should be evaluated in the design flow. Designs must meet EMC regulations, both in terms of susceptibility and emission. This problem is critical in SiP implementations where embedded inductors, etc. can pick up EM signals detrimental to system performance.

Electromagnetic interference (EMI) can couple into an analog IC through the I/O pins and through the supply and interconnect lines hereby impairing the IC performance. Analog integrated circuits are more easily disturbed by electromagnetic interference than digital circuits since they don't have the benefit of dealing with predefined logic levels which ensure some immunity to disturbances.

It is important to ensure that EMI is linearly filtered and/or attenuated, in order to prevent common EMI induced change in DC bias, which is inherently present when non-linear circuits and devices are used. Internally protected I/O pins, as well as circuit blocks exhibiting a high power supply rejection ratio (PSRR) form two of many mandatory requirements in the design of robust analog IC's, providing significantly higher tolerance to EMI levels.

Design tools are needed to analyze these EMC effects at an early stage in the design flow. In particular, tools are needed to pinpoint and locate EMC weak spots in designs, so that designers can modify their designs before fabrication. This requires the development of models for all components of a SiP to be able to analyze the EMC effects with sufficient accuracy and reliability.

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7. Thermal Management

The high junction-to-ambient thermal resistance resulting from an air-cooled heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of the roadmap. Today, a massive heat sink, which is typically much larger than the chip, is attached to a Si chip through a heat spreader and variety of thermal interface materials (TIM). Not only does this provide a very large thermal resistance between the chip and the ambient, but also limits the chip packing density on the substrate thereby increasing chip-to-chip wiring length, which contributes to higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses. The ITRS projected power density and junction-to-ambient thermal resistance for high-performance chips at the 14 nm generation are >100 W/cm^2 and <0.2 °C/W, respectively. The main bottlenecks in reducing the junction-to-ambient thermal resistance are the thermal resistances of the thermal interface material (TIM) [1] and the heat sink. The need for TIMs that exhibit mechanical stability during chip operation, adhesion, and conform to fill the gaps between two rough surfaces generally yields materials with relatively low thermal conductivity, and thus correspondingly high thermal resistance. To address this need, new TIMs are being explored. In one example, the integration of carbon nanotubes (CNTs), which exhibit very high thermal conductivity, within a TIM's matrix is being investigated [1, 2]. Further in depth information may be found in the 2007 ITRS Chapter on Emerging Research Materials. For example, it has been shown that the overall thermal conductivity of epoxy can increase substantially with the integration of CNTs [1]. However, their integration with such materials requires carefully processing to prevent poor dispersion and weak bonding with the polymer/epoxy matrix in order for the overall thermal conductivity to substantially increase. Research is on going to fully demonstrate CNTs as TIMs.

The size of a heat sink may be scaling inversely compared to CMOS technology in order to keep the junction temperature constant as power dissipation increases. Not only does this prevent the reduction of system size with each technology generation, but also prevents close proximity placement of high-performance chips both in the lateral axis and the vertical axis (3D integration). The key to addressing the thermal problem at the heat sink level is to increase the heat transfer coefficient between the fluid and the surface of the heat sink [3, 4]. To this end, the use of microscopic size fluidic channels with forced liquid cooling offers a range of values for the heat transfer coefficient that is orders of magnitude larger than that possible from forced air cooling. Microfluidic cooling was first demonstrated by Tuckerman *et al.* in 1981 (cooling of ~1kW/cm^2 was demonstrated) [3]. The most important feature of the micro channels is their large surface-to-volume ratio, which leads to a high rate of

heat transfer (or heat transfer coefficient). Microfluidic heat sinks and forced liquid cooling appear essential for the 3D integration of microprocessors. However, there are many technical challenges associated with their implementation which include how to integrate the microfluidic heat sink with the electronic chips, how to deliver the fluid (packaging), and how to produce fluid flow at the required pressure.

The most common fabrication technique for micro channels requires the use of anodic wafer bonding technology, which requires smooth and clean interfaces, high pressure, high temperature (>350 ºC), and high voltage (>500 V). Unfortunately, such a process technology prevents the direct integration of the fluidic micro channels on the CMOS chip. Instead, the microfluidic heat sink must be fabricated using a second substrate and attached to the back-side of the die using a TIM (which increases the overall thermal resistance). Methods of forming CMOS process compatible thermofluidic heat sinks and the use of flip-chip microfluidic (micropipe) I/O interconnects have been recently reported [5-6].

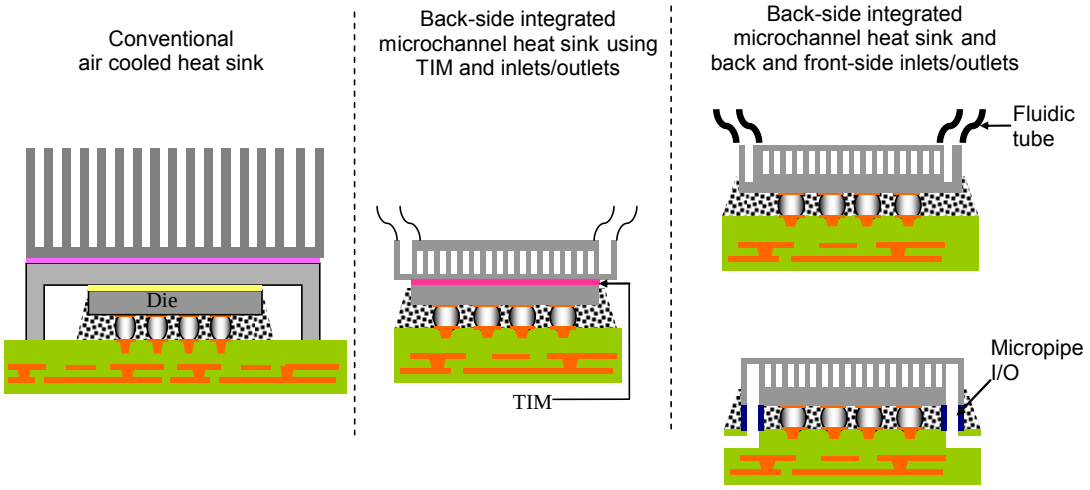

Figure 6: Examples of heat sink technologies and integration of fluidic interconnections with CMOS chips

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An example of integrated cooling technique which is able to effectively cool 3D modules with heat dissipation of 100 W for each layer (total 200 W for two layer modules) are being demonstrated. The cooling solution includes carriers that act as substrate having electrical interconnects and fluidic micro-channels. The development of leak-proof carrier is one of the challenges in this approach. This demonstration includes the fabrication of carriers with micro-channels, through silicon via (TSV) and electrical routings. This type of approach is aimed at 3D packaging of high power devices with applications in avionics and radar systems.

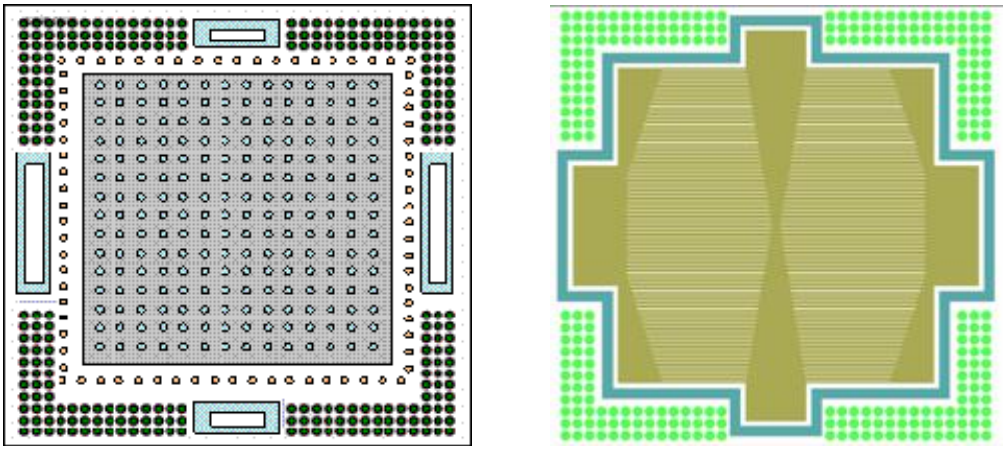

Figure 7: The schematic diagram of the carrier:
top view of carrier (left) micro channel pattern in the carrier (right)

With application of SiP into consumer products where there is a drive towards small component form factor, increase in performance, device density and functionality and limited or no active cooling, system and component level thermal management will become increasing important for SiP and for system integration. Typical examples of such products are as game consoles, smaller format laptops; advance cell phones where with a hot device inside a system and hot spot inside the hot device will require hot spot thermal management.

7. I. Hot spots

Hot spot thermal management may limit the thermal solution of the component. Even when the total power of the component remains within design

specification, the hot spot power density increase could limit the device performance and reliability. For a SiP thermal management must take account of the hot spot thermal dissipation within the die as well as within the package. For example, the side-by-side configuration, the additional challenge over the single chip packaging with individual heat sink, is the need to deal with the increased total power. For stacked die configuration and for embedded device configurations the decreased volume and available exposed surface provide significant challenges to the thermal engineer.

7.2. Component temperature limits

The component temperature needs to be controlled because:

- The higher temperature will impact device performance (lower frequency)
- The higher temperature may result in higher leakage power which is a waste of energy
- The higher temperature will result in faster degradation of the material property and reliability
- The higher component temperature will increase thermal mechanical stress in the package and system impacting reliability and product system life.

The component temperature limit is determined by its function, architecture, and design. For example, the typical Tj_max for microprocessor is about 100C, while the typical Tj_max for memory device is about 85C. Since the different devices inside the same package may have different function, their Tj_max may be different from each other.

In addition to the thermal design requirement of a single chip component, the thermal design for SIP needs to accommodate both the total power dissipation and the individual power dissipation.

7.3. System thermal dissipation requirements

Thermal design needs to be considered at the system level instead of the individual component level. This is because the system cooling design addresses the total system composed all the components inside a system. For example components will heat each other inside a system so that even the low power component can possibly get hot if its neighboring components dissipate excessive heat.

Thermal design needs to consider die-to-die, component-to-component, system-to-system thermal interaction, and the operating environment. The

statistical design will include worst-case scenario and the typical use conditions.

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For low profile systems, especially those using 3D devices, various package and system level thermal solutions should be considered. The hot devices need to be located with due consideration for various primary heat flow paths as shown in figure 6.

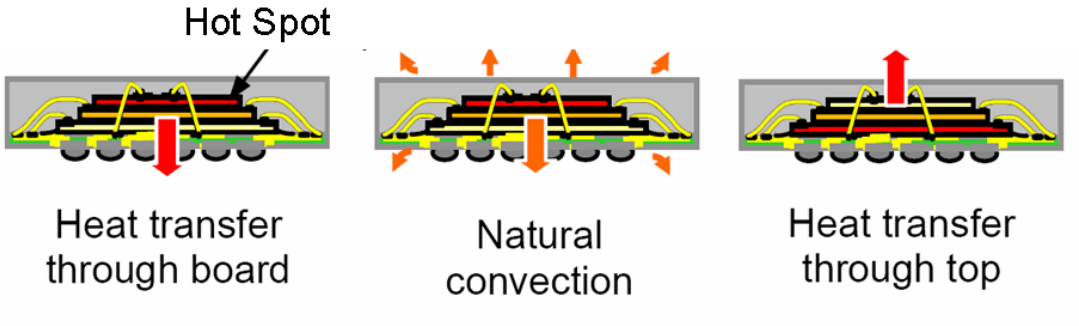

Figure 8: Location of High Power Die vs. Primary Heat flow Path

The hot spot generally occurs farthest from the primary surface used for heat dissipation. The higher power devices need to place closest to the primary heat dissipating surface. Technology improvement to the primary heat flow paths needs to continue. For top side heat flow path, use of higher conductive molding compound, embedded heat spreaders and improved package to casing thermal interface material are potential thermal management options. For bottom side, i.e. board side, heat flow path, thermal performance enhancement options include use of thermally conductive under-fill between package and board, dummy solder balls between package and board, embedded heat spreader within the package substrate, and high conductive die attach between die and die to substrate. System level enhancement options include use of thermally conductive enclosure, venting grill, piezoelectric actuators close to the device as shown in figure below.

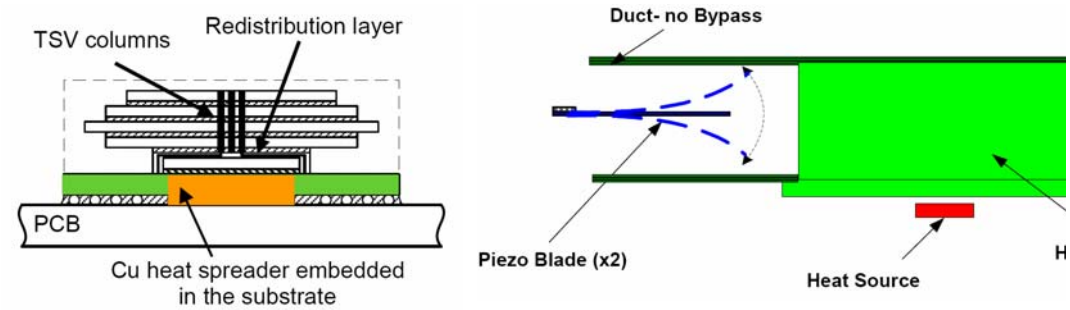

Figure 9: Heat spreaders and Piezo-electric actuator

7.4 Thermal issues for Processors and Memory

As time-of-flight becomes an increasing fraction of system latency, it will

become necessary for processors and their associated memory controllers to be moved together onto the same package. The resulting package will be similar in appearance of past years, with a single processor surrounded by several, typically two or four, secondary chips.

What will be different will be the average power and power distribution of the chips. As multicore chips become mainstream, the number of cores per chip can be expected to follow its own growth trend. Mainstream processors with 8, 16 or 32 cores will appear, resulting in significantly improved power uniformity. Unlike dual core chips with two cores crowded against one side of the chip, future multicore chips are likely to have the hotspots dispersed more uniformly over the chip surface.

In packaging a multichip module with one high power and several low power chips, the preferred technique has been to locate the module lid precisely above the processor chip, permitting use of a thin layer of thermal interface material (TIM). The inevitable variations in chip height and planarity are accommodated by use of gap-pad (conductive elastomeric) TIM which results in significantly higher thermal resistance than that of the processor. Since the processor power density is typically several times that of the memory controllers, resulting junction temperatures of all chips are similar. Average processor heat fluxes as high as 100 W/cm^2 can be accommodated by inorganic TIM or possibly advanced organic or nano-materials in the near future.

Packaging density of air-cooled electronics is dictated by heat sink frontal area requirements, with about 2 - 3 W/cm2 as a practical limit. This frontal area requirement is only weakly affected by the flow length of the heat sink, which unfortunately is usually the dimension with the least restriction. Moving the heat from package to air with pumped liquid cooling does not relax the heat sink (in this case liquid-to-air heat exchanger) frontal area requirement, but does allow the heat exchanger to be located remotely rather than directly above the module.

Maximum allowable junction temperature is expected to decline slowly, at a rate averaging about 1 C per year. However, leakage power concerns may lead to operation at temperatures considerably lower than maximum allowable. The reduction in processor power consumption from 85 to 55 C may exceed the energy required by a refrigeration system to reduce the junction temperature from 85 to 55 C. Thus, a refrigerated system could consume less total power than non-refrigerated system. In addition to energy savings at the user level, significantly less power would have to be routed through the packaging.

8. Equipment and Assembly Issues

8.1 Equipment Requirements and Challenges

Continued shrinkage of component dimensions is placing demands not met by existing equipment. SiPs utilize the smallest components possible including 0201 and soon 01005 size SMT parts. These small parts impose material management challenges because the value of the part is not marked on the part; the parts are so small the space available is inadequate. Thus, verifying the value of a part once it is taken off of a reel is difficult; a meter and isolated contact points are needed. That implies that reels must be carefully managed to ensure the correct parts are used. First article inspection of machine setups must be rigorous to avoid errors. Placement machines to routinely handle 0201 size parts are widely available. Machines to place the smaller 01005 are becoming available. Nonetheless, some challenges remain such as tombstoning, sticking to feeder tape, etc.

Packaging has traditionally met the device or end use application requirements through evolutionary changes in size, wire length, higher IO thin packaging approaches. However, today there is increasing pressure to develop entirely new package technologies to meet the requirements of end use applications. Multi-chip packages (MCP) with die side by side have been around for many years. MCP with this option increases the planar x- y dimension requiring OEM to increase the board and system real estate. An alternative of this is the die stacking that has become a dominant package solution as it increases the product capacity and performance without any constraints in the planar dimension. The stacked die packages are now followed by stacked Package on Package (PoP) and Package in Package (PiP).

The widespread adoption and ready acceptance of Stacked Die Packages and the more recent Package on Package and Package in Package are based upon the basic premise that these packages are all readily designed, manufactured, and tested on existing manufacturing tools, materials set including substrates, and equipment. Stacked packages are based upon commonly available substrates including leadframes, rigid laminate substrates, and flex substrates. Most of the stacked die package applications today use wire bond interconnects with wirebond and flip chip hybrid emerging. In the same way Wafer Level CSP package are based upon the manufacturing technology and infrastructure of flip chip wafer bumping technology and infrastructure and BGA ball drop technology and infrastructure.

Evolutionary development such as for wafer thinning process, thin substrate development are key enablers to address the requirements for packing more dies in a package while meeting the package height reduction challenges.

More recent assembly and packaging innovations such as advanced Wafer Level Package and System in Package have specialized equipment requirements. Current equipment used for wafer level packaging is often modified front end processing equipment. New generations of equipment will be required for wafer level interconnects structures and specialized under bump metallurgy, TSV and embedded wafer level structures. Examples

include: solder bumping, passivation, redistribution, through via interconnect, integrated passives, backside metallization, optical interconnect, dies to wafer and wafer to wafer bonding and post processing thinning. Improvement in throughput and operating cost (cost of ownership) are essential for meeting the cost reduction requirements of the market place as reflected in the Roadmap.

Equally important the equipment for the current set of processes must be able to handle very thin wafers and die in high volume and high through put and high yield manufacturing. .

Discussions on equipment for TSV and related technologies will be found in Section 19.

Wafer thinning equipment exists today but new equipment will be needed as wafer diameter increases and the die thickness continues to decrease. The principal issues will be stress relief and surface thickness variation including roughness. Wafers thinned to 10 µm or less will require improved processes such as dry polishing, dry etching and other process combinations.
Another important equipment requirement will be for wafer or chip handling after thinning. Equipment for ultra thin wafer handling, singulation and ultra thin die handling (e.g. pick and place) will require new technology. In addition, a new generation of die and wafer carriers such as wafer tape and glass plates must be provided to enable safe handling after thinning.

Emerging System in Package products require assembly process equipment with greater versatility and precision. Assembly of SIP with a variety of IC types, optical devices, MEMS devices and biochips on the same substrate will require substantial extension of current assembly equipment capability. Examples include improved molding equipment to meet the requirements of wafer level packaging and SiP MEMS and new dicing equipment required (laser dicing vs. plasma etching vs. dicing with diamond blade saws) for ultra low k dielectrics.

8.2 Assembly requirements and challenges

A major proportion of the SiP technologies in use today are based upon Stacked Die Packages, and side by side packages. The widespread adoption and ready acceptance of Stacked Die package, Side by Side package and the more recent Package on Package and Package in Package are based upon the basic premise that these packages are all readily designed, manufactured, and tested on existing manufacturing tools, materials set including substrates, and equipment. Stacked packages are based upon commonly available substrates including leadframes, rigid laminate substrates, and flex substrates. Most of the stacked die and side by side package applications today use wire bond interconnects with wirebond and flip chip hybrid rapidly emerging.

In the same way Wafer Level CSP package are based upon the manufacturing technology and infrastructure of flip chip wafer bumping technology and

infrastructure and BGA ball drop technology and infrastructure.

Evolutionary development such as for wafer thinning process, thin substrate development are key enablers to address the requirements for packing more dies in a package while meeting the package height reduction and form factor challenges.

The complex inherent stresses within the package along with introduction of Low K silicon materials are drawing a great deal of attention to design and develop material and processes ensuring desired product performance. These issues include long wire bond, lower loop height, finer pitch multi tiered design, improved die attach material for optimum thermal performance for wire bond packages. In flip chip the design and fabrication of UBM and bump metallurgies and underfill materials for flip chip assembly require significant research and development. Each and every assembly process step is extremely critical to address the packaging challenges.

More comprehensive discussion on 3D packaging technologies will be found in Section 16.

8.2.1 Wire Bonding

Wire bonding has been the workhorse of the semiconductor industry. Ninety percent of die to substrate (including leadframe) connections are made in wirebond. It is the dominant method for interconnecting to semiconductor device. IC devices, wire bonded to various forms of lead frames and organic substrates and molded in epoxy molding compounds have been the standard of the industry for years. Despite repeated predictions that wire bond technology has reached its practical physical limit, wire bond technology continues to re-invent itself with new innovative concepts and technology improvements. Multi-tier wire bonding has provided good practical solutions to meet increased IO requirements. Wire bonded stack die packaging has proved to be a versatile method for SiP and memory packaging.
In order to meet thinner and more densely integrated package requirements lower profile wire bond loops are necessary. Innovations such as forward bond loops with 50 µm loop height are in production. (See Section 16 for more detail on wire bonding technology)

There is a well established global infrastructure and supply chain for wire bonded and molded packages from design practices and tools, materials, manufacturing processes, and equipment.
For die stacking the near term challenges include lower profile bonding to meet the drive for smaller form factor and low profile consumer electronic products. Improvements in molding compound materials i.e. flow and filler size are needed for these low profile packages. The industry has been developing faster wire bonders, larger format substrate assembly, and more efficient molding processes to address the market demand for efficiency and cost saving. In a wire bond package the cost of gold wire is a significant fraction of the total package cost. The reduction of gold wire diameter to 20 um for lower

pitch applications has provided cost benefit in the face of historic high gold price. In the long term such cost improvements efforts are approaching their practical limits and are of diminishing returns. The work ongoing in the industry to lower cost wire bond materials, i.e. copper vs. gold wire, may contribute to continue the cost reduction trend for this interconnect technology. While copper wire bond has been in use for 50 µm wire diameter and thick bond pads, for general fine pitch applications replacing gold wire with copper wire utilizing the existing infrastructure would require very significant efforts across the supply chain. The bond pad thickness and metallurgy will need to be optimized for cu wirebond for bond strength formation and no risk of damage due to the higher ball bonding force. In a similar manner careful work to understand the fundamental for the 2nd bond will be necessary.

8.2.2 Flip Chip

Flip Chip and wire bond are the two standard processes to connect die to a substrate. Flip Chip processes were originally developed for multi-chip applications on ceramic modules. It has become the standard die interconnect solution for organic substrates for microprocessors and graphics processors. The key elements are: wafer bumping (UBM and bump metallurgy), underfill, TIM, and build-up substrates. For these applications flip chip pitch, at 150 µm, is limited by availability of high volume cost effective substrates and high volume defect free underfill processes, with higher Pb free temperature, higher Tj, and increased current density. There are requirements to improve underfills, replacing UBM structure, high lead solder and lead free alternatives, and TIM materials in order to meet the demands of future technology nodes and market applications. Copper pillar wafer bumping is being introduced in microprocessor applications. The advantages are in electrical/thermal performances with the potential for lead free bump implementation.

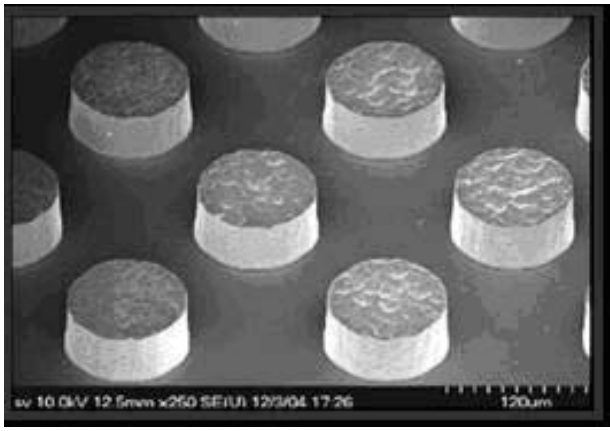

Figure 10: Examples of copper pillar bumps

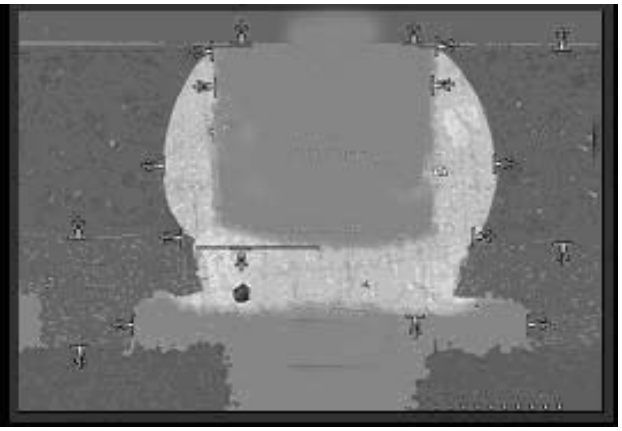

Figure 11: Examples of assembled copper pillar

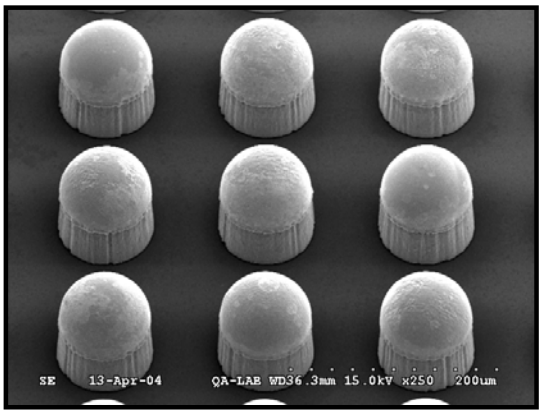

Figure 12: Examples of copper pillar bumps with solder tips

For applications beyond the microprocessor, graphics and game processors, Flip Chip packages have other technical requirements. For example die are typically smaller with lower IO array pitch, smaller UBM openings, and low profile small package format requirements. Drop tests are important in mobile applications. Relative cost of buildup substrates may be too high. These flip chip packages may be stacked onto other flip chip and wire bond packages. Analog and RF ICs have different electrical requirements than digital only applications. Potential solutions include redesigned UBM, copper pillar or flexible sets interconnect, large format overmolding (no underfill) processes, fluxless reflow and PoP and PiP package structures. There is an opportunity for a new generation of flip chip structures, materials, manufacturing processes and equipment to serve the industry for the More than Moore era.

8.2.3 Molding

Conventional bottom-gate molding has been a highly successful workhorse for the industry. For some complex stack dice and complex SiP package there is risk for excessive wire sweep and yield loss. New developments in top center mold gate (TCMG) provides a radial mold compound flow from a top gate that minimizes wire sweep and filler separation that can occur as the fine pitch bond wires filter out part of the fillers as the compound moves between them. There is also avenue for reducing stress on the substrate compound interface during de-gate as the contact is smaller and the breaking stress can be optimized by various design features. TCMG requires a smaller clearance from the top die, allowing a thinner package, particularly important for molding mold cap below 300 µm.
Compression molding is just entering the market. The liquid mold compound is dispensed onto the substrate before it´s placed into the mold die. No gate is needed and the mold flow speed is minimized preventing wire sweep. A new approach introduced recently is underfill molding for flip chip in package solutions.

Thin packages are prone to warpage, and chips with low-k dielectrics are more sensitive to stress. In both cases, low modulus molding compounds are in

development to minimize the problems.
A novel approach to reduce or eliminate the occurrences of wire shorts, particularly for stacked die packages, in molding is the use of insulated or coated wire. Coated wire has been in development for a few years and has achieved some level of technical success. However the high cost of coated wire and limited supply has limited its application and prevented its broad proliferation into the industry.

To reduce stack heights, new materials that allow direct die attach to the top of the bonded wires with subsequent reflow around the wires are now being explored. This approach would adds cost to the process but may be more easily deployed as it is a substitutional cost increment and not completely additional.

8.3. SiP Assembly Line Organization

SiP assembly presents a factory organizational challenge. Many SiP designs require a broad mix of assembly technologies; conventional SMT with solder stencils; dispense of DA attach materials; die placement; flip chip die placement; solder reflow, sometimes with different temperature solders; wire bonding; underfill of specific die; overcoating of specific die; overmolding; marking and finally singulation by sawing or punching. Traditional factories are not designed with all of these processes routinely available. These processes tend to be separated and run by units that do not usually work together. SiP assembly will require that these separate groups work together and this will require realignment of equipment to facilitate efficient process flows and short cycle time.

9. Challenges and Requirements for Materials and Processes

9.1 SiP Substrate and Assembly Processing

One of the challenges in designing a SiP is selecting the most suitable substrate. Substrate selection is made after the schematic is developed, the BOM is complete including the size and configuration of all the parts, the number of units to be built over the life of the project is estimated and the environmental requirements are established.

Substrates for SiP packages vary in their requirements with the specific package feature or type of SiP being designed. One might also observe different specifications depending on whether the SiP package is conceived as a chip package like a PoP, a RF or wireless module or an interposer type board. Designs from the packaging community typically utilize their accustomed materials (e.g. BT or equivalent cores, Taiyo solder mask, etc.) and design rules. Designs from the board or EMS community tend to use their materials (e.g. FR-4 cores) and their design rules (e.g. HDI board design rules).

The most common substrate choices are listed in the next table along with typical applications and characteristics.

Table 3: Comparison of SiP Substrates

Comparison of Substrates Used for SiPs		
Type of Substrate	**Typical SiP Application**	**NRE, Piece part Cost, & availability**
FR-4 substrate	Used for low pin density flip chip & wire bonded die, especially when combined with some SMT parts, and lines and spaces >100 microns are adequate. BGA and LGA footprint compatible. Least expensive, most available.	Lowest NRE, part cost and availability.
FR-4 with built up layers	Used when fine lines (<75 micron) are required. Uses BGA IO.	~5 X higher NRE and part cost vs. FR-4. 8~8 week availability
Flex circuitry	Used for flip chip, wire bonded die and SMT parts when folding is useful. Usually has BGA IO.	NRE and part cost comparable to FR-4.
Silicon substrate	Used when very fine lines (typically <15 microns) are needed.	High part cost today is major challenge
Lead frame	Used when the interconnects between the components is simple, LGA footprint is acceptable and only limited routing is required.	NRE and part costs similar to FR-4. 2 week lead time for new configurations.

Thin (<0.5mm) printed circuit boards, often made with 4 metal layers, FR-4 dielectric and microvias, are commonly used for Land Grid Array SiP packaging. Since SiPs are small (usually less than 35 mm x 35 mm) and will usually be overmolded, the substrates are usually highly panelized in strips (say 200 mm x 75 mm with hundreds of SiPs per strip).

9.2 Alternate Substrate Materials

While FR-4 is the most common substrate material, other dielectrics, flex circuits, silicon substrates and even ceramic substrates are used for specialized applications.

Another FR-4 like substrate in common use has a core made with conventional circuit board fabrication methods and then one or two outer layers built up using a “deposited” method. That usually means sputtering a metal layer, patterning using semiconductor like lithography and microvias to develop 15 micron lines and spaces. This technology is commonly used for BGA substrates and will find some use in SiPs.

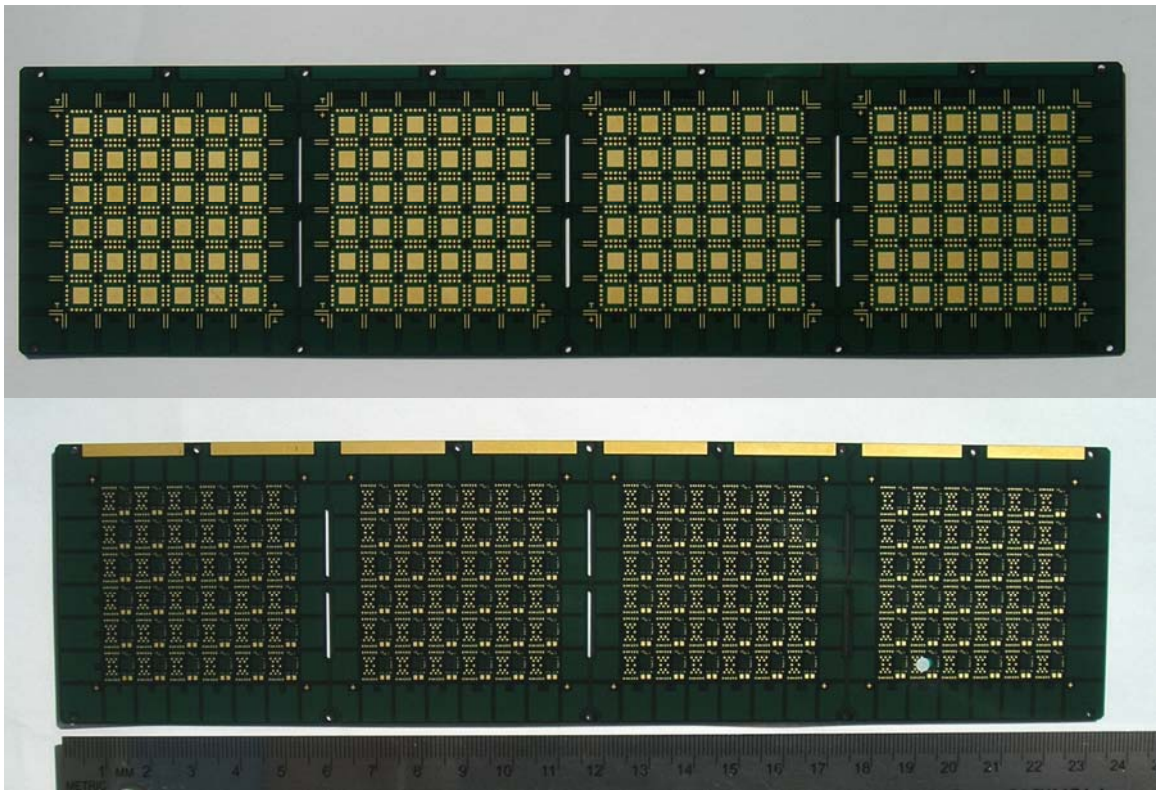

Figure 13: Example of substrate commonly used for BGA packages

Silicon substrates are sometimes used when fine lines are necessary. Using even course semiconductor lithography like technology, 10 micron lines and spaces are viable.

One particularly attractive substrate is a simple plated copper leadframe. These leadframes are suitable if the interconnects to the components and the "pin outs" are simple. An example of a leadframe is shown below.

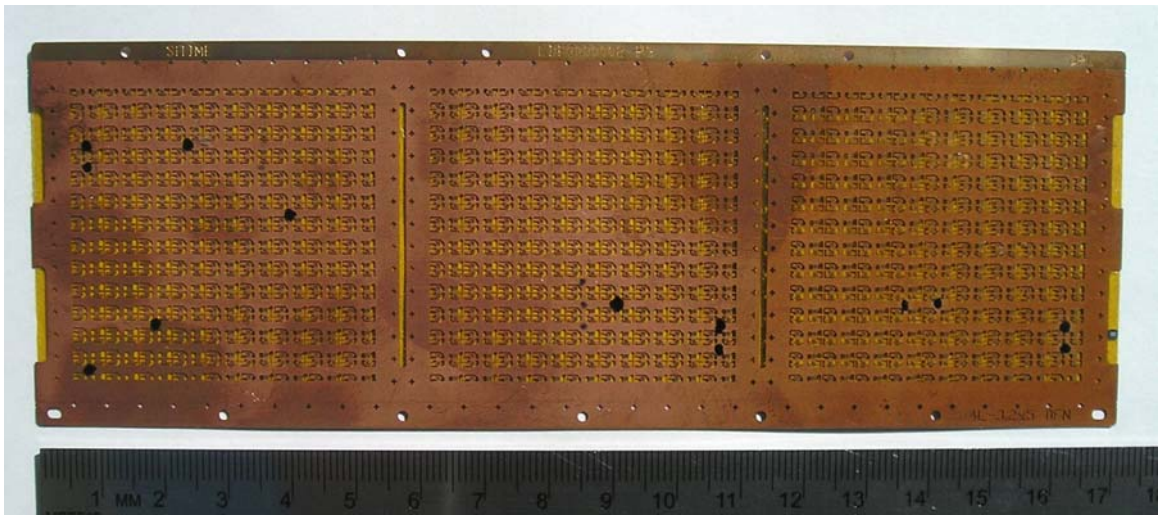

Figure 14: Example of Cu plated lead frame substrate

Leadframe substrates are suitable for some stacked die configurations and some side by side packages. They also have good thermal properties due to the copper die pad on the bottom that can be used to remove heat. The final package has a QFN footprint and is often thicker than the usual 0.8 to 1.0 mm height of a standard QFN to accommodate multiple stacked die.

The unique requirements of embedded substrates are described in section 15.4.

9.3 SiP Assembly Challenges

Panelization

If SMT placement is necessary, a panel with multiple strips side by side (say 200mm x 300mm) is a good configuration that minimizes handling and cost.

After SMT is complete, these panels are divided into strips (say 200mm x 75mm) for die placement, wire bonding, overmolding and marking. Each strip often has 4 arrays to facilitate molding. After marking the SiP array is typically saw singulated for test and packaging.

Singulation

An alternate to saw singulation is punching which is often used for high volume, especially if the package is small (<5 mm x 5mm). While punching is lower in cost than sawing, more expensive molds and punches are required. Fortunately, these tools are size specific and can be used on any project that requires the configuration they are intended for.

Handling the SiPs as panels and/or strips of multiple units can reduce cost substantially.

9.4 Challenges of low k and ultra-low k dielectrics

Many companies began shipping production ICs with low k dielectric as early as 2003. Major bench marks incorporating low k dielectrics include:

- Reliability in packaging low k pushed production back at least 2 years beyond roadmap
- 2006 was ramp year for Low-K
    - 90 nm node High end processors, graphics and ASICs
    - Low K production almost entirely based on CVD carbon doped oxides
    - Subcons now qualified for low k package assembly

The incorporation of ultralow k dielectrics in 2007 posed new challenges for packaging including:

- Materials interface critical – adhesion, moisture, …
- Probe damage control
- Fine pitch wire bond
- Flip Chip thermal stress management

Advanced low k materials are being introduced and qualified at state of the art FABs. Often times this means that along with the reduced hardness and fracture toughness of the Low K dielectric there is a shrink in pad geometry. This complicates the issues by combining fine pitch wire bonding with new pad stack technology. Bonding equipment and materials are being developed to minimize or more evenly distribute the forces that can cause damage to the pad stack. Additionally pad stacks are being redesigned with innovative methods to withstand or protect the underlying structures from these forces.

Challenges and Developments for Wire Bonding to low k and eliminating pad damage include:

- Controlling ultrasonic energy – since ultrasonic (US) energy is the primary cause of pad damage
    - Pure US transducers design not to have any unwanted vibration nodes
    - Capillaries that are designed to normalize the stress and strain forces that the pad sees
    - High Reliability wire that can achieve good reliability test results for fine pitch (especially automotive) applications.
    - Softer wires are desired but are in conflict with other requirements for wire sweep
    - Reducing impact force from Z axis touch down

- Designing Pad stacks with Low K materials to withstand wire bonding forces
    - Al pad thickness – models and actual bonding studies have shown that thicker Al pads transmit less wire bond stress and strain forces to the underlying structures – going from 0.8 um to 1.0 or 1.2 can make a big difference
    - Via design – Models and actual bonding studies have shown that peripheral vias withstand wire bond forces much better then area vias under the pad – this have been confirm with wire bond testing
    - Top metal – Ni Pd or Ni Pd Au pads can protect pad stacks - Nickel is very hard an provides a substantial barrier to wire bond forces and prevents nailhead degradation

- Pad over Passivation – Rectangular pads extending over the passivation can separate the pad stack from wire bond forces

SIP incorporate stacked die and therefore have special requirements for molding compound as follows:

- Improve filling capability in narrower gap
- Improve moldability over bigger MAP
- Reduce wire sweep even with finer and longer wires
- Reduce package warpage with temperature change

Higher fluidity and lower viscosity are needed. Due to narrower gap, filler migration tends to occur, which can cause voids and incomplete fill. Finer filler is also effective in addition to lower viscosity to prevent this. In general, finer filler causes viscosity increase therefore, some features are needed to compensate. Filler sphericity increase and filler distribution optimization can contribute to some level.
Package warpage change over temperature, especially warpage at hot, needs to be reduced. Mold shrinkage should be optimized for each package configuration.

9.5 Die bonding for SiP

The die bonding materials will need to provide new features in the near future including high thermal conductivity, photosensitivity and compatibility with the requirements of thinned die. Die bonding film (DAF) is used in Stacked Multi Chip Package (MCP) which is the main stream of SIP at present. New requirements for DAF include:

DAF for thin wafers

Wafer backside lamination using DAF is the main stream of stacked MCP production at present. The challenge of handling thinned wafers (e.g., below 100μm) for laminating DAF and dicing tape separately has resulted in reduced yield.

Thin DAF

DAF must be thin to meet the requirements of ever thinner packages.
The low adhesion strength of conventional thin DAF does not meet the requirement. Thin DAF with improved high adhesion strength is a requirement.

DAF for wire access in Stacked Die

In case of stacked MCP of the same size chip stacked a dummy chip is used

to give space for the wire bond. At present, the process using wire penetration film is supposed to be used in accordance with thin wafer and thin package. DAF with low viscosity is necessary in such a process.

DAF for Laser Dicing

Laser dicing is emerging method most likely to be adopted for thinned wafers. Stealth dicing* is one of the laser dicing method to divide wafer by expanding.
In such a process, DAF which is divided by expanding is necessary.
(Stealth dicing* was developed by Hamamatsu photonics co.,Ltd.)

9.6 Challenges requiring future Development

- Currently, DBG process requires DAF attachment on the wafer after grinding and additional DAF singulation process. Eliminating this additional process requires new DAF material having cleavage fracture characteristic so that it breaks easily at the expanding mechanism in the die attacher. Or DAF could be attached on a package substrate.

- TSV wafers are repeatedly stacked and bonded until all wafers are integrated. It means the first wafer is exposed at high temperature for the longest duration. To solve these inconsistent heat exposure periods, simultaneous bonding process is needed, such as repeating alignment and temporary wafer attachment at lower temperature and annealing for metallurgy alloying at once.

- Simplifying the TSV wafer stacking requires simultaneous wafer bonding for TSV bumps and dielectric adhesive.

- Carrier support system for extremely thin wafer is preferred to be eliminated or simplified for cost saving.

- The effect of the stress and strain on the circuit from wafer bond adhesive and terminal bond shall be studied for extremely thin wafer with TSV interconnection.

10. SiP for Specialized Functions

10.1 CPU and Memory

The memory type of memory such as SRAM, DRAM, Flash memory etc and the number of components of each type must be identified at the outset of any CPU and Memory SiP.

SiP architecture for CPU and Memory can then be defined. Examples of such architectures include side by side, stacked die, and embedded die SiP. Each configuration requires further understanding and defining a set of requirement.

High bandwidth interconnection schemes need to be defined based on considerations which include the number of data lines, interconnect density, data speed, driver power dissipation at CPU and Memory interfaces. Each SiP configuration would generally require reduction of the interconnect length. The silicon design must be optimized to take advantage of the short interconnect length to reduce power dissipation, transmit/receive circuit and increase data speed. Design automation is needed to support this optimization.

Good quality power delivery to both the CPU and Memory must be provided.

A cooling solution needs to be found for the CPU and the Memory. The solution schemes will be dependent on the SiP configuration. Much research is needed for embedded and stacked die configuration.

Testability of individual component need to be comprehended so that known good die conditions can be achieved for high product test yield.

10.2 High Power SiP

For industrial applications like power generation, automation, building controls and automotive applications such as hybrid car power devices/systems the trend is for higher integration of power and power controls to reduce size and improve efficiency. The output power per unit volume and cost per function are the key areas for market success. Innovation will enable highly integrated power modules based on new high power System in Package technologies. In the last 5 years this integration has resulted in volume reductions in the range of 60-70% with significant improvement in energy use efficiency. The introduction of SiP solutions will enable further shrinks in the range of 70-80% with continued improvement in efficiency. This progress depends on continued research in the area of new materials; interconnect technologies, heat dissipation, circuit design, thermal management and modeling and simulation tools.

10.3 Optoelectronic Components in SiP

There are unique packaging challenges associated with the incorporation of Optoelectronic components in SiP devices. SiP incorporating optoelectronic components must take into account the unique requirements for minimal light loss and high precision alignment as well as accommodating the high thermal

density associated with many optoelectronic devices. Minimizing light loss requires:

a. Robust designs to maximize output.
b. Minimal absorption by optical and/or semiconductor elements.
c. Minimizing refractive index interface difference losses and undesired scattering.
d. Achieving and maintaining good coupling to optical sources and detectors.

The precision alignment requires sub-micron accuracy and stability in operation of the optical chain, especially for single mode fiber coupled to edge emitting laser die. In addition, the dissipation of heat from high power laser die and high brightness LEDs is required to maintain the temperature stability during operation and thereby control hot spots in the SiP and minimize wavelength drift of the optoelectronic components.

A key bottleneck to the realization of high-performance microelectronic systems, including SiP, is the lack of low-latency, high-bandwidth, and high density off-chip interconnects. Some of the challenges in achieving high-bandwidth chip-to-chip communication using electrical interconnects include the high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to crosstalk.

As a result, the motivation for the use of microphotonics technology to overcome these challenges and leverage low-latency and high-bandwidth chip-to-chip communication has been presented in the literature (for example, [1,2]).

Significant progress has been made in developing chip-to-chip optical interconnects [3,4,5], which include fiber-to-the-chip schemes (in one example, an optical signal is coupled to a silicon-based taper), have been reported. Free-space optical interconnects are also being pursued for chip-to-chip communication. Susceptibility to misalignment and complexity in packaging are challenges yet to be fully addressed for these optical interconnection technologies.

Guided-wave interconnects using polymer waveguides, which are batch fabricated on the substrate, are being pursued as yet another alternative to enable optical interconnection. Polymer-based waveguides offer some advantages that include high density, optical confinement, and ease of fabrication.

In one approach, the optical devices, such as detectors (PDs) and sources, are integrated within the package substrate and are interconnected using the polymer waveguides. If the optical devices are integrated on the Si through either monolithic or heterogeneous integration, the polymer optical waveguides route the optical on the substrate to a point directly beneath the chip where the optical sources and photodetectors (PD) are located.

A coupler, such as a mirror, is used to couple the light vertically from the substrate to the chip, and vice-versa. Depending on I/O power budget and bandwidth, such a free-space optical I/O places constraints on the tolerated vertical and horizontal offsets between the optical devices on the chip and the substrate. The use of lenses to alleviate some of these tolerances have been demonstrated but at the expense of fabrication complexity and density. Lateral alignment deviations may be caused either during assembly or thermal cycling, which is important due to the coefficient of thermal expansion (CTE) mismatch between the chip and substrate. Such misalignments could severely reduce the optical power delivered to the PD thereby increasing the bit error rate (BER) and reducing bandwidth. Moreover, such free-space optical I/O schemes have not been shown to be compatible with underfill processes.

The use of vertical optical waveguides, or polymer pins (or pillars), between the chip and the substrate has also been proposed. Some of the optical interconnection technologies are illustrated in Figure 15. These packaging solutions may incorporate chip to chip interconnect within an SiP or provide a long range, high bandwidth communication channel between and SiP and other electronic systems or components.

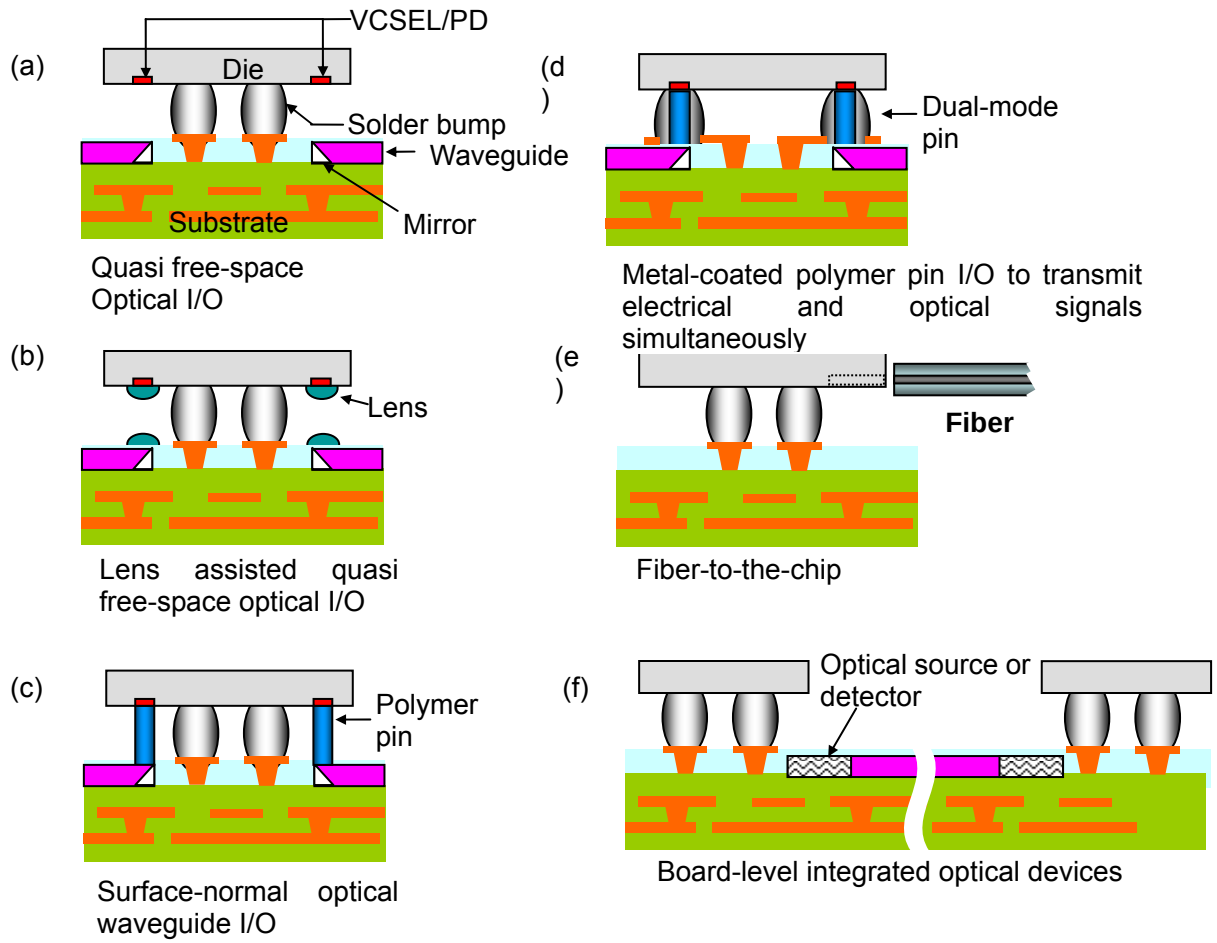

Figure 15: Examples of representative guided wave optical interconnects (first level I/O).

Challenges and Potential Solutions for Optoelectronic packaging are listed in Table 4.

Table 4: Optoelectronic Packaging	
Challenges	Solutions
Optical Transceivers	
New Technology at high data rates is mostly discrete assembly	Greater integration at subassembly with automation
Higher densities in applications	Further reduction in size by increasing densities of optical signals by use of new interconnect technology. Use of more free space interconnects.
Increased mechanical and environmental stresses for FTTX applications (Hill 2007)	Lower reliance on direct contact lens applications, increased development in mirror and bandsplitter technology
Chip Level Interconnects (Haurylau 2005)	Material selection, development of low loss waveguides, use of free-space optics
High Brightness LEDs	
Raise the electrical to optical conversion efficiency	Improve the semiconductor materials, packaging materials and package design
Dissipate the heat	Improve the package materials and design
Reduce the cost	Improve assembly processes & equipment. Configure factories to produce these products and materials
Optically Based Sensors	
Find needs and create economically viable solutions.	Develop a broad understand of the optical technologies, the components available and the economics of the application.
Methods to build stable optical chains	Materials that do not change from exposure to water, UV, heat, aging or the chemistry of the application environment.
Develop standards for the optical components	Industry collaboration

A more detailed description of the challenges of packaging optoelectronic devices can be found in the 2007 ITRS Assembly and Packaging Chapter.

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Advanced Packaging, vol. 26, pp. 122-127, 2003.
4. M. Bakir, B. Dang, and J. Meindl, "Revolutionary nanosilicon ancillary technologies for *ultimate*-performance gigascale systems" in *Proc. IEEE Custom Integrated Circuits Conf.* (CICC), 2007.
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10.4 RF and Millimeter Wave Packaging

Mobile phones are the driver for RF packaging up to a frequency of 5 GHz. Today mobile phones include more and more frequency bands for the various standards like GSM, GPRS, EDGE, UMTS or the new HSDPA (High Speed Downlink Package Access) standard. In addition mobile phones include more and more functionalities like GPS, WLAN, WiFi or Bluetooth, which are related to RF. Typically the RF part of a mobile phone consists of an RF front-end, a transceiver and a power amplifier (+ power management) chip including passive components like SAW and BAW filters or RF MEMS. General trend is higher system integration. Today already SoC solutions for RF parts which include GSM, GPRS, EDGE, and HSDPA exist.
Today for transceiver with less I/Os (often single band transceiver) VQFN type packages, which are comparable cheap, are typically used today. But also due to improved front-end chip design VQFN type packages appear for multi-band applications, because less I/O are achieved. LFBGA type packages are typically used for more complex transceiver, which include multi-bands. Transceivers are also set-up for higher integration as System-in-Package, including e.g. SAW filters or even baseband parts. In today's new mobile phones one can also find transceiver with WLP type devices, which offer the advantages of low cost, miniaturisation and RF performance, but have less integration capability.
Power amplifiers are especially designed as modules. Some solutions also integrate the power amplifier with the front-end antenna switches in the module.
The main interconnect technology used for RF parts is wire bonding and it is expected that this technology will still be important for the future up to 5 GHz. Flip chip is used for some more complex SiP set-ups. A clear trend for transceiver is increasing integration of passives. Here passives integrated in Si substrates offer interesting solutions.

A challenge for the RF part is the ongoing increase of complexity. Thus, for the future new package approaches are required. A promising new solution could be a thin film technology which allows reduction of complexity by appropriate rerouting. Embedded wafer level ball grid array solutions based on reconfigured wafers and thin film technologies are a promising example for future complex RF devices in various frequency ranges. They allow integration of passive components and open interesting possibilities for combining baseband and RF parts. For the future with increasing Si technology

performance also software radio based architectures are discussed which require appropriate package solutions.

RF CMOS and CMOS based technologies like SiGe or CMOS on SOI substrates meanwhile are investigated up to 100 GHz region and even beyond. Regions for investigations are automotive radar in the 24 and 77 - 81 GHz region. For these high frequencies packaging is extremely difficult: The most important challenges are

- material constraints (high frequency data for many of the new materials are not available)
- heat dissipation (~ 3W/mm^2 needs to be removed)
- shielding
- transmission lines (coplanar or micro strip lines)
- crosstalk

These high frequencies packaging technologies involving thin film are highly attractive because of their capability for transmission line design. At frequency beyond 40 GHz integration of antennas to the package becomes very attractive. An integrated SiP based solution has the advantage that the internal transmission lines need not be adjusted to 50 Ohm, which allows performance improvement.

10.5 Medical and Bio Chip Packaging

The requirements of medical electronics are often best met with SiP solutions. This is particularly true for implantable and wearable devices such as biosensors, hearing aids, pacemakers, implantable cardioverter defibrillators and similar products. Additional implantable electronic and electromechanical systems are being developed and qualified at a rapid pace. The emerging applications range from drug delivery through integration of biomaterials with integrated circuits for neurostimulation. Future products will incorporate telemetry for real time data monitoring which incorporate RF circuitry and antenna structures that are biocompatible. The requirements for SiP based medical products are similar to those of SiP based products for other applications with two important exceptions. First the reliability required for medical SiP based products is at the highest possible level since a failure may be fatal for the user. Second the environmental requirements of the package have to include exposure to body fluids.

There are several areas where additional development is needed for medical SiP. Among those are:

- Low power, biocompatible radios with a signal that can reliably penetrate the human body and package to reach a remote receiver. This receiver is most likely worn by the user.

- Reduced power consumption through improved interconnect

- Power scavenging from the user's body temperature (up to 30 micro Watts/cm2) or motion (up to 10 micro Watts/cm2) to extend battery life of implantable products. This will require research and development of biocompatible MEMS SiP components

- Biological and silicon integration such as neurons grown on silicon. This allows silicon to monitor brain waves to detect seizures and provide counteracting neurostimulus.
- Reliable interoperability of wireless telemetry for medical devices in a world where RF devices operating across a number of frequencies have become ubiquitous.

One common method used in biomedical devices is to illuminate a sample with a suitable light source, then look for the presence, absence or difference in intensity between two or more wavelengths with photodetectors that may require narrow band optical filters.

Many of the biomedical devices incorporating this sensor concept are disposable products made to detect pregnancy, glucose levels, blood oxygen levels, CO or NOx levels in the air, etc. Thus, they must be rugged, small, required minimal amounts of power to operate on batteries and be manufactured for low cost.

The packaging issues with these products are:

1. Mechanical design, especially of the optical elements, to
    a. ensure optical alignment is achieved initially
    b. ensure alignment is retained for the life of the product
    c. protect the optical chain integrity over the lifetime of the device
2. Materials selection, especially adhesives
3. Protection of the optical system and related electronics from external light and EMI effects
4. Protection of the device from the environment including from fluids that are either samples to be evaluated or used in the detection process.
5. MicroTAS (Total Analytic Systems; lab on chip)
6. Chemical sensors (gas and liquid)

11. Operating Environment Specification

SiP architectures are now penetrating an increasing variety of operating environments beyond the normal operating environments typical for single chip packages in computers and consumer devices. Medical SiP have no challenges associated with temperature but they must be compatible with the corrosive body fluids encountered in vivo applications. One of the most demanding environments is for automotive SiP. The current specification for automotive is given below.

Operating Environment Specification

Automotive max. Temperatures (Ambient Temperatures):

- **Passenger compartment**
  - Dashboard, panel + 85°C
  - hatrack, roof + 120°C
- **Chassis**
  - isolated areas + 85 °C
  - exposed to heat source + 125 °C
- **Transmission**
  - exposed to heat source + 125 °C
  - exposed to oil/hydraulics + 175 °C

(today always bare die on ceramic substrate)

- **Engine Compartment**
  - Moderate areas + 125 °C
  - Attached to Engine + 155 °C

(today always bare die on ceramic substrates)

Storage range: -55°C to 125 °C
Operating range: -40°C to 150°C

Typical Mission Profile

-40 to - 20°C	300h
-20 to + 20°C	600h
20 to +130°C	4000h
130 to + 140°C	1000h
+150°C	100h

Vibration: 40g / 10 - 1000Hz
Mechanical Shock: 50g / 11ms

In some cases the ambient operating temperature is projected to rise to 200 °C.

(See Assembly and Packaging section of the 2007 ITRS for detailed operating temperature forecast**)**

Components in a future smart power technology (as single components) for engine control or Chassis (exposed to heat source) will have an ambient temperature range from -40 to +150°C. These components will have embedded Flash, µC and LDMOS. This means that the LDMOS circuits add a temperature of about 20-40°C and as well the silicon as the package has to cover a temperature (Ambient + Power dissipation) of -40°C up to 165°C. (This is very critical for controllers and Flash => the Package heat dissipation has to be very good). In addition packages and silicon for such applications have to withstand thermal hot spots of 350 to 400°C.

Another example concerning future applications will be "automotive radar". In

the future all components will be integrated in a SiP. This means an ambient temperature range of 105°C and in addition heat from power dissipation of 10 to 20 Watt.

12. MEMS

MEMS devices have become mainstream element in many electronics systems today however device fabrication and packaging technologies for these devices are to a large degree still based on customized processes. As a result there are few standards yet established for device design, simulation, materials characterization, manufacturing processes, manufacturing tools, packaging technology, device testing, or product qualification. Many of these technology needs are further complicated by the diversity of device types present in production or under development which each have unique requirements.

Table 5: Package requirements

MEMS Device Type	Key Packaging Requirements
Pressure Sensors	Low cost integration of mechanical mounting an adapter for pipe; low stress interconnect is also important
Accelerometers	Low cost hermetic cavities
Chemical Sensors	Electrical and environmental connections
Magnetic Sensors	Non Magnetic packages materials
RF Switches, Oscillators, and filters	Low stress interconnect between MEMS device and package hermetic cavities and low electrical parasitic interconnect
Optical	Low cost optical transmission structures, hermetic cavities

The incorporation of MEMS devices into SiP is being driven from the bottom up as it becomes clear to MEMS designers that greater value is realized when logic and memory to handle MEMS control and data transfer are an integral part of the MEMS package. Both cost reduction and improved performance of MEMS devices may be realized through integration of MEMS devices into an SiP with standard semiconductor devices which provide drive, control, and signal processing functions. At the same time complex SiPs are incorporating MEMS for pressure sensing, relays, accelerometers and other functions required for a system. More detail of the development of MEMS packaging can be found in the 2007 ITRS. Some MEMS devices that will add value in SiP require development before they are fully compatible with the constraints associated with SiP architectures. These include fluidics, bio sensors/devices and certain optical components for example. Many of these will require cavity packaging and may be incorporated as PiP or PoP structures into SiP products.

13. Chip-Package-System Co-design

Mario A. Bolanos, Darvin Edwards, Gary Morrison, Hongwei Liang
Texas Instruments Inc.
Hosack, Harold, SRC
HeeSoo Lee, Marc Petersen, Agilent Technologies
Manoj Nagulapally, Chetan Desai, Fluent Inc.
Lawrence Williams
Ansoft Corp.

13.1. Introduction

There is a need to identify, develop and support Chip-Package-System Co-design tools and methods to provide better chip-package-PCB design collaboration and to reduce development time for system-in-package solutions (i.e. side by side configurations and 3D packaging, which includes stacked die, package on package, die stacking by TSV, and also embedded die passive configurations). Both system in package (SiP) and system on chip (SoC) are growing very fast to support the era of pervasive Communications.

SoC's for example, include integration of digital cores, custom logic, memory and analog on a single chip. This leads to complex requirements for ensuring signal integrity of critical nets and adequate power distribution simultaneously in both the chip and the package.

System memory requirements are also exploding in some applications, for example average system memory in 2G cell phone is 10MB or 80Mb. In 2.5G/3G this is exploding to even larger memory requirements. The same is true for many other applications. This has spawned the SiP (especially stacked die or stacked package PoP) as a solution that meets the cost, time to market, foot print and flexibility goals of these applications.

A Chip-Package-System Co-Design Methodology is a vital enabler for effective SiP packaging of system-on-chip (SoC) designs. Implementing a co-design methodology requires iterative design reviews and collaboration between chip design, application development, electrical, thermal and mechanical modeling, simulation and high-density substrate design teams.

Some key challenges in SiP packaging are Design for Manufacturability, Design for Low Cost, reducing iteration time, complex wire bond rules/checking, chip design flexibility trade-offs, and interface/alignment with tools and flows such as those provided by EDA design software tools, IDM specific design flow and tools, and with substrate suppliers and assembly sites.

13.2. The Challenge

Silicon integration of system-on-chip (SoC) designs presents a formidable challenge, but the complexities expand when packaging these devices in complex SiP.

Integrating SoCs into SiPs, without sacrificing performance, cost or cycle time, demands a shift from traditional package design methods and tools to a systems design approach – also known as chip-package co-design. The typical SoC package designer wrestles with many new challenges compared to the previous generation of IC package designs. Some of these new complications include the following:

- Comprehending the interaction and IO planning of multiple functions on a single chip and package
- Handling of an order of magnitude more design data
- Minor tweaks in the IC or package design can lead to additional levels of design work
- The need for tighter integration of chip IO planning, system-level reliability and manufacturability testing, as well as system-level electrical, thermal and mechanical modeling add reliability here as well
- The learning curve associated with using new, more powerful package design tools

Design changes that originate from many different functional areas are usually beyond the control of the package designer. As a result, package designers end up applying these changes in piecemeal fashion.

13.3. Cost and Time to Market

Without the benefit of the extraordinary collaboration within the design team, the package is almost impossible to optimize at the system level. The cost trade-offs are not clear, system level performance impacts are uncertain, and changes are cumbersome to fan-out. To avoid this, designers often use overly conservative design margins and assumptions which lead to higher package costs. Also, without co-design analysis tools that function across design environments, “What-If” analyses are difficult and time-consuming which leads to longer design cycle times.

13.4. Need for a Systematic Approach

Package design requirements and changes originate from many different functional areas and usually end up being applied piecemeal. To help stave off this piecemeal approach, the chip-package co-design borrows methods and tools from modern systems design.

This approach can head off constant iteration and other challenges. One way

to reduce iterations is to use “look-ahead” test and modeling vehicles to support system-level reliability and manufacturability testing, as well as system-level electrical and thermal modeling.

Look-ahead vehicles come in two forms: an actual mechanical vehicle for reliability and manufacturability testing, and a paper design vehicle for feasibility and electrical modeling analysis. These vehicles require a certain discipline and commitment.

Once they are part of the standard co-design flow they allow new product teams to get a head start on package design and analysis despite numerous minor changes that accompany complex designs. This approach helps answer many general design questions early in the process, and at a fraction of the cost of using production test vehicles.

13.5 Design for Reliability: Impact on SiP

Effective co-design should comprehend the interaction between physical, thermal, mechanical, electrical design and reliability. Many of the trade-offs between design areas and reliability that are evident in conventional packaging, become complex and harder to recognize in SiP configurations. So it is not good practice, especially in SiPs, to keep the electrical, mechanical, and thermal and reliability portions of the design habitually separated.

For example, in package electrical design, we can easily recognize why too little space between signal lines could give improved routability but reduce reliability, since contamination or particles may become more likely to bridge the shorter distance between traces. However, it may be less obvious that too much space between signal lines might reduce reliability as well – by creating an unbalanced copper density between layers, resulting in thermo-mechanical stress.

Understanding and investigation of interfaces, which become more complex in SiP, are key prerequisite for Design for Reliability. Of special importance is the knowledge of the material data. Because of the complexity of sub-component interactions, there is not a universal or specific list of design for reliability design parameters. In general, one needs to examine the sub-component interactions, design goals, trade-offs, design rules, specifications and existing design for reliability practices in order to select the appropriate design for reliability guidelines. One can examine SiP reliability interactions and predictions with tools such as test chips and modeling. Test chips and packages, for example, allow one to simultaneously evaluate many different areas of reliability:

- Bond integrity
- Materials
- Dielectrics
- Metallurgy
- Die and package size limits
- Modeling validation
    - Thermal impedance
    - Component level reliability

- Fail location
- Design rules
- Electro-migration
- Processes, settings
- Board level reliability
- Temperature cycling
- Drop testing
  - Bending

Although SiP design for reliability is more complex than that of conventional packaging, the co-design process can augment design for reliability in SiPs by creating or identifying extra design margins that might be adapted to improve the overall reliability of the design.

13.6. The Need for Co-Design Tool Development

SoC and SiP package design requires 3D capable thermal, electrical and mechanical modeling tools that are capable of integrating and analyzing chip, package and system level requirements and inter-actions. We also need Electronic Design Automation (EDA) tools for powerful chip-package-system design and routing capability, built-in checks, standards and reporting features like Design Rule Checks (DRC), standard net list syntax, and connectivity reports.

Custom automation tools can provide fast and efficient communication and verification of design data between different design environments. Spreadsheets are a common platform for these automation tools since they are available in almost all design environments and readily scale to handle large volumes of data. These tools have three primary uses: 1) convert data to pictures, 2) convert data to standard formats, and 3) compare the standard format datasets. This type of automation is essential on typical SoC designs to reduce the time spent manipulating relatively large datasets, and to reduce possible manual errors in handling large amounts of raw data.

The development of chip-package co-design methods and tools is an ongoing process. A comprehensive, user-friendly, and tightly integrated tool(s) that can seamlessly span all the different design environments might not be available yet. Nevertheless, existing chip-package co-design tools, with the right methodology and custom-developed internal tools can provide crucial benefits. These tools allow advanced package designers to meet essential SoC and SiP performance requirements, reduce advanced package costs, and considerably cut design cycle time and verification time.

13.7. Chip-Package-System Mechanical/Stress Modeling and Design Challenges

Areas of stress modeling concern:

- Board Level Reliability (BLR): all tests (BLR-TC, BLR-Bend, BLR-Drop)
- Internal package stresses
- Chip-package interaction (include on-chip metal layers and low-k ILD)

Modeling limitations:

- Stacked package increases model complexity, mesh density, etc.
    - Longer run times, especially through dynamic drop test modeling
    - Longer set-up times initially until macros developed

- Structure will dictate need for new material property inclusions such as cure shrinkage. Need to study packaging process steps to fully realize die stress and warpage.

- There are many new problems and / or failure mechanisms that need to be simulated in order to be able to predict SiP packaging reliability. Some of these issues are listed below:

- SiP (Stacked Die Package, Stacked Package) BLR Impact
    - If die stack and / or stacked package makes package more rigid, BLR-TC, BLR-Bend, and BLR-Drop likely worsen
        - Rigidity can be reduced with lower modulus die attach adhesives, low modulus spacers, lower modulus mold compounds
        - Material sensitivity studies are needed
        - Die size has impact
    - If package becomes heavier (higher Si % volume), BLR-Drop will suffer
        - Silicon density is 1.3x typical mold compound
    - More Si volume in package will reduce effective CTE, worsening BLR-TC
        - Thinner Si on bottom with low modulus connect to upper die may offset the concern
    - Very complex dynamic system for BLR-Drop
        - Vibrational resonances may occur between packages
        - Package “bouncing” and interference possible
        - Solder balls at bottom of stack bear brunt of extra weight from packages above (BLR-Drop)
        - Overall structure may be less rigid, offsetting weight issues
    - Differing sized die in package stack will modulate CTE of each package, resulting in possible inter stack solder fatigue on BLR-TC
        - BLR-TC for the bottom package will also degrade compared to single package

- Cantilevered die provide for complex stress distribution inside package
    - Spacer, spacer adhesive, and mold compound have different expansions and cure shrinkage
        - Large warping of die
        - Corner stress effects applied to die circuitry: High potential for parametric shifts and for die cracking

- Parametric shift risks
    - Stress gradients on die surface give rise to parametric shift concerns

  - High sensitivity analog components should be on top-most die or near center of dies lower in stack for more uniform stress gradients
    - Sensitive balanced circuits must avoid corners and edges of die OR spacer above them

- Moisture sensitivity
  - If die attaches, spacer attaches, or spacers absorb moisture, package moisture level may be degraded

- Internal package delamination risks
  - Many more interfaces in package give rise to risk of many more internal delamination regions
    - Detecting delamination within the stack is very difficult

- Package substrate cracking risks
  - Die stacking introduces higher stress and warpage to the package substrate
    - Risk of substrate mask and copper trace cracking is higher

13.8. Chip-Package-System Electrical Modeling and Design Challenges

Technology scaling leads to higher switching speeds, greater package pin count, lower supply voltages with associated narrow noise margins, and greater demands on power supply integrity. Greater reliance on high-performance packaging solutions including BGA, flip-chip, and system-in-package (SiP) methods are used to meet some of the demanding performance goals. Design challenges are observed at the IC die, package, and board levels and verification of an electronic system requires thorough consideration of the effects across these design disciplines.

- Coupling in high density and multiple-loop wire bonding

  In stacked die package, the coupling and crosstalk effects between wire bonds could be severe. As 3D packages relentless pursue thinner dies for a smaller module thickness, the various layers of wire bonds will get closer. This will make the coupling between wire bonds more severe. This is a new coupling scheme not seen by single die package.

  The bonding pad space will get smaller, causing coupling between two adjacent wires to be strong. The wires for the top dies may be longer, causing larger parasitic inductance. All these coupling are more severe as clock rate gets higher.

- Electrical modeling tools need to improved to incorporate all possible interconnect schemes in an SiP (3D and side by side)

Mixed flip chip and wire bond interconnects in 3D packages. Ability to model very complex wire bond loop profiles in stacked die packages. For example, a simple stacked die package with 3 die, there can be 5 or even 6 wire bonding layers: top die to substrate; middle die to substrate, bottom die to substrate; and 2 or 3 wire bond layers for die to die communication. More dies in stacked die package will have more wire layers.

The package database importation is difficult. More importantly, the modeling accuracy is critical. The Jedec 4-point representation for wire bonds, which is popular and works well for single die package, may be too simple for many situations in stacked die package because it could cause wire bonds shorting and crossing in the model.

The industry may require a more rigorous implementation of wire bond loop profile in modeling tools. Tools are expected to be able to assign more realistic profiles to wire bonds.

- EMC issue

  Taking full advantage of in shrinking size and voltage provided by the nanometer silicon technology, the memory technology is advancing quickly. DDR3 is the first memory technology that breaks the 1Gb/s limit. It now runs at 1.6Gb/s for some server and high end graphics applications. The future cell phones and personal entertainment devices will have more memory-hunger functions such as videoing, which inevitably demands a faster memory access. As a result, in stacked die packages for these applications, the memory technology will have to keep pace with the demand in speed. The memory speed in the stacked die package will likely reach 1Gb/s level in a few years. The current DDR3 uses a single ended data transmission, which is known to be not as robust in EMC aspect as differential signaling. At gigabit per second speed, the question of EMC issues such as radiation will consequently be raised by both designers and customers.

  The EMC issue will be more obvious when the RF functions are integrated in the SiP or 3D packages with these fast single ended memories.

- Bond wire modeling is now true 3D

  This means we need to have accurate bond wire profiles included in the modeling. This is similar to staggered pitch with multiple landing layer cavity packages. We need to consider as well the Silicon Die Effects and Die to Die Coupling.

  Strong parasitic capacitance to interposer materials used in SiP is an important consideration if significantly different than the mold compound material of the package; coupling through bond wires is stronger.

Vss/Vdd Noise Reduction is more difficult for the topmost die of the package design.

- General requirements:

  - Communication across different design environments is essential
  - Interactive and fast (not batch) analysis of current substrate design iteration within package design EDA tools is needed.
  - True 3D simulation capability is required.
  - Capabilities to model cross talk, coupling, inductance, power distribution networks, IR drop, shielding, SSO,
  - Eye-diagram simulation capability is a requirement
  - The models should comprehend the bond wires in the analysis (stacked wires, die to die wires, etc.)
  - Visualization of noise/hot spots is needed (for substrate designers)
  - Accurate SPICE models are needed.
  - A function that reads substrate IBIS models is desired
  - Tools that handle S-parameters in time-domain are needed
  - Simulate chip plus package plus board together is a must
  - Common pass/fail criteria is desirable

13.9. Chip-Package-System Thermal Modeling and Design Challenges

In many systems, 80-95% of power is dissipated by the PCB, not by the package. To enhance the thermal performance of the package, the design must maximize thermal conduction to the system heat sink. This will vary with system type and in some systems it may be represented by the PCB.

Thermal conductivity of metal is ~400x that of plastics, while the thermal conductivity of silicon is ~120x that of plastics, therefore, the package thermal performance is enhanced by having direct thermal conduction paths through the Si and Cu of the package. If a polymer gap is required, it must be thin and have a large area to avoid impeding the heat flow

To optimize SiP (stacked packages) thermal performance, thermal conduction through the stack must be maintained.

- The top packages will not conduct heat as effectively into the PCB
- Their thermal performance will be degraded
- Thermal balls are not possible for top packages
- Adhesive between packages would provide some relief
- The thermal performance of the bottom most package will look largely the same as in a single package case if we assume little thermal input from the top packages
- The best system design is to put high power die in bottom package for best thermal conduction into PCB

- Thermal performance of stacked packages will be somewhat worse than for a stacked die approach with the same die compliment

The system problem is that stacking packages results in higher power density on the PCB than single die package. Since the PCB must dissipate most of the heat, this means the die complement will run hotter in a stacked configuration than it would if it were spread out on the PCB. Hotter junction temperatures will be a show stopper for certain stacking options. System thermal enhancements will be needed to increase PCB thermal conductivity; they will add cost if not optimized.

It is important to consider providing other means to conduct heat to a sinking source close to the high power density part, such as:

- Screw, glue, or thermal interface material to chassis which further conducts/convects/radiates into environment
- Use heat pipe to move heat to some heat sinking location
- Use micro fans with vents
- Use pressure fit plates to spread heat to PCB

13.10. Generic Chip-Package-System Co-Design Tool Development Requirements

- Improve design cycle time, accuracy and design-for-manufacturability.
- Align with critical tools, flows and rules such as: IDM's internal tools die design tools, suppliers, assembly sites, electrical constraints and modeling tools.
- Reduce iterations, less manual/more automated checking, capture complex design rules and enable more chip-package-PCB trade-off capabilities.
- Forward-looking: better methods to handle increasing complexity, collaboration, and technology combinations.
- Easier verification. Substrate, substrate plus die, manufacturability, electrical, functional, thermal and mechanical verification. Import/Export data to IDM's internal tools.
- Easier rapid feasibility analysis.
- Collaboration with die design team. Good data formats, chip plus package plus PCB verification tools, etc.
- Comprehend the interaction and IO planning of multiple functions within a single package (also passives).
- Great complexity – amount of design data, multiple layers, elaborate patterns, multiple net lists.
- Complicated electrical constraints (long traces/wires, crossing traces/wires…). Enhanced Constrain Management.
- Allow minor tweaks in IC or package design without leading to significant cycle time hit.
- Need faster design iterations in early phase to avoid more costly design iterations in the later phase

- Capture complex mechanical, wire bond and assembly-rule constraints driven by smaller and thinner packages.
- Better design for manufacturability and cost analysis. More and easier to use manufacturability constraints
- Real-time Chip-Package-PCB design trade-offs.
- Interface and alignment with internal tools and flows.
- Shortening design cycle of complex designs
- Cost-weighting of constraints
- More flexibility to handle frequent design changes
- Tighter integration with chip, PCB and manufacturability design teams across the globe
- System-level electrical modeling, including high-speed applications.
- Complexity drives verification tools that work across different design environments
- Tight collaboration with suppliers, support, development, production and customers to enable better methods and tools for complex package co-design.
- More powerful user-friendly scripting capabilities.
- Common, technology independent data base to facilitate reuse

13.11. Proposed Chip-Package-System Co-design Methodologies and Tools

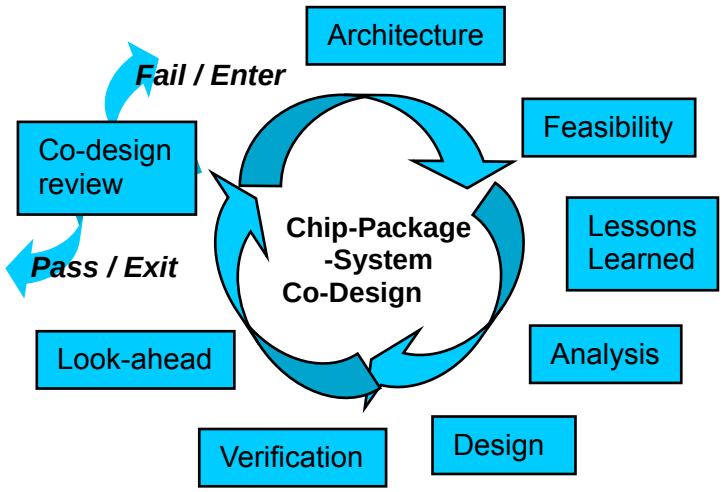

Figure 16: Co-Design cycle

Multiple tools
Electronic Design Automation (EDA) tool. Electrical modeling tools for signal integrity and power analysis. Separate architecture and verification tools.

Collaboration
Expert users of each tool collaborate to optimize the design with the help of custom interface utilities. Co-design could also improve performance while reducing costs and cycle time dramatically – often by 2x.

13.12. A Future Vision of Chip-Package-System Co-Design

- **One Tool.** Simultaneous design enabled by a multi-user, cross-functional EDA + system analysis + knowledge-based tool.

- **Wizard-like interface.** Automatically constructs baseline design for each component based on series of user questions, what if's, analysis and expert system for technology selection and design rules.

13.13. Stress/Mechanical Modeling and Design Co-Design Solutions

The challenges in chip-package-system Stress/Mechanical Modeling and Design were described earlier in Section 4. These challenges are very broad ranging, They include several new challenges due to uncharacterized mechanical properties of novel Cu-low k materials and material interfaces, difficult thermal environments brought on by porous dielectric materials both on-chip and off-chip, and electrical current induced extrusion and cavitation impact of Cu metallization on the stress/mechanical features of the system.

The challenges in stress/mechanical modeling also include those that are particularly important to the increasingly prevalent area of hand held devices-rapid thermal cycling, high moisture environments and drop-induced mechanical shock conditions.

In the 3D SiP case, these challenges are noted to be even more severe than in single layer devices due to the need to include the impact of features such as very thin chips, bonding layers and redistribution layers between chips, and more complicated stress behavior in multiple stacked chips and stacked packages. All of the challenges noted in Section 6 are expected to become even more severe as nanotechnology materials and structures begin to be introduced into IC components.

Stress and Mechanical Modeling has not been emphasized enough in the past. It is a pity that even today there is no single good EDA tool in this field even after more than 5 decades of the introduction of the first IC.

The stress modeling should address the following important issues 1) design for reliability, 2) design for yield (the example outputs are IC design rules and package design rules), and 3) design for cost effectiveness (use the cheapest material available to achieve the reliability requirement).

In the past, the material and mechanical design of IC and package had relatively large margin since stresses were well below the limits, therefore the stress modeling is used only after failure is found. However, a lot of factors (such as constant cost-reduction pressure, new materials replacing old materials, constant form factor-reduction pressure, SiP including 3D packaging, etc.) have already driven the stress modeling design margin to the limits. The

industry feels the urgent need of EDA tool vendors to address the stress modeling issue immediately.

There are currently several partial solutions to the stress/mechanical Co-design Modeling and Design challenges. For example, various electrical design companies[1] offer logical, physical, and electrical design systems at the SiP level (including 3D) including connection of a signal, its associated return path, and the power delivery system.

However, these systems do not couple to a stress/mechanical modeling capability. Other mechanical modeling providers[2] feature chip/package stress/mechanical co-design that includes thermal-mechanical analysis including such effects as thermal resistance and thermally induced stress. In addition, these systems provide analysis of solder joint fatigue, package warpage, and other mechanical stresses. However these capability do not generally have models for the critical on-chip features of Cu-low k interconnect, are often not easy to use in 3D implementations, and do not tie into the electrical modeling systems to allow for chip-package-system co-design.

To provide a complete solution to the chip/package/system co-design problem for stress/mechanical modeling and design a cooperative effort among the university community, CAD system vendors, and the IC manufacturing and Assembly and Packaging communities will be needed. The university community will play a key role in this effort. Their primary needed contributions are: developing numerical capabilities for rapid, accurate solutions to the multi-scale, multi-phenomenon modeling needed to simulate chip/package and system level reliability; identifying new materials and researching their properties, including in-process issues such as shrinkage, CTE, moisture sensitivity and adhesion; and in developing models and associated metrology techniques applicable to full characterization of the new materials.

Activities of this type are already occurring at various universities[3,4,5]. However, the issues associated with increased mesh densities, very complex structures, and new materials in SiP applications are very needing of added emphasis.
In general, the universities have been responsive to developing new modeling methodologies to speed analysis. The major gap has been with the EDA tool vendors picking up these new techniques and incorporating them in their tools.

The EDA tool vendors have not seen any need to provide more automation in their tools since the SC industry is small compared to other customers such as automotive and aerospace. The SC industry needs are somewhat unique in that our structures are different from those of either automotive or aerospace as our structures are unique.

University research without strong interaction with EDA tool vendors will likely not be implemented by the member companies.

The EDA vendors also play a significant role in the implementation of stress/mechanical modeling for chip/package/system co-design. Their key role is to incorporate advances in numerical techniques and models into combined chip/package/system co-design tools, and provide the user friendly front-end to make effective use of these tool capabilities.

This activity is particularly challenging in the chip/package/system co-design case because it will require EDA vendors to extend their breadth across both mechanical and electrical disciplines. Such activities are currently being accomplished at some EDA vendors[6], however significant further work will need to be completed to produce a co-design environment.

The IC manufacturers and A&P communities also play a key role in this effort. Their primary function is to be the driver for development of the co-design capability. In doing this, their primary activities are to clearly define the needs going forward and the specific constraints being placed on the stress/mechanical portion of the co-design system, and to provide data for calibration of model parameters and validation of the entire modeling and simulation system[7].

The IC manufacturers and A&P community will also need to provide funding for much of the co-design development through individual company contracts with the universities and EDA vendors, as well as through consortia activities such as SRC and SEMATECH.

Sources

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13.14. Thermal chip-package-system Co-design Solutions

The thermal dissipation challenges that we see today with single-chip components (smaller size, increased functionality, higher power) will only get magnified as the SiP design approach goes mainstream. Tighter integration with layout tools, flexibility in handling various SiP technologies, design scenario testing and addressing the length-scale problem by using advanced solver technologies and devising new compact modeling techniques are the

key challenges that need to be tackled. Therefore semiconductor companies need to be equipped with a robust analysis environment to accurately predict thermal performance.

Tighter integration with layout tools

Traditionally, thermal analysts for chip-package structures have preferred to abstract the details of package substrate entities (traces, planes, vias, bond wires etc.), primarily due to the lack of integration with EDA layout tools and also due to the computational penalty associated with including these details. Engineers generally rely on an “equivalent copper content” and “equivalent thermal resistance network” approach to try and capture the disparate thermal properties of various materials and components in an IC package design.

While this approach may be acceptable now in single-die components with a wealth of reference data, it is quite obvious that such an “approximate” approach could be dangerous and lead to significant inaccuracies in newer SiP structures. Moreover, for analysis tools to support a co-design environment, such assumptions cannot lead to meaningful feedback to design engineers who are trying to quantify the impact of their design decisions on overall thermal margins.

Next-generation analysis tools for SiP analysis will need to increase the fidelity of the IC package thermal modeling approach. Capturing the package design details from EDA layout tools will be the key to accurate thermal modeling of these complex SiP structures. Seamless integration of analysis tools and EDA layout tools will be more or less mandatory. Furthermore, depending on the SiP design, the data source may not reside within one design team e.g. in a PoP structure, the layout for the memory chip may not be owned by the same team that does the final integrated product. In this situation, analysis tools have to import data from multiple sources and provide an efficient mechanism to model the combined assembly.

Flexibility in handling various SiP technologies

Going forward, thermal analysis tools that can perform detailed thermal analysis inclusive of IC package substrates, traces, vias, non-uniform heat generation, wire bonds, and solder balls will be mandatory. Tools should provide complete flexibility in modeling the different SiP technologies (multi-die designs, stacked packages, combination of flipchip and bond wire designs etc.). Further, the tools should directly handle every degree of detail and all types of emerging packages thus eliminating expensive, manual, and time consuming procedures used in conventional design flows.

Design scenario testing

Accurate prediction of key thermal conduction paths and spreading mechanisms is of paramount importance in the design of SiPs, especially stacked-die packages. Package designers need reliable and fast answers to

what-if scenarios and optimization of several design problems if any thermal enhancements need to be cost-effective. Hence thermal simulation tools must be able to efficiently handle issues like parameterization and mathematical design optimization. Rapid setup and solution of various design scenarios and optimization problems aids the design process immensely and reduces cycle times.

Tackling the length-scale problem

The complexity in modeling SiP structures results from the presence of disparate length scales ranging from the sub-micron level to the millimeter level. The necessity of resolving these scales for accurate thermal modeling of these structures renders the computational problem intractable. As thermal simulations increasingly become part of the tools in the overall design process of SiPs, addressing the length-scale problem remains a key challenge in making the simulation tools more effective in the design cycle.

The presence of highly non-symmetric heat transfer paths in SiP components like substrates necessitates the need to model many details like local metal contents and via details. Using traditional lumped-parameter methods will lead to huge errors in temperature and heat flow predictions. Detailed handling of the small-scale structures in SiPs leads to a tremendous increase in the computational mesh sizes.

New solver technologies like non-conformal meshing and the use of automatic three dimensional conductivity maps can circumvent the above difficulties and make accurate thermal simulations of SiPs possible. Thermal tools need to incorporate these technologies if they are to be incorporated in the SiP design cycle.

Compact Modeling of SiPs in systems

While semiconductor companies are primarily concerned with meeting reference metrics (theta-ja, theta-jb, theta-jc), the package has to ultimately function in a complete system. Traditionally compact representations of IC packages involve the use of thermal resistance networks. In these approaches, the complex mechanical structure of IC packages is reduced to a thermal network of a fixed number of computational nodes connected by thermal resistors. The thermal network represents the behavior of package internal thermal conduction, while the fluid flow in electronic systems is predicted using conventional CFD. These approaches reduce grid size and the computational complexity, increasing the turnaround time and allowing CFD to be used in system design cycles. The present multi-resistor network modeling approach proposed by the DELPHI consortium can only handle single die packages. The future modeling of SiPs in system level CFD simulations will necessitate the development of such compact models for multi-die packages. Alternate technologies like ACE (Automatic Compact model Extraction) that allow for automatic generation of network topologies and refinement of the compact models to the degree desired by the user need to be explored for this purpose.

13.15. Electrical Chip-Package-System Co-design Solutions

A chip-package-system co-design methodology is a key enabler of system in package (SiP) designs. This methodology requires simulation at the IC die, package, and board levels. The foundation is the ability to model the inherent 3D nature of SiP packaging hence electrical modeling must be built upon an accurate solution for 3D model extraction.

The trends that engineers designing high-performance systems need to perform design and verification with consideration of the package, board, and circuit together are explored, including focuses on signal integrity, power delivery, and electromagnetic radiation.

Simulation and Modeling of Packages and Interconnects

Excellent package and interconnect performance is a crucial factor for successful high speed and wider bandwidth system design since lower electrical performance of packages and interconnects may degrade the entire system performance, especially with faster chips' edge rates. Having said that, accurate characterization and modeling of packages and interconnects is a critical design step in a modern SiP design flow. In other words, a good package design with accurate characterization and modeling must be a part of chip-package co-design methodology.

A different packaging technology may lead to a different interconnect technology. For example, traditional and low cost plastic packages mostly use bond wires as the standard method of connecting the chip to the package or substrate. However the high impedance of the bond wires causes inductive discontinuities which result in impedance mismatches and unwanted reflections. Flip-chip technology adopts solder bumps for the chip-to-package or substrate interconnect so that the inductance associated with the chip-to-package connection can be significantly reduced. Depending on the application, required frequency performance, and cost of the design, a proper selection for packages and interconnects should be made. In order to get more accurate models of these packages and interconnects, generally full 3D EM simulations are required to take account of 3-dimensional effects such as the curvature of the bond wires, cavity effect, as well as the interaction with ground planes and other substrates.

The increasing number of I/Os and decreasing pad pitches with the semiconductor technology advances have been difficult challenges to package designers. Optimizing complex interconnect routes while minimizing signal contamination is not an easy task. With mixing analog and digital functions into a single package and by stacking multiple dies into a 3D form, more complicated problems to deal with are anticipated. Also a larger ground loop inductance due to 3D stack-up of dies and longer routing path as well as increased coupling between smaller pad pitches may make even hard to

achieve the required system's performance. EM solvers can characterize and model these in a form of S-parameters or visualizing electric or magnetic field plots. No matter what form of data is used, it is always necessary to analyze and optimize their performance with other part of circuits or systems combined together.

These are all challenging opportunities for package/circuit/system designers. All different kinds of commercially available design tools can facilitate this challenging design tasks. However no single tool provides a complete solution yet and continuing efforts have been being made to improve the performance of tools and design flows by EDA vendors.

Full Wave 3D Solvers

Extraction of electrical models for a complex SiP design with 3D nature of the wire bonds is best performed using 3D electromagnetic (EM) field simulation software. A wide variety of commercial EM extraction tools exist, some provide 2D solutions for planar structures and/or for uniform transmission lines, others provide full 3D solutions with a broad offering of materials and modeling capabilities. The 3D simulators can be further divided into static field simulators and full-wave field simulators. Static field simulators solve Poisson's Equation for the electric field E and the magnetic field H separately to examine capacitive and inductive effects, respectively. Because E and H are decoupled, a static field solver is best applied to structures that are small compared to wavelength (λ/10 where λ is the smallest wavelength of the frequency of interest). In electrically small structures there are no significant transmission line or field radiation effects and hence decoupled E and H fields are appropriate. The static solvers are very useful because they can rapidly extract low-frequency lumped element models for complex 3D packages including EM coupled bond wires and package routing. Most commercial static simulators can generate SPICE equivalent circuit models with capacitive and inductive cross coupling among all conductors in the 3D package. These SPICE models can be used immediately in chip-package circuit SPICE simulations.

Full-wave 3D field simulators solve the Wave Equation derived from Maxwell's Equations with E and H fully coupled and valid to the highest frequencies. Because E and H are fully coupled, a full-wave solver is best applied to structures that are large compared to wavelength (typically larger than λ/10 where λ is the smallest wavelength of the frequency of interest). All high-frequency behavior such as transmission line, skin depth, and radiation effects are included in the simulation. Most commercial full-wave field simulators natively export frequency-dependent S-parameter models for the interconnect with user-selected reporting of single-ended, differential, or multi-mode data. Although traditional SPICE simulators do not handle S-parameter data directly, there are modern SPICE simulators that are able to handle full-wave S-parameters in the time- and frequency-domains by creating compact models based on pole-zero and/or state-space modeling. EM field plots in the near- and far-field can be computed and plotted to gain a

comprehensive understanding of radiation behavior.

EMC Radiation

Energy from excited traces couple to neighboring planes and subsequent radiation can occur due to excited parallel plate modes between power and ground planes and/or the electric currents on traces exposed on the top or bottom layers. Typically parallel plate modes are the dominant source of radiation. Simulations are usually performed using the full-wave simulator across a wide frequency band. Calculated fields for each frequency were stored and then used as the source for additional 3D FEM solution to calculate radiated emissions for the board when placed within a conducting enclosure.

13.16 RF Chip-Package-System Co-design Solutions

With ever increasing frequencies in RF applications, package pin counts and densities have put more pressure on the development of an effective chip-package co-design methodology because a package's lower electrical performance combined with a chip's faster edge rate may degrade the entire system performance.

In addition, the technology trend towards integration of embedded passive devices (EP) and integrated passive devices (IPD) in the packages requires extensive characterization and modeling of those components with electro-magnetic simulations beforehand due to the difficulties of testing and measuring these structures.

Co-simulation of RF, Analog/Mixed Signal, DSP, EM, and Digital

SiPs that combine all of the functions, RF, analog/mixed signal, DSP, EM, and digital bring not only design and manufacturing challenges but also simulation challenges. Usually a different function of ICs requires different simulation technology. For instance, frequency domain simulations such as Harmonic Balance are adequate simulation technologies for RF circuit designs especially frequency translation circuitries, whereas time domain simulations are typically good choice for digital applications. Since the trend toward to the convergence of computers and communications and more high speed designs becomes a quite common transition in the market, the distinctive separation of them is obscure. Furthermore, the need to simulate the system that combines all different functions together such as RF, analog/mixed signal, digital, DSP and EM has significantly risen. This is because it is important to understand the system's behavior with packages and interconnect parasitics and also by adding embedded and integrated passives in SiP applications. Also the selection of either on-chip or off-chip components can be evaluated in this system design process.

Simulating all functions together is a quite challenging task for simulation tools even with the advances in modern simulation technologies. The data/signal

conversion during the simulation process from analog to digital and modulated signal and vice versa must be seamless, effective, and accurate such that convergence issues can be avoided and the simulation gets done without taking too long. The complexity of SiP has pushed the limit of simulation technologies beyond. Behavioral modeling became a very important aspect in addressing the simulation technology limits since it improves the simulation speed by relatively simplified representation of circuits and systems without losing much of the simulation accuracy.

Simulation and Modeling of Embedded Passives and Integrated Passive Devices

Integrated passive devices may be formed at several levels. Typically they will be used:

- On the redistribution layers of semiconductors.
- On the rerouting layer of a wafer level package using materials such as Ti, Cr for resistors, and Ta_2O_5 for capacitors.
- In the interconnect layers of the SiP substrate providing functions such as impedance matching networks, filters, balance-to-unbalance (balun) transformers, and directional couplers.

Embedded and integrated passives are used to replace traditional surface mount parts. They are seen as a key enabling technology in SiP designs, especially in RF systems. The substrate for embedded passives can take many different forms, from laminates to ceramics to polymers. The advantages of embedding passive components into substrates are cost reduction, reduced circuit size, and possible performance improvement.

Typical embedded passives are resistors, capacitors, and inductors that account for 80% of the total component count in mobile telephone applications. Embedded passives have been used to reduce the size of modules by 25% to 75%.[1] However the design trade-off in embedding passives into the substrate is the difficulty of tuning: there is almost no chance of tuning, characterizing, and measuring these devices due to the embedded nature of structures. In addition, the advantage coming from the flexibility of making almost any arbitrary value and structure with embedded passives makes simulation and modeling even harder.

Since these embedded and integrated passives are all physically structured components, it requires an electro-magnetic simulator to simulate and model these devices. With commercially available 3D planar or full-wave 3D EM (Electro-Magnetic) solvers, the simulation and modeling can be easily performed and the process consists of 3 steps, modeling, solving, and post-processing. The choice between 3D planar and full-wave 3D EM depends on different needs based on what applications are targeted. For example, if the structure contains cavities, then 3D EM might be a better choice since 3D planar can’t handle cavities well. EM simulators typically provide very accurate simulation results that may shorten the design cycle and reduce the cost of designs. However an EM simulation is quite a time consuming process unlike

circuit simulations. The simulation time depends on the size of the problem. With complicated structures, the number of meshes and unknowns may be quite large such that it requires a very long simulation time or possibly even unsolvable. Nevertheless this problem is somewhat relaxed with EM simulators moving from 32 bit to 64 bit technology that entirely remove the 2GB memory limit for the solvers, especially for PC platforms.

Due to the lengthy simulation time and difficulty of tweaking and tuning the components by EM simulators, building up a scalable model that can be used in circuit simulations is a very desirable solution to speed up the design cycle while achieving simulation speed and accuracy improvement. Simulation or measurement based scalable models can be generated to serve this purpose with commercially available design tools.

13.17. Conclusion

A chip-package Co-Design methodology is an essential component of effective SoCs integrated in SiP packaging. The alternatives to a system package co-design approach, at least in the case of SoC, could leave one well short of the goals of higher performance, lower cost, and faster cycle time. For example, the failure to identify and meet the essential system-level requirements, or to not apply lessons-learned, may result in lower-than-expected performance. Likewise, the absence of some way to quantify the design trade-offs, and the lack of some critical system-level analysis, may produce an overly conservative design more expensive than desired. Finally, incomplete feasibility studies and failure to capture some key interaction at the system level can result in extra iterations before the package design is finalized. Without the benefit of co-design, the net result is a device that is late to market with an expensive, overly conservative package. That predicament can knock a breakthrough product to its knees. Now who would want that?

References:

1] RF SiP: the Next Wave for Wireless System Integration -A.B.Smolders, N.J. Pulsford, P. Philippe, F. E. van Straten, 2004 IEEE RFIC Symposium Digest.

14. Application Specific Physical Architecture

SiP launched into the place where it was the only solution satisfying the system requirements. Its structures are diversifying afterward associated with the penetration into the consumer market and matured understanding of the advantages of SiP. Each system level application has led to the different physical architecture of SiP.

14.1 Hand-held Applications

Hand-held products are being miniaturized from the note-book size to passport, cell phone, or further miniaturized wearable sizes. They would be even embedded in a human body as a remote controller to enable instant commands to the external electronics devices or for medical purposes in the future. The demands for increasing functions and higher memory size have semiconductor devices stacked each other to save the real estate on PWB. Then, Known Good Die (KGD) problem has arisen due to the cumulative yield loss of packaged dice. Package on package (PoP) was developed to solve the problem by packaging separately and stacking them afterward. The trend of the increasing memory size has accelerated the deployment of PoP in the market. Smaller outline of the semiconductor package is regarded as an added value in the hand-held applications, and manufacturers kept developing new processes to make them thinner, smaller, and lighter. PoP packages, which are mainly used for stacking logic die (bottom) with memory die (top), have the advantage that a system manufacturer can easily implement a second source and can change memory suppliers without system redesign.

Even in hand-held applications, higher resolution images are preferred in pictures and videos; therefore, larger memory size and higher data transfer rate are required. PoP satisfies the larger memory size requirement but not the higher data transfer rate because of the detour of fan-out and fan-in paths between top and bottom packages. On the other hand, embedded DRAM meets the higher data transfer rate but not the larger memory size. New structures that satisfy both requirements have been proposed from several companies [1], [2].

14.2 Low-cost Applications

Digital AV and home appliances are stringent in cost, and small form factor is rarely regarded as an added value; therefore, SiP solution has been proposed only when SiP could cut costs down.
To meet this demand, one of the solutions is a die-stacked SiP with high-yield dice. It is because material cost is in inversely proportional to the number of dice comparing to the monolithic devices, and the yield loss cost is negligible when the dice were made through the matured wafer process. KGD problem has been the biggest obstacle for this structure. Built in self-test (BIST) or Boundary Scan Test may not be sufficient to ensure functionality, but at least it helps to increase the SiP yield and prevail over the monolithic devices from the view point of cost. Number of dice stacked in SiP is projected to be 10 for the low cost/handheld products in 2010 in Table AP101a, ITRS 2007 update. Even though this number includes the number of the dice in the PoP, still KGD problem is expected to be solved by that time.
The design concept of the die-stacked SiP is the most important in this application to achieve the lowest cost. They include co-design methodology

to optimize the substrate design with bonding pads at the best location so that substrate layer count is the least and the establishment of the standard specifications at the logistic interfaces along with supply chain management. Standard specifications include the physical pad sequence of memories as they have been discussed in JEDEC JC63 [3] and the standardized format of the die [4].

14.3 High-Performance and Cost-Performance Applications

For the high- and cost-performance applications, such as servers, PCs, and TV games, the leading requirements are the superior electrical and thermal performances for the lowest cost. Side-by-side flip-chip modules have been used for these applications with satisfactory performance. Some of these examples are a set of a micro processor unit (MPU) and memories, or a set of a graphic processor unit (GPU) and graphic memories, which require high speed data transfer rate between the processor and memory. There are several dice attached close enough to have the shortest path with well-matched characteristic impedance, while dice are immune from the interference of the heat from the next die. The distance between dice on a substrate is determined by both electrical and thermal conditions.
Further improvement of the characteristic impedance matching over signal traces, new architectures, such as embedded actives and direct build-up on a die, have been developed. Several dice and passive components are embedded in a printed wiring board (PWB) and their performance was enhanced. Heat will be dissipated via ground planes inside PWB or exposed backside of the die on the reverse side of the PWB.
Recent studies of a 3D-stacked SiP with through silicon via (TSV) interconnections enabled a large number of the shortest signal interconnections through silicon. The advantages of this structure are the smaller form factor, higher data transfer rate, and larger memory size. One of the applications may be the replacement of the Fully Buffered Dual Inline Memory Module with the bottom die as an interface die including Advanced Memory Buffer and upper dice as high speed memories [5], provided that thermal dissipation means are available.

14.4 Harsh Applications

The consumption of the semiconductor devices is growing in the automotive electronics industry associated with the increasing number of hybrid cars. Electronics components cost only 15 % for the compact car, 28 % for luxury car, but now 48 % for hybrid car. The amount of the semiconductor wafer was 0.21 of a wafer of 150 mm in diameter for compact car, while hybrid car consumes 0.96 of a wafer, which is 8 times more than the semiconductor consumption in a PC [6]. The consumption of the semiconductor devices is increasing in the automotive industry, but the quality requirements are quite high. The engine controller unit (ECU) has been located in the engine room;

auto-manufacturers are, however, now trying to place the ECU directly on the engine. The environment temperature rises to 150°C or higher, which is close to the specified maximum operating temperature of the typical semiconductors, implying that the package thermal resistance shall be extremely low.
On the other hand, other electronic devices are squeezed into the small remaining spaces in a car to provide passengers with a more comfortable cabin. The performance of automotives is rising so that they demand higher CPU performance and local network communication between devices.
With the development of high temperature-durable substrate with advanced solder resist material, as well as higher solder joint reliability mechanisms, FBGA-type SiP meets the automotive reliability requirements of engine room application. MEMS sensors, AD converter, CPU, and network devices will be packaged in a SiP for the air bag deployment sensor, active suspension, tire pressure monitoring and ESP. Automotive electronics might be the most diversifying area with sensors in terms of SiP structure.

SiP is expected to penetrate into various markets and substitute for the traditional monolithic packages on the basis of the development of the higher density package structure, its process, and the industrial infrastructure.
ITRS 2005 describe the higher value system as a combined vector of More Moore (SoC) and More than Moore (SiP), implying that SiP accommodates the analogues, passives, MEMS, biochip, etc. In addition to the inclusion of the heterogeneous devices, numerous interconnections between logic device and memories are required to provide multiple buses for higher data transfer rates.

15. Physical Architecture

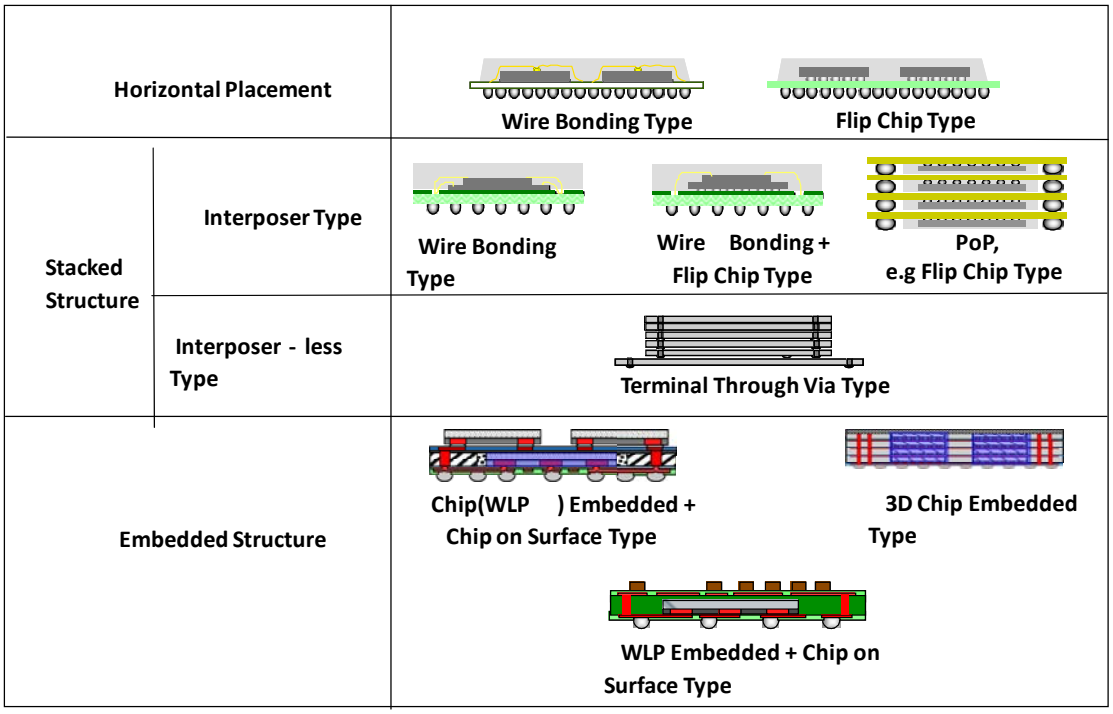

Figure 17: Representative SiP types and categories

Today we observe two main trends for system integration: i) Integration of active and passive devices, especially silicon ICs, into a package structure which is then connected to a board (e.g. stacked die, PoP, PiP, eWLB, …) and ii) embedding of passive and/or active devices directly into a board or substrate (embedded structures). SiP provides an overlap between the traditional components of chip; package and system printed wiring board.

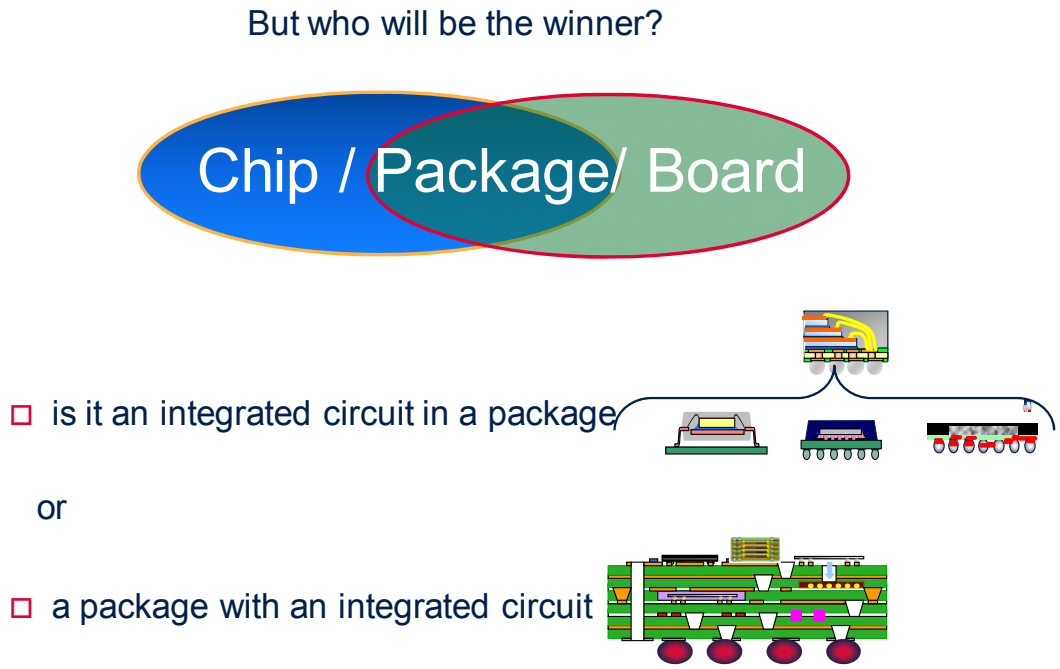

Figure 18: SiP may replace traditional system interconnect partitioning

15.1 Side-by-side placement (horizontal)

The SiP with side-by-side placement (horizontal) is a traditional multi-chip module where wire bonding or flip-chip bonding technology has been used. The chief reason of this structure is to enable higher data transfer rate between dice on module by means of flip-chip bonding and build-up substrate. For commercial applications, even though this structure is considered to be an expensive structure, the side-by-side placement with small dice may not expand the package size and keep the package inexpensive. The die-stacked structure is mostly cheaper than the side-by-side placement in terms of packaging cost.

For high-performance applications with GHz-level signal transmission, the conductor loss and dielectric loss induce the attenuation of the signals and result in the ambiguous eye patterns in the low voltage differential signal. The signal traces are designed to be wide enough to counteract the skin effect of GHz transmission, but the physical dimensions of traces, including cross-sectional dimensions, and dielectric layer thickness are to be accurately

produced to have better matching with the spice model simulation. On the other hand, the advancement of the wafer process has accompanied devices with lower core voltage, which results in less noise margin and ends up with the increasing susceptibility to the noise. Flip-chip bumps scattered over the die works as the stable power delivery system for the advanced die with the firm reference voltage level.

15.2 Stacked structure

For stacked structures we distinguish between
- stacked dice
- Package-on-package (not shown in the figure above).
- Package-in-package (not shown in the figure above)
- Terminal through via types

Stacked die

A trend towards thinner hand-held products requires less height of the die, wire bond, die-attach adhesives, substrate, and solder terminals. When the package height becomes less than 0.5 mm, the package warps significantly after molding due to the flimsy outlines and higher susceptibility to the CTE difference among the materials. The development of the thinner packages requires well-balanced combinations of package materials in terms of CTE, Tg, and elasticity. Some other requirements for the molding compound include higher flow characteristics during transfer molding and a resistance to the higher reflow temperature. When FBGA is reflowed during board assembly, solder balls collapse and tolerate some coplanarity error and package warpage. However, lowering package height makes FBGA packages migrate to lower stand-off height packages, and it tolerates little package warpage. Material development and structural study is on going to keep the package flat during the reflow process, while the criteria of the maximum tolerable package warpage at elevated temperatures are being established in standardization activities.

Package-on-Package (PoP)

PoP is a highly attractive approach to combine devices from different suppliers, to improve yield and to avoid the Known Good Die (KGD) Challenge. Today PoP is especially pushed by the mobile phone industry. Typically baseband chips are used for the bottom package and memory chips for the top package. For this set-up the interface between the top and bottom package has been standardized in JEDEC. This allows for example a mobile phone company to take an optimum choice of the top memory package applying the required memory capacity. Also for PoP warpage is a major problem. Thus, to combine packages from different suppliers the consideration of warpage is a crucial factor.

Package-in-Package (PiP)

STATSChipPAC together with Qualcom introduced a flip chip based three dice PiP solution (see ECTC 2007 [1]). According to them the package represents the ultimate in integration, wiring density, performance and miniaturization. Such a solution requires close co-working between multidisciplinary teams including packaging, design and device architecture.
[1] R. Pendse et al., “Electronic Components Technology Conference ECTC 2007”, Reno, p.1425

Terminal through via types

These solutions require TSV technology. Presently a lot of work is on-going especially driven by memory companies because they run into time delay problems using long wires. A key challenge for memory stacking is presently is to elaborate processes that achieve attractive costs for mass production.

15.3 Embedded Wafer Level Ball (eWLB) Grid Array Technologies

Embedded wafer level package technologies are now emerging. These technologies allow higher integration density and fan-out solutions. For this new approach the chips are reconstituted and embedded in epoxy compound to build an artificial wafer. A thin film redistribution layer is applied (see Fig. 1) instead of a laminate substrate which is typical for classical BGAs. Examples for investigations on such technologies can be found in Refs. [1-3]. Laminate substrates reach their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layer opens new opportunities for SiP. The possibility to integrate passives like inductors, capacitors or even active devices into the various thin film layers opens additional design possibilities for new SiP.

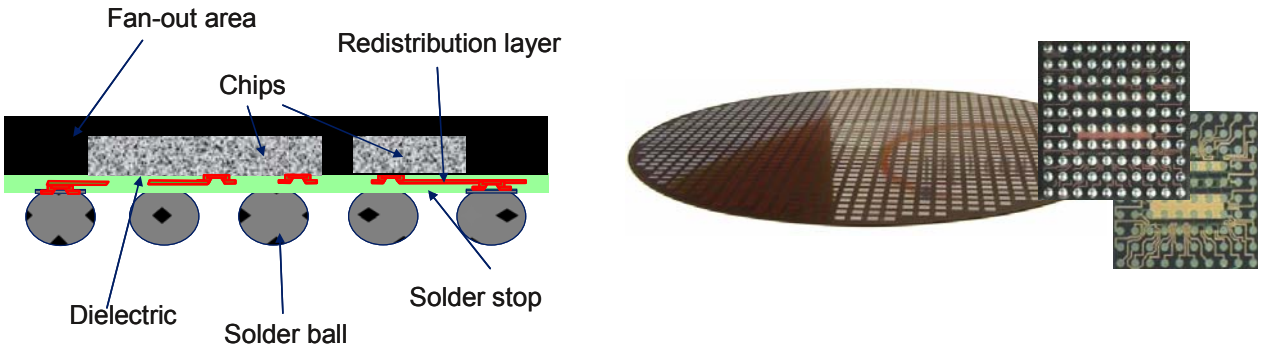

Figure 19: left: example of a side by side solution of an embedded eWLB; right: example of a reconstituted wafer (courtesy Infineon)

[1] Brunnbauer M. et al. “Embedded Wafer Level Ball Grid Array”, EPTC 2006, p. 1
[2] Keser B. et al. “The Redistributed Chip Package: A Breakthrough for Advanced Packaging”, ECTC 2007, p. 286
[3] Souriau J.C. et al. « Wafer Level Processing of 3D SiP for RF and Data Application” ECTC 2005” p. 356

15.4 Embedded and Integrated Active and Passive Devices

15.4.1 Integrated Passives (IPD)

Integrated passive devices (IPD) are subcomponents which exclusively contain passive components. They may contain all three types of passives (R, L and C) in any combination. The elements can be connected to each other in order to form certain a network, matching or filter functions, or stand alone elements to serve their function.

The introduction of new materials like thin oxides or filled polymers as dielectrics as well as the introduction of deep silicon vias is extending the value range of capacitors into the micro farad realm. Besides standard redistribution wiring systems, it is also possible to form ground planes and transmission lines to create impedance controlled RF-signal transmission.

The use of wafer level thin film processes (polymer – metal –oxide) technology offers the possibility to manufacture application specific WL-IPDs with passives in the range of:

- Resistors: 10 Ohm to 150 KOhm (e.g. NiCr at 100 Ohm/sq)
- Inductors: 1 nH to 80 nH
- Capacitors: 3 to 6 pF/mm^2 (e.g. BCB at D_k = 2.65)
  1 to 3 nF/mm^2 (e.g. Ta_2O_3 at D_k = 23)

Basically with this value range nearly 70% of capacitors and 95% of resistors and nearly all inductors for a wireless / cellular application can be covered.

WL-IPDs are designed as flip chip mountable as well as wire bondable components by using different thin film substrates like silicon, alumina or glass. Figure 20 shows an example of an Integrated Passive Device as a CSP with 2x low-pass filter with 3x inductors 3.9 nH, 2x capacitors 1.8 pF realized with a multi-layer polymer (BCB) – metal (Cu) redistribution layer on Pyrex.

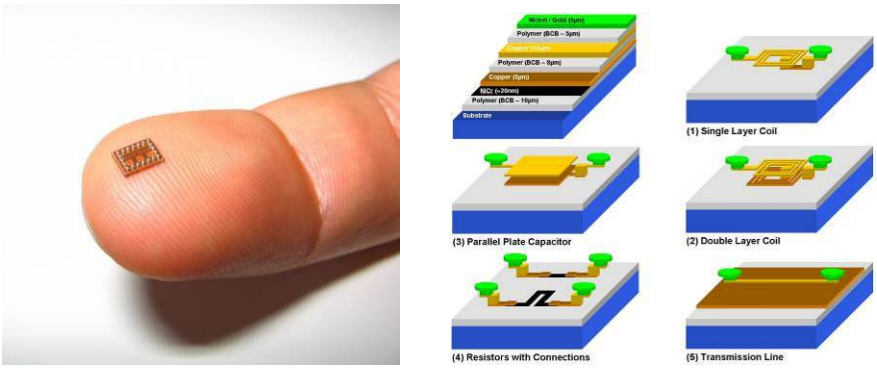

Figure 20: CSP with integrated passive devices and thin-film build-up passive elements (FhG-IZM)

Today´s bottleneck for the realization of integrated passive devices are capacitors, In combination with high aspect ratio DRI etching in silicon deep trench capacitors with an value of (20 -30 nF /cm^2) can be realized. This very promising technology is currently in development by different companies special with focus to Wafer level System in Package approaches.

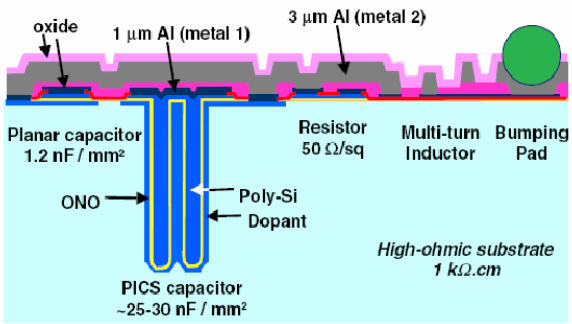

Figure 21: PICS substrate with high density “trench” MOS capacitors, planar MIM, multi-turn inductors and poly-Si resistors [13].

With respect to cost and form factor larger passive devices are implemented as SMD devices on top or embedded into substrates for System in Package approaches.

15.4.2 Active and Passive Devices Embedded in PCB

Currently some cellular applications use embedded active devices for e.g. TV tuners, finger print ID sensor, etc. Cell phone manufacturers and semiconductor device manufacturers are expected to expand the implementation of embedded actives in the next generation of communication modules e.g. GPS and wireless LAN with passive devices using the now free real estate from buried active devices. Power supply units with embedded actives and surface mounted passives also have strong demand in the market

place. Likewise, image sensors such as CMOS sensors and strobe lights for cell phone cameras will adopt the same approach in order to reduce the form factor. ASICs and graphics processors with stacked memory devices will also use embedded actives and passives.

At this point in time, two different types of active devices are common for embedded applications. One type is based on a wafer level package with thinned active devices without Cu posts which are directly interconnected by thin film RDLs. The other type is based on FC dice with Au stud bumps or Cu posts which are embedded in an organic substrate. In either case, micro via technology is used to access the die terminals and then to fan out from the die. Most often two layers of fan out are used, in advanced cases four layers may be required but may be avoided by the best chip/package co-design.

Embedded passives have been in production in PCBs for many years. Resistors and capacitor materials can be embedded as thin film or thick film materials depending on the values required. Thick film materials are typically screen printed and cured (resistors based on polymeric pastes) or fired (capacitors based on ceramic pastes). Thin film resistors are based on metal foils of either NiP or NiCr on Cu. Capacitor materials come as Cu clad cores with the thin dielectric (24um, 16um, 12 um or less) sandwiched between 1 or 2 oz Cu foils. Either foil is laminated into the substrate or PWB and processed as usual. Discrete passives are typically placed into a cavity. If the cavity is metalized, the capacitor can be soldered in place and encapsulated with prepreg. If the cavity is not metalized, the encapsulation is the same but micro vias are then used to access the terminals as in the case of embedded actives.

Figure 22 gives a schematic overview of the different embedding concepts.

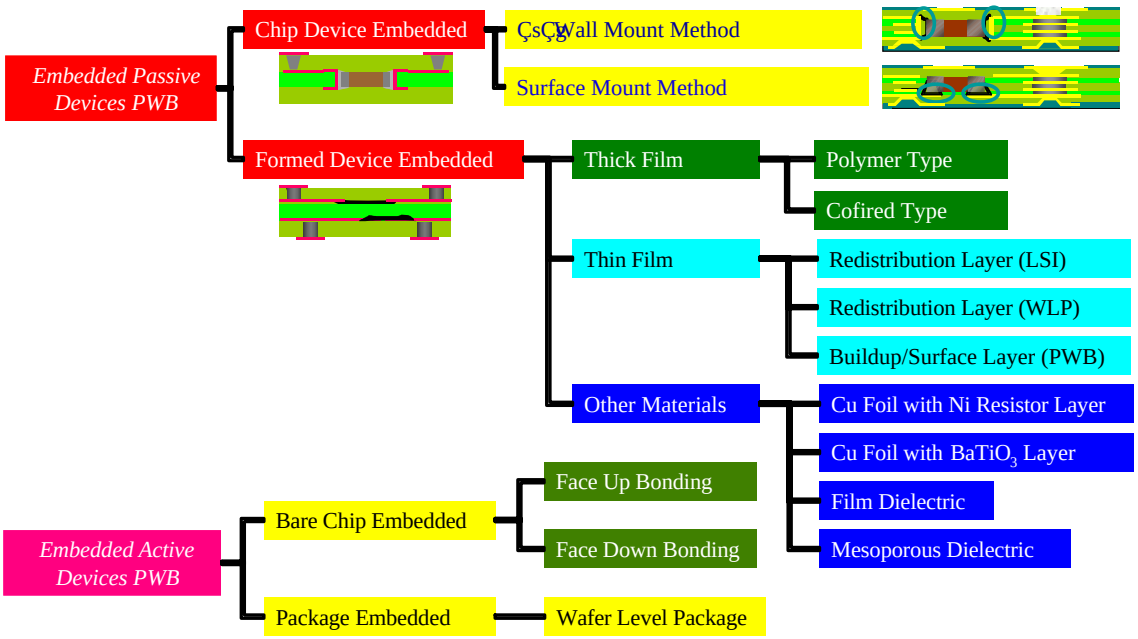

Figure 22: Overview Embedded active devices and passive devices

15.5 Architectural Selection

The SiP with equivalent performance may be assembled in many configurations. The selection process should include consideration if size, power, cost, reliability, etc. of alternatives. An example of an evaluation matrix if shown in Table 6.

Table 6: Comparison of Stacked CSP vs. PoP

Stacked CSP	PoP
Prospects • IDM ownership • Low package profile available with advanced wafer thinning technology • SMT line infrastructure • Low package cost with small substrate consumption	**Prospects** • OEM ownership • Flexible memory selection. i.e. memory density adjustment by switching stacked memory package and multiple memory suppliers • Tested as individual package level for Known Good Devices
Concerns • KGD required for high product yield • Single-sourced product • New development needed to change stacked device	**Concerns** • Package profile • Infrastructure for package stacking

SiP will both benefit from and drive the incorporation of many new technologies into more powerful systems that are smaller, lighter and more power efficient. One example of such integration is shown in figure 23 below. This system incorporates electrical, optical and fluidic I/Os that could provide for thermal management for stacked die as well as support for high speed optical interconnect. These innovations are being published today and will be incorporated into products in the near future.

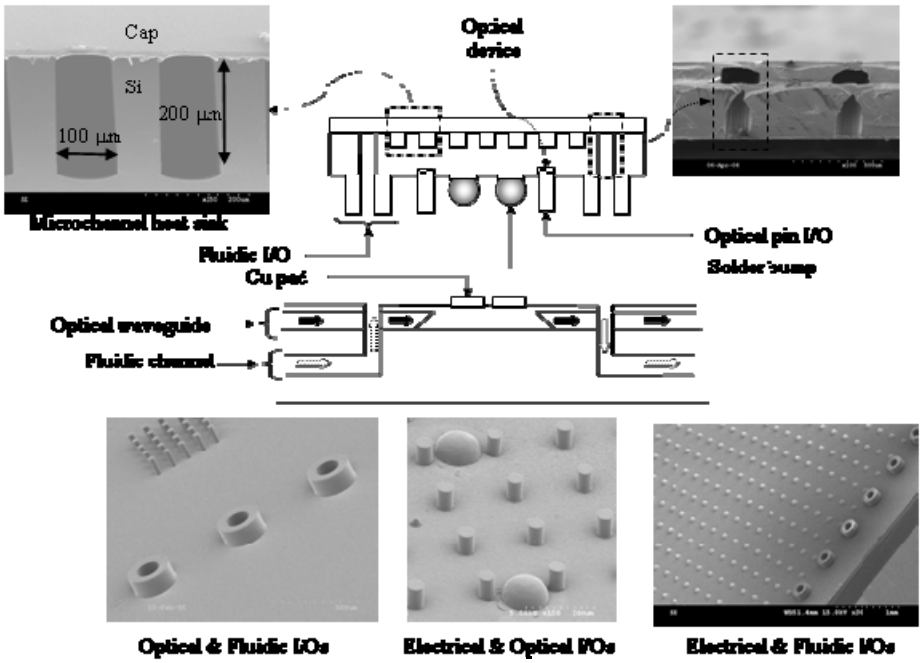

Figure 23: Schematic illustration of a chip with electrical, optical, and fluidic I/O interconnects. SEM images are also shown [1].

1. M. Bakir, B. Dang, and J. Meindl, "Revolutionary nanosilicon ancillary technologies for *ultimate*-performance gigascale systems" in *Proc. IEEE Custom Integrated Circuits Conf.* (CICC), 2007.

16. Assembly processes for System Integration

The key assembly processes of SiP are wafer thinning and singulation, die attach, wire bond, non-wire interconnection, molding, and package stack, which are becoming more complex to meet the system level requirements. Material development and selection are also important in line with the process development, such as die attach film for new laser singulation, mold compound for compression mold, and solder balls for flexible interconnection.

16.1 Wafer thinning and singulation

Wafer thinning has become a standard for consumer products and today products are being shipped with wafer thickness below 100 microns. This will accelerate for SiP where die stacks of 10 layers and more will require much thinner die to meet the package thickness requirements of portable consumer products. The challenges of singulation and handling these extremely thin die will innovative solutions requiring both new equipment and new materials.

16.1.1 Introduction

ITRS provides two separate tables for wafer thinning; one is for extremely thin packages and die-stacked packages, the other is for conventional packages. The extremely thin packages are such as embedded active components in build up layers, chip in a film, and wearable devices. The die-stacked packages include SiP with tens of dice stacked and interconnected with wire bonding or through silicon vias (TSV). The wafer thinning roadmap of the extremely thin packages have been driven by the form factor which is indispensable for mobile electronics, but now the advantage of higher process throughput is accelerating the thinning trend for other applications. It is because thin wafer allows shallow depth of TSV or Reactive Ion Etching (RIE) trench for dicing. On the other hand, the wafer thinning for the conventional single package is strictly constrained by cost and die strength. Die breakage force is proportional to the die thickness, even though durable maximum stress on the die is nearly constant regardless of its thickness. How much thinner the manufacturers could manage wafers depends on the process and quality control capability. The practical limitations on die thickness will be a function of performance of thinned integrated circuits and BEOL yield rather than the ability to thin the wafers.

16.1.2 Thinning, polishing and dicing

Wafer thinning and subsequent handling process are one of the competitive development activities. The most popular wafer thinning method is mechanical grinding due to its high throughput, about 15 times faster than dry etch method, even though it generates residual defects on the ground surface. Removing this defect layer requires additional process to realize the intrinsic strength of raw silicon bulk. This process includes chemical mechanical polishing (CMP), dry chemical etching, or wet chemical etching. There were many technical reports related to the thin devices. For example, a flash memory die with thickness of 10 μm was made and verified if it functioned. A tiny RF device with 50 μm x 50 μm x 5 μm was fabricated from SOI wafer, and the top and reverse faces of the die were designed as terminals for antenna. In contrast to these aggressive development reports, the manufacturing infrastructure for the extremely thin wafer has never been satisfactory.

When a wafer is thinned to 50 μm, it becomes flexible and tends to warp due to CTE mismatch between dielectric cover layer and silicon substrate. Wafer support carrier is often attached on the wafer prior to thinning process to redeem its flimsiness, and then detached after wafer bonding with TSV interconnection. Carrier support system increases the handling cost of attachment, detachment, carrier maintenance, and material. One of the challenges is a carrier-less grinding with the wafer rim remained in original thickness to retain robustness of the wafer. This method may eliminate additional handling cost for the extremely thin wafers, especially for very small devices.

Wafer has conventionally been diced by diamond blade, which creates scars and chippings on the side surfaces and deteriorates its durability against the wafer breakage. These scars and chippings can be reduced by finer mesh blade at high spindle speed at the expense of shorter blade life. There are other alternative dicing methods which provide a clean cut, such as RIE for extremely thin wafer or for the process of dicing before grinding (DBG) and laser dicing.

Advantage of shorter process time to create shallower TSV and RIE trench accelerates the development of extremely thin wafer. Wafer thinning, polishing, and dicing are interacting processes, and their process design for extremely thin wafer is still on the way to establishment of the infrastructure. Equipment suppliers and semiconductor manufacturers are cooperating to establish the complete system for handling the extremely thin wafers.

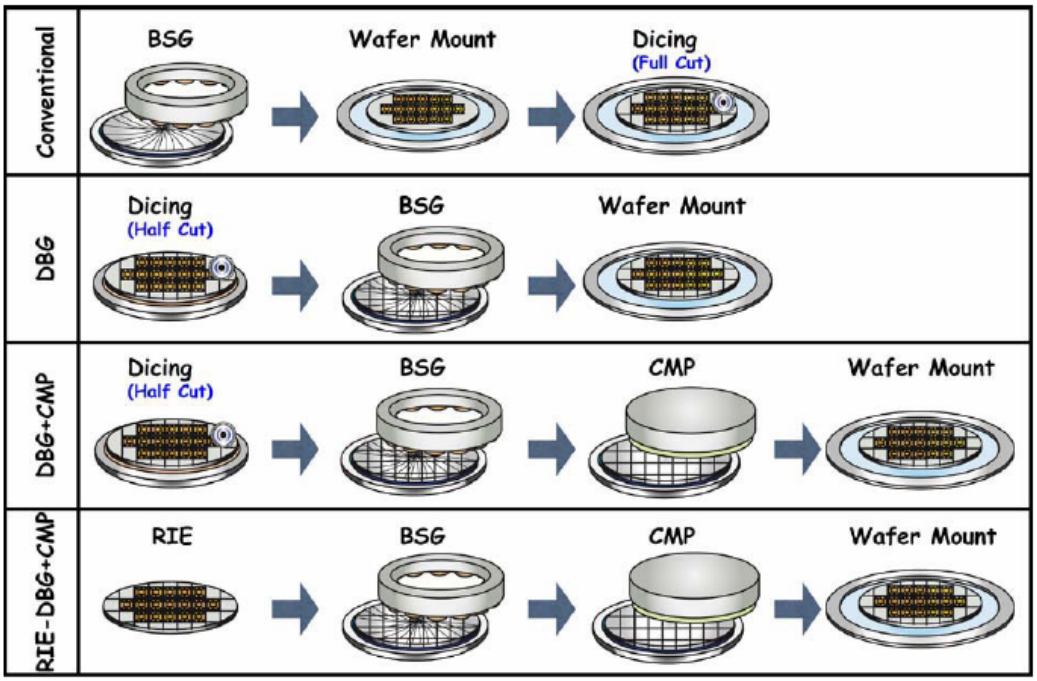

Figure 24: From ECTC 2006; Novel Wafer Dicing and Chip Thinning Technologies Realizing High Chip Strength, Shinya Takyu, et al.

16.1.3 Assembling extremely thin die

Thin wafer or die requires sensitive handling and fine machine tuning, which is more challenging rather than thinning wafer itself. Conventional die preparation process follows the sequence of dicing after grinding, while DBG is said to be preferable for the wafers whose thicknesses are less than 50 um. However, even DBG process is not efficient in the preparation of the extremely thin dice. For example, die attach film (DAF) ought to be attached after the defect layer removal; DAF shall be cut separately for each die by laser in the additional process.

There are three major technical developments required in assembly; a stress relief after grinding, a dicing before grinding method (DBG), and a wafer

carrier support. Entire die shall be immune from the chipping or cracks caused by wafer thinning or die singulation. The DBG and fine wafer-grinding method, such as wafer grinding by resin bonded wheel, have been introduced. Additional polishing process is required to keep the thinned dice, such as 25 um in 2006 and 15 um in 2010 as ITRS states, durable to the external stress in a package. Singulation of a wafer is another key technology to retain the die strength. Wheel dicing has been the main stream of the singulation, but it tends to create the chipping at the side of the die and induces cracks of the die by external stress.
New singulation method includes a new laser cut, the principle of which is to focus the laser beam below the surface of the silicon wafer, thus creating a fault line that cracks the wafer from the inside outwards. Complete breakage may be either spontaneous or by means of expanding the tape upon which the wafer is mounted.

16.2 Die attach

Die-attach film became popular as a die-attach adhesive because of its uniform thickness, compatibility with the existing assembly process, and bleed-free characteristics. When many dice are stacked each other, the thicknesses of the die-attach adhesives are not negligible. The thickness of the die-attach film is requested to be thinner but still capable of filling the indented pattern surface of the substrate. And the traditional silicon spacer between active dice is going to be replaced by the thick die-attach film to lower the height and lower the cost. The die-attach film for that purpose is capable of embedding bonding wires in the film bulk during the die-attach process. New pick and place mechanisms for very thin die have been proposed from several vendors and already examined in various locations. (See Section 9.5 for detail on die bonding film)
Picking thin die is a new technology that is required for stacked die. Methods are being developed. To stay within standard package heights, the stacked chips need to be thinned. The backgrinding process is used to reduce the die thickness to the range of 50 - 125 µm. As a result, wafer handling needs special attention. A gentle and controlled die pick-up procedure is needed. These designs often involve sequenced needles or telescoping mechanisms.

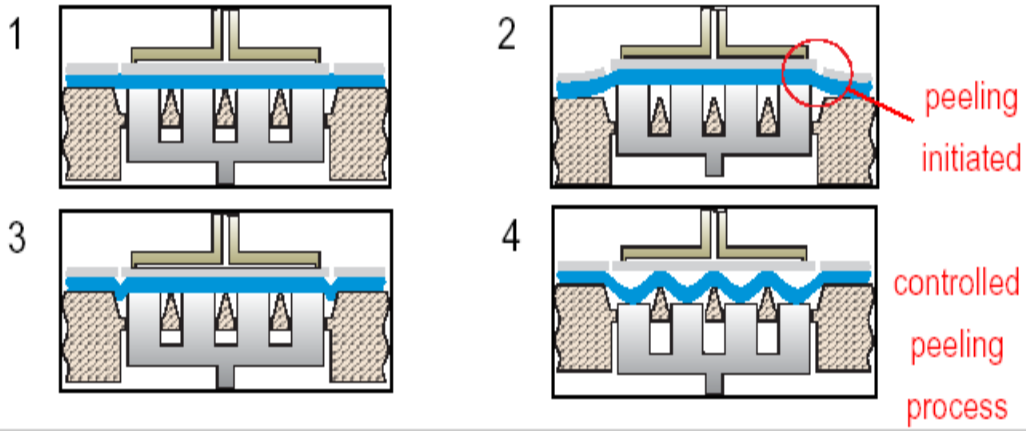

Figure 25: Mechanism and technique for Picking Thin Die

16.3 Wire bond

A number of approaches have been developed for attaching die mechanically to the SiP package substrate and making electrical contact between the die and substrate electrical traces. Figure 25 shows the wire bonding technology for SiP.

Green Validated
Blue Projected

Max Package height			
1.0 mm	0.9 mm	0.8 mm	0.7 mm
Loop Height (max.)			
75 um	50 um/	40 um	
Overhang Thickness / Distance (mass production)			
100 um / 1.0 mm	100 um / 1.5 mm	100 um / 2.0 mm	
75 um / 0.5 mm	75 um / 0.75 mm	75 um / 1.75 mm	75 um / 2.0 mm
50 um / 0.25 mm	50 um / 0.4 mm	50 um / 0.75 mm	50 um / 1.0 mm
First Die Thickness			
75 um	50 um	40 um	
Pitch / Wire Diameter			
60 um / 1.0 mil	50 um / 0.8 mil	45 um / 0.7 mil	40 um / 0.6 mil
Active Die per Stack (leading edge)			
6 (ITRS 6)	8 (ITRS 7)	8 (ITRS 8)	9 (ITRS 9)
Active Die per Package High Volume			
3	4	5	6
Special Requirements			
Programmable Focus / Cascade Bonding	3D Looping	Special Wire	

Figure 26: Wire Bonding for SiP Packaging

Another new technology under development for same size stacked die is called “film over wire” or “chip over wire”. This technology is already used in mass production by some companies. In this technology film is attached to the bottom of the wafer. In the die bonding process a heated collet picks up the die and places it directly over a previously wire bonded die. The heated film becomes the consistency of oil and if proper force is applied the liquid film will encapsulate the wires. The die must be held in place for 3 to 5 seconds for curing. In order for this process to work the wire bonding temperature must be lower than normal, less than 120 or 100°C.

Figure 27: Film over Wire Technology

There are many innovative approaches using wire bonding that are extending the life of this technology. The example given below of bonding on both sides of die illustrates the ability to build complex interconnect structures using the 3D routing for SiP implementations that is available with wire bonds.

Note:
This device is bonded in four passes..

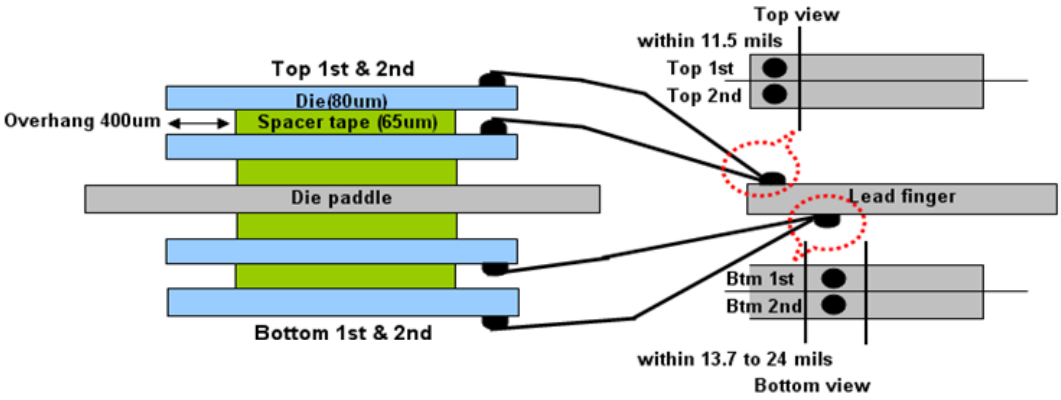

Figure 28: Bonded on both sides

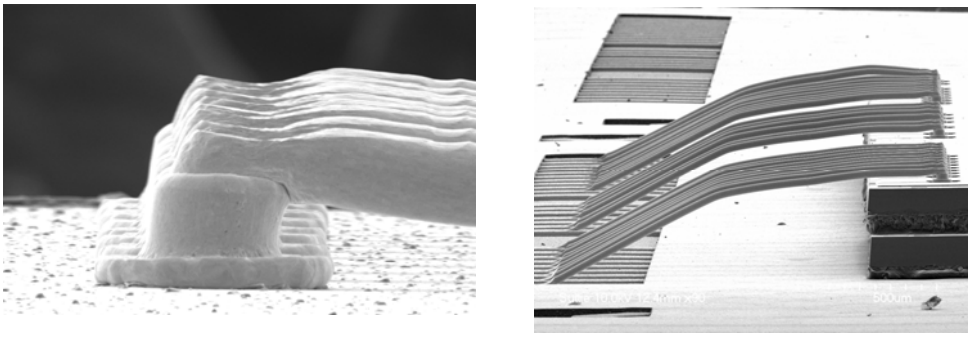

Figure 29. Compress low loops

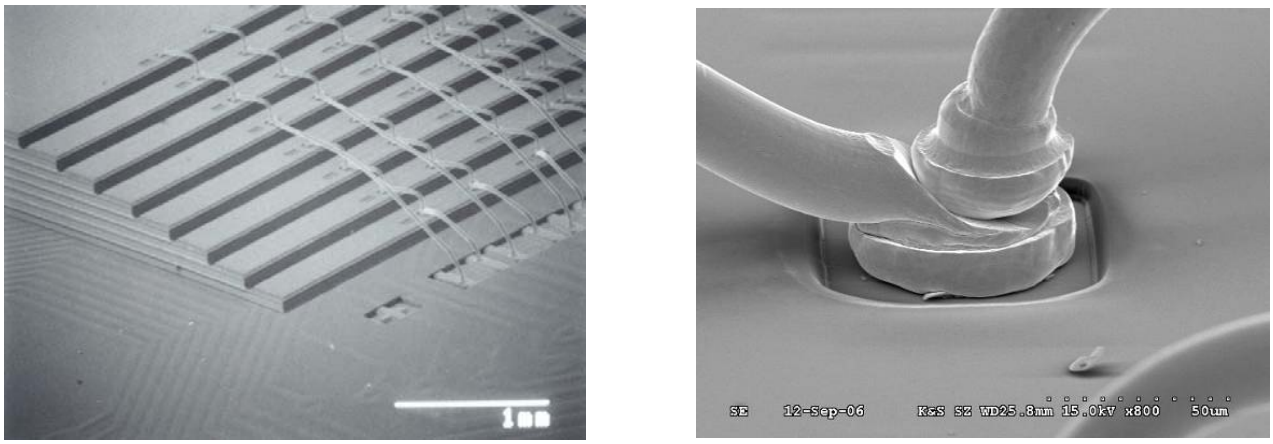

Figure 30: Cascade Bonding

As package wiring becomes more complex creating designs that avoid crossed wires and have workable wire-to-wire clearances. Traditionally package design tools have 2 D capability and this is not sufficient for stacked die SiP packages. Companies have 3 D package modeling Tools that interface to the bonder and create looping trajectories that can be utilized in production.

Stacked DRAM packages that have center “spine” pads and small die sitting on larger die that need to be bonded to the substrate fingers require Long in Board Looping – This long in board looping needs create consistent kinks in the wire far away from 1st bond.

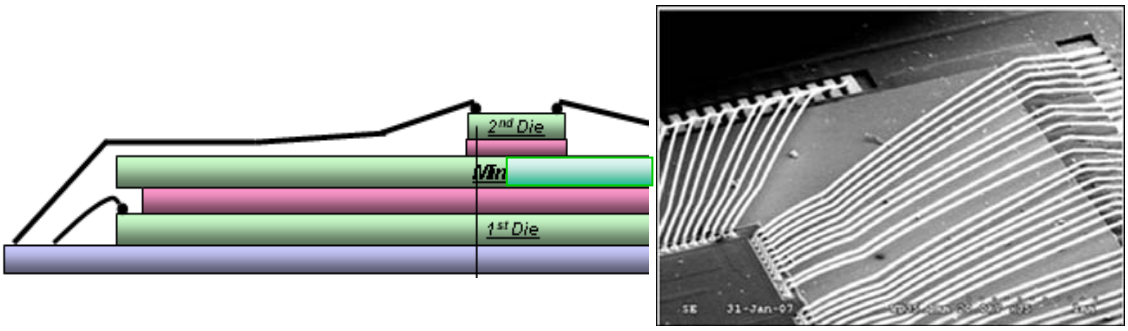

Figure 31: Long In-Board Application

As same side die are space apart and stacked, Bonding to Overhung die becomes necessary – The normal bond forces can deflect these thinned die and this compliance can create looping and bonding difficulties

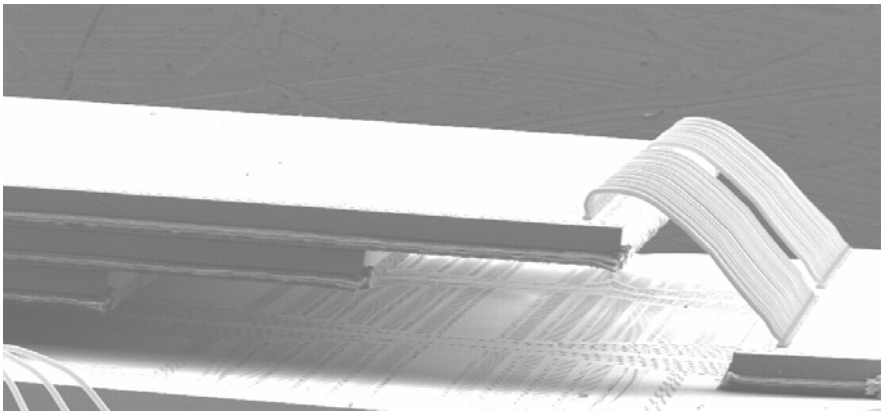

Figure 32: Bonding to overhangs

The 2 layer laminate substrates in production are as thin as 125 um and are roadmapped to be down to 100 um in the near future. This coupled with the very low wire bond loops provide a very difficult challenge for looping because there is no ability for these nearly horizontal loops to accommodate the contraction of the substrate when it returns to room temperature after bonding. Thermally compliant Loops that have compliance in the horizontal direction are being developed.

16.4 Flip-chip interconnection

Flip-chip interconnection is used in some of the side-by-side SiP, where electrical function is the major reason to adopt FC bond, and in some of the PoP, where the height of the bottom package is limited by the solder ball height of the top package.
There are generally three types of bumps; gold-stud bumps, solder bumps, and copper columns. The gold stud bumps are used for the peripheral pad layout, where volume is relatively small to design a redistributed layer. The solder bumps are used for the high volume production with area array layout. The copper column is used especially for fine pitch applications, and it may be too early to use in SiP. Also there are two underfill-applying methods; underfill after flip-chip attach or applying underfill resin before flip-chip attach. The former method has higher throughput in a flip-chip bonder, while the latter method has relatively lower throughput but advantage of less process steps. The advanced underfill material for the latter process functions as a flux during reflow process, and then it is deactivated and turns into underfill resin after reflow [8]. Only recently underfill molding was introduced for an RF SiP. Even though flip-chip bonding technology has been used for a long time, its technologies are diversifying and not ready to converge to a single method yet.

16.5 Through Silicon Via

Via last

One method used to achieve 3D integration is bonding integrated circuits interconnected with through silicon vias (TSV). The technologies required for 3D-stacked SiP with TSV interconnections are the wafer-thinning, efficient drilling, filling of the conductive material, interconnections between wafers, and heat dissipation. TSV is mainly formed by the Bosch [10] process (add a reference), the principle of which is the repetition of oxidizing the silicon via wall and dry etching the bottom of the via.
Other drilling methods have been studied and reported such as the laser drilling [9], and single etching with beveled holes [11] but plasma etching is the dominant method today. Laser drilling is used successfully for some applications today and may become more important as wafer thickness decreases further.

The limiting factor in TSV technology is via filling. The aspect ratio for filling small diameter TSV structures is limited unless a very slow process is used. Fine pitch via filling is primarily through copper plating. The filling of larger vias can be accomplished through many processes. The processes in use today for production filling of large vias include poly-Si, conductive paste and several others.

A system level concern for TSV 3D integration is thermal management which is dealt with elsewhere in this document.
TSV presents significant assembly challenges. These include placement

accuracy and, more importantly, the attachment method. The attachment will depend on the configuration of the die with the TSV; are they to be stacked? Placed on a substrate? etc. The issues with TSV assembly, especially in SiP assembly are still not totally defined. In general, die are likely to be stacked in a separate operation before SiP assembly.

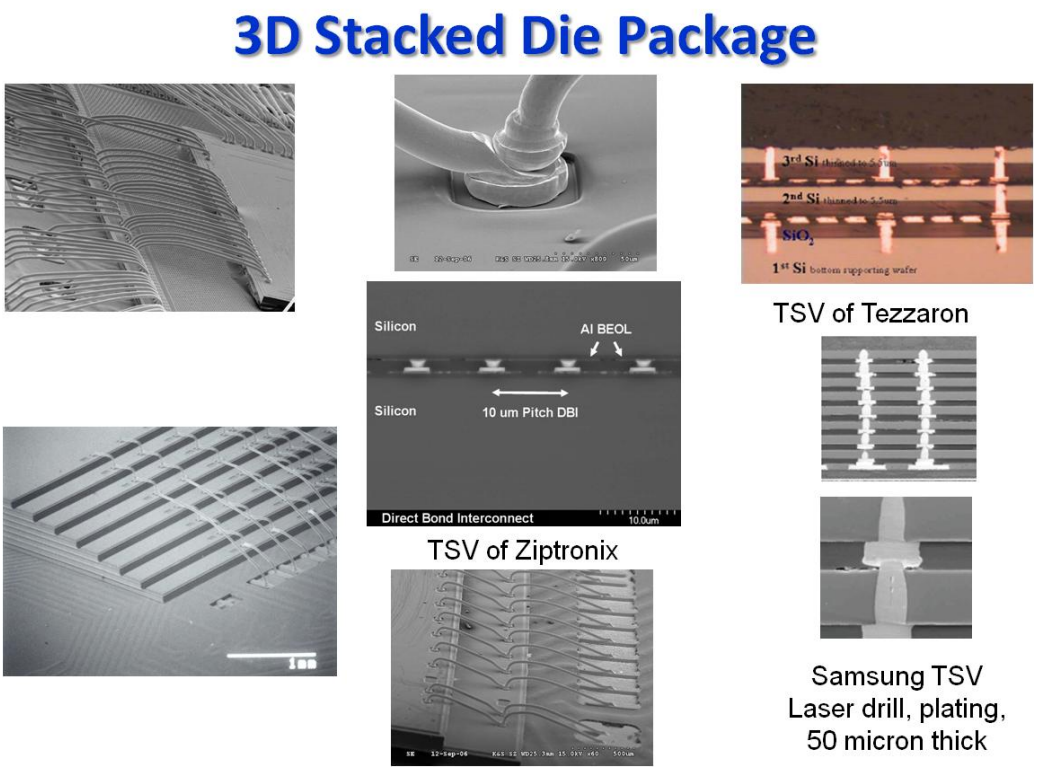

Figure 33: Examples of die stacking approaches

Via first

One example of via first construction, based on several annular concentric trenches is described below. In order to find a compromise between high aspect ratio deep etching and the subsequent void-free polysilicon filling, several via geometries have been tested. The main idea is to have a global via diameter with a maximum of 100 µm or 80µm. The via is formed by 3 or 4 annular trenches and the width of each trench varies from 3 µm to 6 µm
This new pre-process vias technology included 8 main steps:

1. Silicon deep etching
2. Thermal SiO2 insulation
3. Doped polysilicon void-free filling
4. Front side polysilicon CMP and backside etching

5. Front side daisy chain achievement

6. Front-side handling wafer bonding

7. Backside Silicon thinning

8. Backside technology for taking contact and complementary daisy chain achievement.

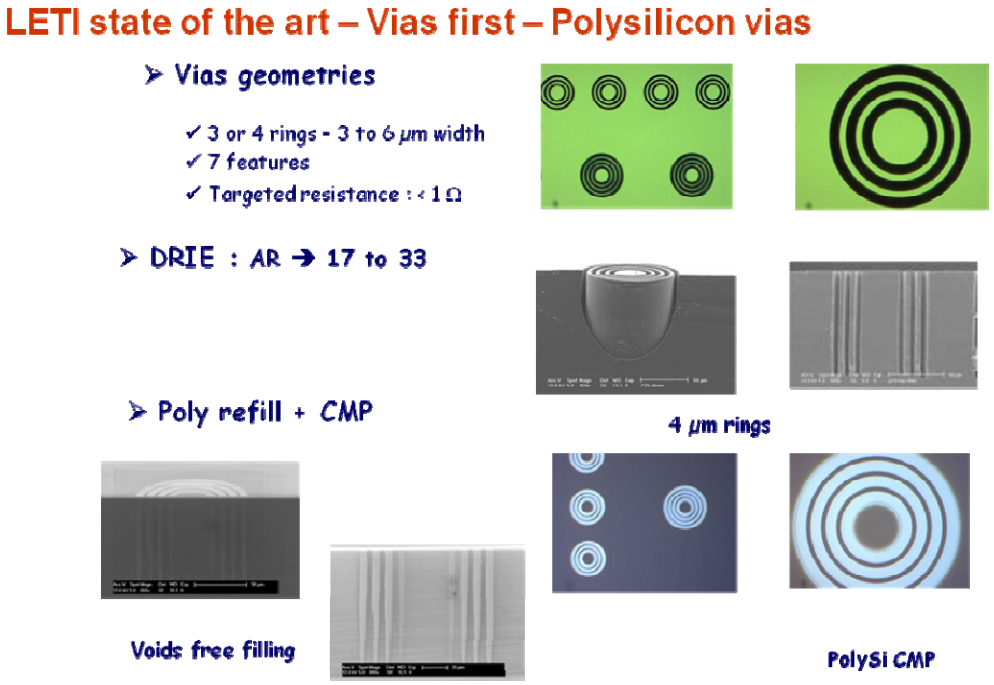

Figure 34: Via first polysilicon vias Source: LETI

One impact of high density through silicon vias is to alter the stress on transistors located near the vias, particularly during thermal cycling. It is not yet known how close TSVs can be to transistors without degrading their performance due to stress. This issue will be important for both via last and via first processes.

16.5.1 Bonding technology for TSV

TSV bonding can be performed at the wafer level (wafer to wafer) or at the die level (die to wafer). The advantage of bonding wafer to wafer is high throughput but it is not likely to be dominant for SiP. There are several issues that are problems for wafer to wafer bonding. They include:

- Wafer to wafer does not allow bonding of only known good die. Yield loss associated with defective die is multiplied by the number of layers.
- The number of different die types is limited
- Dicing bonded wafers is not yet a production process

- Bumpless interconnect and alignment tolerance at wafer level is not yet a production process.
- Wafer bowing of thinned wafers will require a solution to achieve production yields.

16.6 Molding

The challenges in the SiP molding include thin-body molding, wiring sweep, voids under the overhang die, bonding wire shorts and limited production through-put. Progress is being made in these areas but much work remains to be done.

Thin Body Molding

Thin packages are prone to warpage, and chips with low-k dielectrics are more sensitive to stress. In both cases, low modulus molding compounds are in development to minimize the problems.

Wire Sweep

Conventional bottom-gate molding can cause excessive wire sweep and create yield loss in complex SiP packages. New developments in top center mold gate (TCMG) provide a radial mold compound flow from a top gate that minimizes wire sweep. TCMG requires a smaller clearance from the top die, allowing a thinner package and reduces substrate cost by reducing the overhead space between units on the strip because of the absence of the bottom gold gate. TCMG is critical to molding mold caps of <300 μm for both stacked-die and stacked packages. Pin gate transfer molding method has also been used in the PBGA molding to avoid wire sweep and enabled longer wiring. The brief principle of this method is transferring mold compound from the pin gate located at the center of the die so that the melted mold compound flows radiationally along with wires, which keeps wires straight.

Bonding Wire Shorting

A novel approach to reduce or eliminate the occurrences of wire shorts in molding is the employment of coated wire. Coated wire has been in development for a few years and has achieved some level of technical success. However extra relatively high expense of coated wire has prevented it's proliferation into the market.

Production Throughput

Most of the substrate design of the SiP and FBGA follows the area array format to maximize the number of devices on a substrate strip aiming at the minimum package cost. Dice are attached any location on a strip; therefore, pin gate molding is not appropriate for SiP or FBGA. To fulfill these requirements, the compression molding process was developed. It follows the

sequences of placing necessary amount of molding compound in the cavity first, heating up, placing the ready-to-mold substrate strip over the cavity, clamping the strip by the die set, and providing the pressure to the molding compound to have sufficient bond with the substrate and die [14].
This technology causes little movement of the melted molding compound and is most likely to have the wire length longer, package body thinner, accepting larger number of die on a strip.

16.7 Package stack

Package stack is a particular process for PoP. Either board assembly vendor or semiconductor manufacturer stacks packages. Top and bottom package warp in different manner during reflow process. For that reason maximum tolerable package warpage at the elevated temperature is much less than that for other packages. For better process capability of the package stack, the top package is stamped on the disc where solder paste is leveled to the specified thickness by blade [15]. The crowns of solder balls gains some amount of solder paste and it functions as the additional tolerance for the coplanarity error. Also double deck structure having additional interposer substrate to allow more gap distance between bottom and top package is becoming popular. The top and bottom packages contain two or more dice each, and then stacked to PoP which accommodates four or more dice without any cumulative yield loss problem. It may accelerate to increase the numbers of the stacked die in a package, as stated in Table AP11a, ITRS 2007.

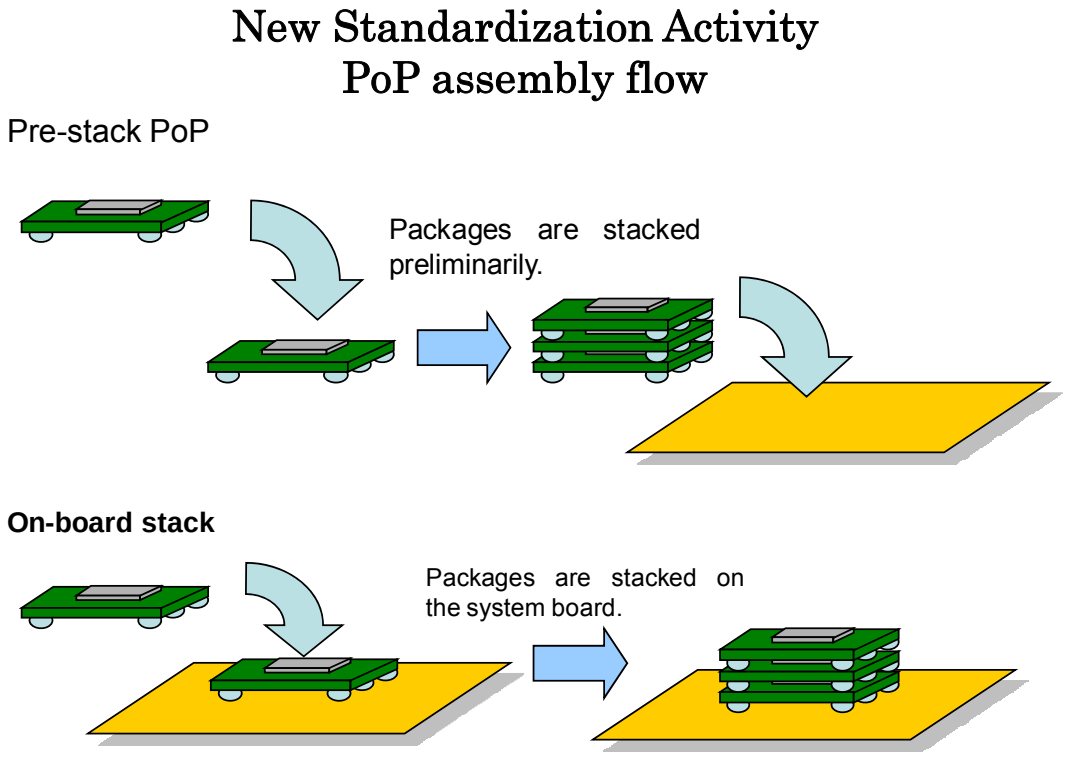

Figure 35: Production flow for PoP

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17. Materials

The Assembly and Packaging industry has been in the midst of a sea change in materials. The bill of materials in packages only yesterday may not be the same tomorrow. And these changes are expected to accelerate in pace and scope in the coming years. Much of the near term new materials introduction is driven by environmental regulatory compliance requirements including Pb-Free and RoHS compliance (European Union Directive for Reduction of Hazardous Substances). The migration to “green” materials that are lead-free (ROHS) and halogen-free (WEEE) compatible are in full swing. Industry has been adopting “green” materials for the new products packages when they transition to new packaging materials to meet RoHS requirements. . Materials for the traditional wire bond and flip chip packages including molding compound, die attach materials, underfill materials, thermal interface materials (TIM) and package substrates, will have to be improved to meet Lead-free,

Halogen-free and Low-κ/ULK requirements.

The widespread adoption and ready acceptance of Stacked Die package and the more recent Package on Package and Package in Package are based upon the basic premise that these packages are all readily designed, manufactured, and tested and qualified on existing manufacturing tools, materials set including substrates, and equipment. Stacked packages are based upon commonly available substrates including leadframes, rigid laminate substrates, and flex substrates. Most of the stacked die package applications today use wire bond interconnects with wirebond and flip chip hybrid emerging.

In the same way Wafer Level CSP package are based upon the manufacturing technology and infrastructure of flip chip wafer bumping technology and infrastructure and BGA ball drop technology and infrastructure.

New materials and materials processing technologies will be needed to meet the technology requirements for the packaging and assembly advanced node of next generation devices. While wirebond and flip chip remains to be the two basic interconnect methodologies, the introduction of low k dielectric materials, increasing power density, and hand held consumer products, imposes additional requirements to traditional materials applications. For example with the mechanically weak low-k and the still weaker ultra low-κ dielectrics in the device, comprehensive design of underfill materials properties compatible with the bump materials properties are crucial in addressing the risk for interface stress damage to the dielectric layer. With the increasing thermal output and uneven temperature distribution of many IC device applications, thermal interface materials represent an important opportunity for innovation. The drive for miniaturization through die stacking, package stacking, and low profile packages requires improvements in molding compounds, underfill materials and die attach materials originally developed for traditional single chip packages.

The developments of system in package (SiP), wafer level packaging, embedded die and passives, and through silicon via (TSV), will call for innovations in design of materials and materials processing innovations beyond what is available today. Wafer Level Packaging (WLP) will require materials with improved or different properties as it evolves to meet new packaging applications. Different metallization systems for both redistribution traces and under bump metallization, as well as new dielectric polymers are needed to meet the ever changing reliability requirements for portable electronic devices. The development of fanout WLP and embedded passives/actives will require new low temperature embedding polymers and low temperature cure redistribution layer polymers. TSVs will benefit from new dielectric insulators and conductive via filling media for improved low cost manufacturability. Integrated Passive Devices (IPDs) will also require better materials, with improved electrical properties, for both resistive and capacitive devices.
The Emerging Research Materials Chapter of 2007 ITRS will review advanced

packaging materials such nanomaterials based TIM with significant better capabilities over the current materials set. The major materials challenges are summarized in Table 7 below.

Table 7: Materials Challenge for Packaging

Materials Challenges for Packaging	Issues
Wirebond	Materials and processes for low profile wirebond loop. Materials and process for multilevel stacked die without wire sweep. 30 um fine pitch wire bond
Underfills	Ability to support high Tj operation, compatible with low-K die, and compatibility with lead free reflow temperature. Optimal Cu Piller underfill
Thermal Interfaces	Increased thermal conduction, lower interface resistance, improved adhesion, higher modulus for heat sink applications
Materials Properties	Methodology and characterization database for frequencies above 10 GHz
Molding Compound	Molding compound for low profile multi-die package. Compatible with low-κ wafer structures with low moisture absorption for high temperature lead free applications Molding compound for hybrid wirebond and flip chip w/o underfill Gate leakage associated with charge storage in halogen free mold compounds Metal particle contamination causing delamination and assembly yield problems
Lead-free Solder Flip Chip Materials	Solder and UBM the supports high current density and avoid electromigration
Low stress die attach for Tj >200C	No feasible solution known to compensate for TCE mismatch with high thermal and electrical conductivity
Rigid Organic substrates	Lower loss dielectric, lower TCE, and higher Tg at low cost
Embedded passives	Improved high frequency performance of dielectrics with κ above 1000; High reliability, better stability resistor materials. Ferromagnetics for sensor and MEMs applications
Environmental regulation	Cost, reliability and performance compatible materials must be identified to replace those banned
Solder bump replacement	Flexibility in joining to accommodate stress associated with TCE mismatch over the operating range
Die attach film	Thin wafers will suggest combination of dicing film and die attach film in a single thin film material. Lower thickness film Embedded wiring in film
Through silicon vias	low cost via filling material & process (e.g. low cost seeding and plating process) thin wafer handling carrier material and compatible attach material

18. Equipment

As has been discussed in earlier section on equipment packaging innovations such as Wafer Level Package and System in Package have specialized equipment requirements. Current equipment used for wafer level packaging is based upon front end processing equipment modified to meet specific packaging needs. New generations of equipment will be required for wafer level interconnects structures and specialized under bump metallurgy, TSV and embedded wafer level structures. Examples include: solder bumping, passivation, redistribution, through via interconnect, integrated passives, backside metallization, optical interconnect, dies to wafer and wafer to wafer bonding and post processing thinning. Improvement in throughput and operating cost (cost of ownership) are essential for meeting the cost reduction requirements of the Roadmap.

With Wafer Level Packaging the boundary between front end processing (wafer fabrication) and the back end of the process (assembly and packaging) is blurring. With the introduction of TSV and wafer to wafer bonding there is a still wider gray area. Today TSV technology is being developed with different directions and applications under different business models. The situation analysis may be depicted in the following bullet points.

- Different Directions for TSV for different design requirements, form factors, applications and markets
- No high volume TSV device and product in manufacturing
- Many diverse groups pursuing different conceptual manufacturing process approaches.
- Thin wafer handling protocol through different process environments and different equipments will be important consideration for high volume production equipment manufacturers.
- Process and materials compatibility and design objective often determined the conceptual process configurations.
- Industry, research institutes, and academic institutions are working on TSV R&D using equipments designed for other purposes
- There are many diverse approaches. It is expected that these approaches will consolidate into a few, in order for the equipment industry infrastructure to meet the TSV process and manufacturing needs.

- Consideration will be given to processes, materials (including consumables) and equipment for the best cost of ownership and lowest possible product cost and productivity for the market place.

- Likely emerging adoption of TSV are: memory stacking, heterogeneous system integration

For TSV implementation there are some common process steps which include some of the following:

- Wafer Carrier and Carrier attach to wafer
- Sequential Wafer Thinning
- Via Making
- Isolation
- Seed deposition – High aspect ratio Cu via plating
- Via Filling
- Redistribution
- Backside processing
- Mini-bump
- Align and Bonding – Die to wafer, wafer to wafer, Die to Die
- Dicing
- Probe and Test

In order to understand the issues and cost drivers for these overlap processes such as wafer level packaging and through silicon vias, materials and equipment suppliers are creating alliances or consortia. One example addressing 3D integration using Through Silicon via technology is the EMC-3D consortium (www.emc3d.org). This consortium will develop processes for creating TSV structures use both via-first and via-last techniques with the goal of reducing today's 3D integration manufacturing cost by substantial percentage.

19. Testing of SiP

Testing of SiP poses many new challenges. The incorporation of components such as bio-chips, MEMS devices, micro-fluidics and optoelectronics that require tests outside the boundary of traditional ATE will require innovation. In order to minimize cost and cycle time in production new approaches will be required. The solution will not be one single breakthrough but rather a combination of innovations that will use DFT and BIST technology as well as the incorporation of test elements into the SiP itself.

There are 2 major issues with SiP test for conventional electronics:

First, for the known good die (KGD) issue, a KGD may be defined, from practicality point of view, as a die good enough for SiP integration. It must be

functionally good before assembly and reliable as well. To satisfy the 1st condition of goodness, the Circuit Probe (CP or wafer sort) yield criterion should be upgraded to its final test level. The issue then is the ability to probe wafers at speed, or to embed a comprehensive set of DFTs to be tested at low speed, or a combination of both. The 2nd KGD requirement is known reliability before assembly, which would require a wafer-level burn-in methodology equivalent to its packaged burn-in test.

Second, the final test (FT) solutions for SiP would be similar to those of the conventional packages, except for custom socket designs for non-standard or high-pin count SiPs, and FT failure analysis for a 3D SiP with through-Silicon-vias (TSVs): probing the internally sandwiched dice upon an FT failure being an issue. DFT development for 3D-TSV SiP remains a challenge.

The limited test access in SiP architectures requires the partitioning of test during design to ensure the ability to perform adequate testing.

19.1 Partitioning of SiP Test

The testing to ensure the quality and reliability of SiP must occur at multiple levels in the production process beginning with a definition of test strategy even before the detail design is started. The levels of test planning and implementation include:

- System level test strategy
- Test strategy and test platform at SiP level
- Design for Test (DFT)
- Component level test
- ATE based Electrical test methodology/procedure
- Individual test of sensor/MEMS/opto/microfluidics/MEMS/etc.
- Burn in

Additional information concerning SiP testing can be found in the Test Chapter of the 2007 ITRS.

20. Cost

The cost of SiP vs. conventional system integration is favorable for only a few relatively simple products today. The most common are stacked die components used in cellular telephones. The issues that drive high cost for the more complex SiP devices include assembly yield and cost of test.

The advantages in system cost due to higher levels of integration will drive SiP market share for an increasing number of products as the technology matures. The intrinsic cost advantages of SiP which uses less material, requires less energy and increases performance will outpace the disadvantages in yield and cost of test as the processes mature and production volume increases. Detailed cost analysis is not yet available comparing SiP to Soc and conventional system level integration and will be needed to support system partitioning decisions by manufacturers. The elements of cost that must be quantified for SiP relative to conventional alternatives include:

- Cost of Known good die (KGD) including test costs
- Substrate cost
- Cost for embedded components
- Final test cost
- Component bonding and interconnect
- Yield
- Thermal management
- Repair and rework
- Unique equipment costs
- TSV processing equipment, process and yield
- manufacturing (processing) cost
- PoP vs. Die-stacked SiP (KGD)

21. Regulatory Issues

There are important environmental issues that are covered by legislation and additional regulatory actions should be anticipated as new materials are developed and the health and safety issues associated with materials currently in use are better understood. The regulations impact the cost, reliability and performance of electronics products and have a significant impact on the industry. The history of regulatory constraints is shown in figure 3.

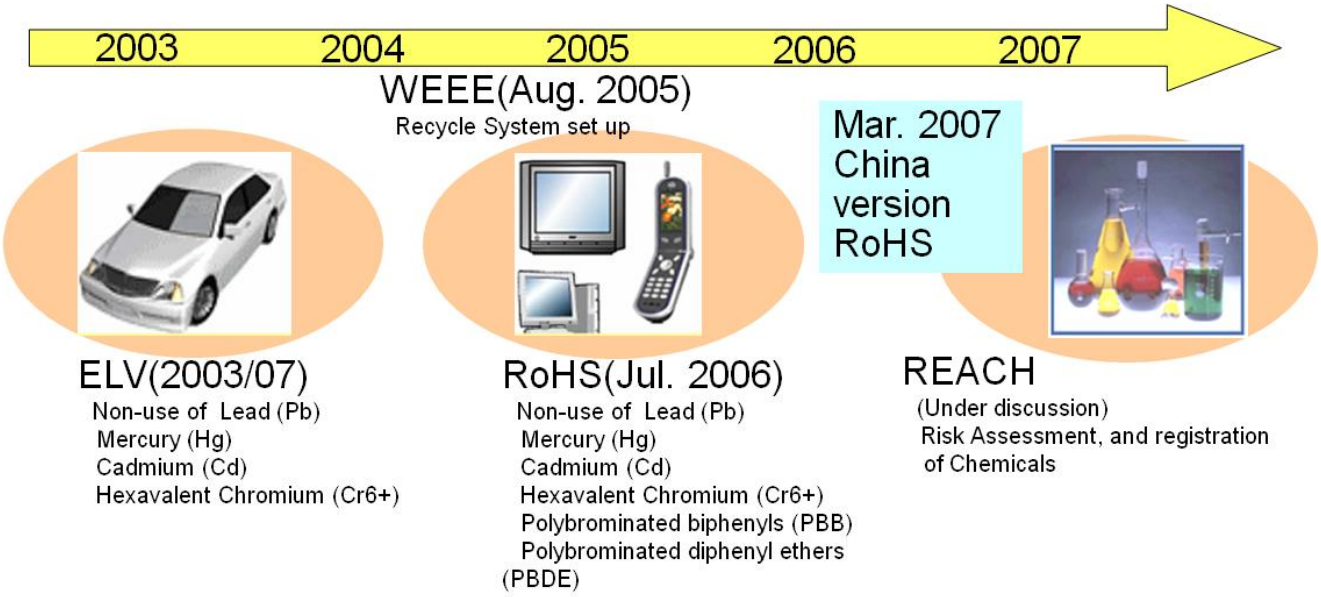

Figure 36: The history of environmental regulation for the electronics industry

There are several regulatory activities resulting from environmental considerations that will impact the future SiP technology as well as all other parts of the electronics industry. These include:

ELV:	Directive on end-of life vehicles
RoHS:	Directive on the restriction of the use of certain hazardous substances in electrical and electric equipment
WEEE:	Directive on waste electrical and electronic equipment
EuP:	Directive on the eco-design of Energy-using Products
REACH:	Registration, Evaluation and Authorization of Chemicals

22. Infrastructure Issues

System in package technology merges the surface mount technology of the EMS industry with the semiconductor assembly and test technologies of the semiconductor assembly services (SAS) industry. This convergence thrusts surface mount technology (SMT) and bare die assembly technologies together in a single factory, which poses several challenges and raises critical infrastructure issues that must be addressed. The two groups (EMS and SAT) have different business models as well as different requirements, specifications, equipment and skill sets.

To hit reasonable profit levels, the SAS companies target gross margins in the 20% range while the EMS companies target gross margins in the 10% range. The difference in these operating models is due to differences in factory overhead (clean room vs. standard manufacturing), R&D equipment and labor cost. For SiP, manufacturing companies must develop a new operating model which mixes the SAT and EMS structures. This model must also be able to support the industry target of a 15% reduction in product cost per year to maintain competitiveness

In addition, EMS and SAT operations do not follow the same quality and reliability specifications. EMS providers use IPC board mount specifications while the SAT providers use JEDEC component specifications. This can create some major differences, depending where the SiPs are built and what is needed for the end market requirements.

Skill set is another big issue. The mixed technology skills required for SiPs are not readily available and require taking specialists from different areas and combining their skills. Typically, a company has to hire one or the other skill set, and then train the individual, which is a two-year process. The industry will need to develop better SiP training forums to help resolve this issue.

23. Innovation needed for SiP market success

SiP has become the package of choice for a number of high volume consumer products and progress is accelerating in SiP technologies. Continued innovation is necessary for SiP to enable the cost effective equivalent scaling that is the under pinning of the “More than Moore” concept. At the outset this will require chip/package¥system co-design (see section 13) tools that are not yet available. A list of some of the other important areas for innovation is presented below.

- TSV processing and models
- Direct bonding die to die, wafer to wafer, die to wafer
- Handling and assembly of thinned die
- Singulation of bonded wafers
- Stress associated with thinning, TSV, etc. and its impact on device performance
- Via filling technology for TSV (including materials)
- New materials:
  - High K dielectrics
  - Low K dielectrics for thin films
  - High Q inductors
  - Low stress molding compounds
- Combined optical/electric interconnect
- Thermal management including active cooling, laminating cooling element into 3D stack, new materials
- Testing and test access (including optical components).

24. Consortia/Research Institutes

A number of consortia addressing the need for innovation in packaging exist. In this section, we summarize some of the consortia activities in table format.

Table 8: Consortia and research institutes in SiP and SiP related technology

Consortium	Headquarters (Date Formed)	Website	Areas of Interest
CALCE (Center for Advanced Life Cycle Engineering)	University of Maryland, University park, Md (1983)	www.calce.umd.edu	Strategies for Risk Assessment, Mitigation and Management of electronic products and systems -Physics of Failure, Failure Mechanisms and Material Behavior -Design for Reliability and Virtual Qualification -Accelerated Testing, Screening and Quality Assurance -Diagnostic and Prognostic Health Management (failure precursors, stress sensors, condition-based prognostics in semiconductors, components and assemblies) -Supply Chain Assessment and Management (Electronic part obsolescence forecasting and management) -Life Cycle Risk, Cost Analysis and Management (Maintenance, refresh and sustainability planning, cost modeling)
EPACK Lab/CAMP (Electronic Packaging Laboratory/Center for Advanced Microsystems Packaging)	Hong Kong University of Science & Technology (1997)	www.ust.hk/epack-lab	R&D, technical training and industrial services in the following areas: - wafer bumping and flip chip technologies - wafer level and chip scale packaging - through silicon vias and 3D packaging - LED packaging for solid state lighting - silicon bench for passive alignment of optical fibers - lead-free soldering and solder joint reliability computational modeling and simulation
Fraunhofer IZM (Fraunhofer Institute for Reliability and Microintegration)	Berlin, Germany (Headquarters)	www.izm.fhg.de	Non-profit scientific institute for applied research. Areas of interest revolve around: - Packaging and system integration technologies, - Micro Reliability and Lifetime Estimation - Wafer Level System Packaging - 3D System Integration - Thermal Management - RF & Wireless - Photonic Packaging - Large Area Electronics - MEMS Packaging - - Sustainable Technical Development
Fraunhofer IWMH (Fraunhofer Institute for Mechanics of Materials at Halle)		*www.iwmh.fraunhofer.de*	- Failure detection and analysis - Metal physics

HDPUG (High Density Packaging Users Group)	Arizona	www.hdpug.org	Projects include: -Power Cycling/Temperature Cycling Correlation -Flip Chip Reliability Characterization -Flip Chip Reliability Characterization -Lead Free Soldering -Low Temperature Lead Free Soldering -Wafer Scale CSP Reliability -Advanced Flip Chip -Optical Workgroup
IEEC	Binghamton University, NY (1984)	www.ieec.binghamton.edu/ieec/	New York State Center for Advanced Technology Areas of research interest include: -Electrical/Thermal/Mechanical analysis and measurements - Novel materials for packaging - 3D stacked systems - Small Scale Systems Integration and Packaging - Reliability and failure analysis - Roll-to-roll flexible electronics - Product tear down analysis
IFC (Interconnect Focus Center)	Atlanta, Georgia (1998)	www.ifc.gatech.edu	Multi-university research effort addressing long-term exploratory research into the interconnect problems. Headquartered on Georgia Tech campus Research interests include electrical and optical interconnects, thermal dissipation and power management, and circuit and system design and modeling
IME	Singapore (1991)	www.ime.a-star.edu.sg	Non-profit R & D organization established by Agency of Science Technology and Research (ASTAR) focuses on upstream research areas in microelectronics. Three core laboratories: Semiconductor Process Technologies Laboratory Micro system, Modules and Components Laboratory Integrated Circuits & Systems Laboratory Focused research programs in - Silicon Photonics - Nano electronics - Bioelectronics and Biomedical - MEMS & NEMS technology - RF & Wireless systems
IMEC (Interuniversity Microelectronics Centre)	Leuven, Belgium (1984)	www.imec.be	Independent research center IMEC aims to bridge gap between fundamental research at universities and technology development in industry Area of interest include: -CMOS and post-CMOS nano-electronics -Solar cells -Advanced packaging and interconnection technologies -Bioelectronics and organic electronics -RF devices and technology
ITRI (Industrial Technology Research Institute)	Hsin Chu, Taiwan (1973)	www.itri.org.tw	Non-profit R&D organization established by the Ministry of Economic Affairs Six core laboratories and research interests: -Communication and Optoelectronics -Precision Machinery and MEMS -Materials and Chemical Engineering -Biomedical Technology -Sustainable Development -Nanotechnology
JIEP (Japan Institute of	Japan	www.e-JISSO.jp	Material for 3D assembly CAE research for JISSO system

Electronics Packaging)			-EMC modeling -Extremely high frequency board design -Noise reduction -PWB fabrication -Micro and nano fabrication -EPADs -Next generation circuit board research -Evaluation method for ion migration -Tin whisker -Advanced JISSO technology -DFT -Optoelectronics JISSO technology -Environmentally friendly JISSO technology -Nano-bio device JISSO technology -Semiconductor packaging
KAIST (Korea Advanced Institute of Science and Technology)	South Korea (1971)	www.kaist.edu	The Center for Electronic Packaging Materials (CEPM) at KAIST (Korea Advanced Institute of Science and Technology) addresses advanced electronic packaging materials, processing technologies, design and reliability of electronic systems. CEPM's main thrust is research and development of the electronic packaging technologies with emphasis on the packaging materials. Their fields of study include Materials Science & Engineering, Mechanical Engineering, Chemical Engineering, and Electrical Engineering.
LETI (Laboratoire d'électronique et de technologie de l'information)	Grenoble, France	www-leti.cea.fr	A CEA (French Atomic Energy Commission) Research lab Areas of interest include: Micro and nano-technologies for electronics and bio Technologies, design and integration of microsystems Imagery technologies Communication technologies and nomad objects
PRC (Packaging Research Center)	Atlanta, GA (1994)	www.prc.gatech.edu	University-industry consortium Headquarter located on Georgia Tech campus Research interests revolve around developing System-on-Package technologies relating to mixed signal design, test, materials, processes, assembly, thermal and reliability
SEMATECH (Semiconductor Manufacturing Technology)	Austin, Texas (1987)	www.sematech.org	Share risks, and increase productivity. Research interests include lithography, materials and processes, manufacturing, 3D interconnects, and workforce development share risks, and increase productivity. Research interests include lithography, materials and processes, manufacturing, 3D interconnects, and workforce development
SRC (Semiconductor Research Corporation)	Durham, NC (1981)	www.src.org	-US semiconductor industry university research management consortium with objectives of solving the technical challenges facing the semiconductor industry and developing technical talent for its member companies -Research interests span short and long term research as well as span from front-end devices to system level issues

25. Summary

The pace of development in packaging is in general and System in Package is faster today than at any other time in history. Innovation is present from the package design and simulation tools through the entire process to the test technology for finished products. The economic benefits of functional diversification and system level integration at the package level will inevitably drive increased investment in SiP. This is evident from the increased number of publications, the rapid expansion in the number of package types, the rise of many Consortia focused on this area of the electronics industry. One result of this shift in investment and development focus toward a greater concentration on package innovation is that this document will be quickly outdated.

It is our intent to periodically update this paper to reflect major changes so that it can be a useful, up to date guide for system level integration at the package level.

We would like to ask the readers of this paper to send any suggestions and/or corrections to bill_bottoms@3mts.com. This will assist us in keeping the document up to date and accurate so that it can be a continuing reference to the state of the art in SiP and a guide to developments critical to meeting future market requirements.

26. List of Tables

27. List of Figures

28. Abbreviations

ACE: *Automatic Compact model Extraction (Automated design tool)*

BEOL: *Back end of the line (formation of interconnects in IC fabrication)*

BER: *Bit error rate*

BGA: *Ball grid array package*

BIST: *Built in self test (the use of on chip transistors to test a device)*

CFD: *Computational fluid dynamics*

CNT: *Carbon nanotubes*

CSP: *Chip size package*

CTE: *Coefficient of thermal expansion*

CVD: *Chemical vapor deposition*

DA: *Die attach*

DAF: *Die attach film (die attach is often employed in a film format)*

DBG: *Dice before grind (process flow with singulation before grinding)*

DFT: *Design for test (methodology with test strategy addressed at design)*

DRC: *Design rule check*

ECU: *Engine controller unit (a term used in automotive electronics)*

EM: *Electromagnetic*

EMC: *Electromagnetic coupling*

EMI: *Electromagnetic interference*

EMS: *Electronic manufacturing services*

EP: *Embedded passives*

EuP: *Energy using products (definition used in environmental regulation)*

eWLB: *Embedded wafer level ball grid array*

FBGA: *Fine pitch Ball grid array*

FC: *Flip chip*

FT: *Final test*

IDM: *Independent device manufacturer*

ILD: *Inter-layer dielectric*

IPD: *Integrated passive device*

KGD: *Known good die*

MAP: *Mold array package*

MAPBGA: *Mold array ball grid array package*

MAPPoP: *Mold array PoP*

MCP: *Multi chip package*

MEMS: *Microelectromechanical systems*

PCB: *Printed circuit board*

PCMCIA: *Personal computer memory card international association*

PD: *Photo detector*

PoP: *Package on package*

PWB: *Printed wiring board*

QFN: *Quad Flat No leads package*

RDL: ***R****edistribution layer*

RIE: *Reactive ion etching*

RoHS: *Restriction of the use of certain hazardous substances*

SAS: *Semiconductor assembly services*

SAT: *Semiconductor assembly and test*

SiP: *System in a package*

SMD: *Surface mount device*

SMT: *Surface mount*

SoC: *System on a chip*

SoP: *Solder on pad*

TCMG: *Top center mold gate*

TIM: *Thermal interface material*

T_{J}_max: *Maximum junction temperature*

TSV: *Through silicon via*

UBM: *Under bump metal*

ULK: *Ultra low k (interlayer dielectric I with dielectric constant below 2.4)*

USB: *Universal serial bus*

WEEE: *Waste electrical and electronic equipment*

WLP: *Wafer level Packaging*

29. Acknowledgements

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W. R. Bottoms

Editors:

William Chen	ASE
W. R. Bottoms	3MTS
Klaus Pressel	Infineon
Juergen Wolf	Fraunhofer

Contributors:

Bernd K. Appelt, Ph.D., ASE (Europe) Inc.

Bob Chylak, Kulicke & Soffa Industries Inc.

Carl Chen, Silicon Precision Industries Co., Ltd.

Charles Reynolds, IBM

Chetan Desai, Fluent Inc

.

Chi- Shi Chang, Ph.D., SMSmicro

Clinton Chao, Ph.D., Taiwan Semiconductor Manufacturing Company, Ltd.

Coen Tak, NXP

Darvin Edwards, Texas Instruments Inc.

Debendra Mallik, Intel Corporation

Dongho Lee, Ph.D., Samsung Electronics Co., Ltd.

Dr. Klaus Pressel, Infineon Technologies

Eiji Yoshida, Fujitsu

Eric Beyne, IMEC

Futawatari, Oki

Gary Morrison, Texas Instruments Inc.

George G. Harman, National Institute of Standards and Technology

Gilles Poupon, Laboratoire d' electronique et de technologie de l'information

Gottfried Beer, Infineon Technologies AG

HeeSoo Lee, Agilent Technologies

Henry U. Utsunomiya, Interconnection Technologies, Inc.

Hirofumi Nakajima, NEC Electronics Corporation

Hongwei Liang, Texas Instruments Inc.

Hosack, Harold, SRC

Jie Xue, Ph. D., Cisco

Joseph M. Adam, WiSPRY, Inc.

Jurgen Wolf, Fraunhofer IZM

Katarina Boustedt, Ericsson

Kazuo Nishiyama, Sony

Keith Newman, Sun Microsystems

Kishor Desai, LSI Logic Corporation

Kubo Takanori, Kyocera Corporation

Lawrence Williams, Ansoft Corp.

Lei Mercado, Medtronics

Luu T. Nguyen, Ph.D., National Semiconductor Corporation

Mahadevan K. Iyer, Ph.D., Institute of Microelectronics of Singapore

Manoj Nagulapally, Fluent Inc.

Marc Petersen, Agilent Technologies

Mario Bolanos-Avila, Texas Instruments Incorporated

Masashi Otsuka, Toshiba Corporation Semiconductor Company

Matthias Petzold, Fraunhofer IWM Halle

Michitaka Kimura, Renesas Technology Corporation

Mike Hung, Ph.D., ASE Group Kaoshiung

Muhannad S. Bakir, Ph.D., Georgia Institute of Technology

Peter Caldera, Infineon Technologies Austria AG

Richard F. Otte, Promex Industries Inc.

Robert C. Pfahl, Jr., Ph.D., INEMI

Rong-Shen Lee, Industrial Technology Research Institute

Ryo Haruta, Renesas Technology Corporation

Shigeyuki Ueda , LSI Rohm Co.

Shoji Uegaki, ASE Marketing & Service Japan Co., Ltd.

Shuhya Haruguchi, Sharp Corporation

Stan Mihelcic, eASIC

W.R. Bottoms, Ph.D., Third Millennium Test Solutions

William T. Chen, Ph.D., ASE (US) Inc.

Zhiping Yang, Ph.D., Cisco Systems, Inc.