Volume 12 Issue 02 Published June 17, 2008 ISSN 1535-864X DOI: 10.1535/itj.1202.06

Intel's 45nm CMOS Technology

45nm Transistor Reliability

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45nm Transistor Reliability

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Index words: 45nm, High-K + Metal Gate, Bias Temperature Instability, Time Dependent Dielectric Breakdown (TDDB)

ABSTRACT

It has been clear for a number of years that increasing transistor gate leakage with device scaling would ultimately necessitate an alternative to traditional SiON dielectrics with polysilicon gates. Material systems providing higher dielectric constants, and therefore allowing physically thicker dielectrics, have been the object of extensive research. Such high-k dielectrics, when combined with metal gate electrodes, have emerged as the leading alternative, demonstrating good transistor performance and offering reductions in gate leakage of 25X-100X. Achieving the required reliability, particularly at the high operating electric fields at which the performance advantages are realized, however, proved much more difficult.

Intel strove to overcome the reliability obstacles by introducing high-k dielectrics combined with metal gate electrodes (HK+MG) transistors in its 45nm logic process, as it judged the transition to this technology would provide compelling performance advantages. In this paper we discuss the general considerations for the reliability of HK+MG transistors and specifically we discuss what was achieved with Intel's 45nm process technology.

A particularly extensive effort was undertaken to characterize the reliability physics of this revolutionary new transistor and to gather the data to ensure accurate modeling of failure rates. This entailed accelerated testing and fully integrated test vehicles, representing over seven orders of magnitude in the transistor area, at a variety of stress conditions, some of which lasted over three months.

The intrinsic transistor reliability fail modes addressed in this paper fall into two basic classes. First we have the integrity of the transistor dielectric itself, which in the course of operation, can fail, a phenomenon typically referred to as Time Dependent Dielectric Breakdown (TDDB). The transistor must be engineered to ensure that components don't wear out within their operating lifetimes.

Second, in addition to abrupt failure of the dielectric, transistors can also experience progressive parametric degradation. The primary parametric reliability mode for traditional SiON-based transistors is a slowdown of the PMOS devices due to progressive trapping of charge, typically referred to as Bias Temp Instability (BTI). For HK-based dielectrics, at their higher target operating fields, similar degradation is observed on NMOS transistors as well as potentially significant increases in gate leakage with stress, known as Stress Induced Leakage Current (SILC).

We discuss these reliability phenomena and illustrate that while they pose large reliability challenges for HK+MG, these challenges can be overcome through refinement of process architecture and optimization of processing conditions. Intel's 45nm technology is shown to achieve intrinsic TDDB and aggregate (N+P) BTI performance equivalent to its 65nm predecessor with negligible SILC at its 30% higher operating electric fields.

PROCESS BACKGROUND

The 45nm high-k dielectrics combined with metal gate electrodes (HK+MG) transistors studied in this work have a Hafnium-based gate dielectric and dual workfunction

metal gate electrodes for NMOS and PMOS. The transistor fabrication utilizes a HK first and MG last process as detailed in [1]. In this flow, HK is deposited using an Atomic Layer Deposition (ALD) process, and polysilicon is used for the gate patterning. After the Interconnect Dielectric deposition, a polish step exposes poly gates, and the dummy poly is removed. Then, workfunction metal electrodes are deposited followed by a gate fill process. The SiO_2 equivalent oxide thickness (EOT) of the HK plus the Interface Layer (IL) that forms between the HK and the silicon is ~1.0nm. Figure 1 describes the gate stack, with its SiO_2-like interface layer (IL) and the HK dielectric proper.

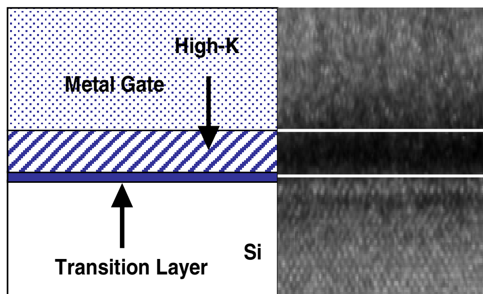
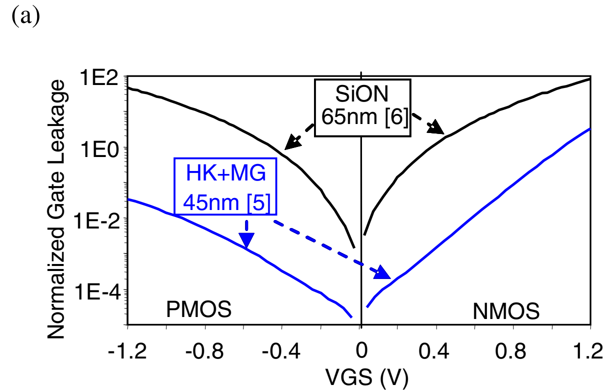


Figure 1: TEM of High-K and Metal gate (HK+MG) transistor stack

Figure 2(a) shows the typical gate leakage behavior of these 45nm HK+MG transistors measured in inversion, compared to that of 65nm Poly/SiON transistors [2]. Substantial reduction (25-1000X) is achieved with the physically thicker HK film employed while still enabling inversion Tox scaling consistent with the historical trend of ~0.7X per technology generation. Figure 2(b) shows the appropriate band diagrams for these HK+MG transistors. Lower inversion gate leakage current on the HK+MG PMOS is due to the larger band offset than for the NMOS (as indicated by the direction of arrows of the tunneling current).

(a)



(b)

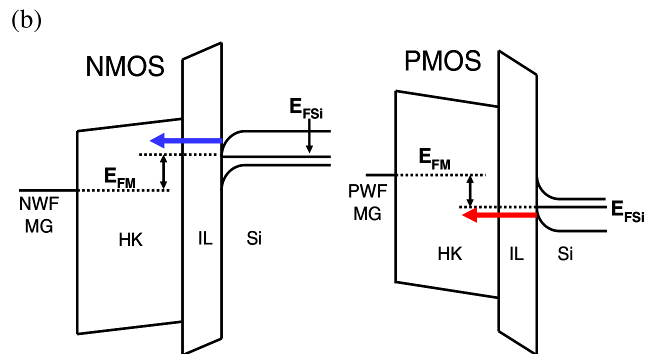


Figure 2: (a) 45nm HK+MG leakage comparison to that of 65nm Poly/SiON transistors. HK+MG process enables 25-1000X gate leakage reduction. (b) Band diagrams of HK+MG transistors.

Despite the reduced gate leakage current due to use of physically thicker HK dielectric, the effective E-field in the operating regime increases substantially (~30%). Figure 3 shows the gate dielectric E-field vs. technology node. The increase in the E-field provides higher transistor performance, but this must be achieved with no degradation in reliability.

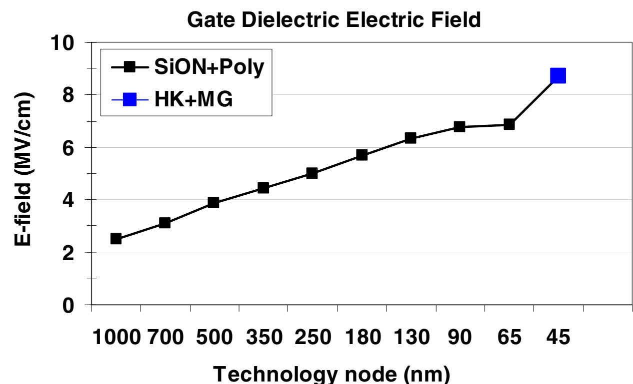


Figure 3: Gate Electric field increase vs. technology nodes. The average E-field for the 45nm technology is 30% higher than in the 65nm generation.

The large increase in E-field with HK+MG contributes to the reliability challenges of this major technology transition. In the next section we provide background on the key reliability mechanisms that need to be considered in this transition.

TRANSISTOR RELIABILITY FUNDAMENTALS

Transistor Bias Temperature Instability (BTI) Degradation

When subject to operating bias, transistors exhibit changes in transistor characteristics over time, an effect termed Bias Temperature Instability or BTI. Typically, transistor thresholds $|(V_T)|$ increase, and other electrical parameters, such as drive current (I_D) and transconductance (G_m), are also affected. At typical operating fields of SiO_2 transistors, BTI is only significant for PMOS transistors with negative gate bias (NBTI).

BTI results from the creation of both interface states (D_{it}) and oxide trapped charges (D_{ot}), and the mechanism is accelerated by both voltage and temperature. As the name implies, the PMOS channel must be inverted for NBTI to occur. NBTI degradation does not require a large amount of tunneling current and can be significant even at a very low bias. Characterization of true NBTI degradation is very challenging, due to the recovery of trapping that occurs in stress upon removal of the bias. Several fast measurement techniques have been developed to minimize the recovery influence including On-The-Fly (OTF) measurements, Ultra-fast V_T measurements on the order of micro-seconds, and Pulse-IV measurements [3, 4].

Figure 4 shows a diagram of a typical PMOS NBTI degradation and recovery process well reported in the literature. There is no consensus on the exact physical mechanism, but one of the leading models for PMOS NBTI recovery is the back diffusion of Hydrogen near the substrate/dielectric interface [5].

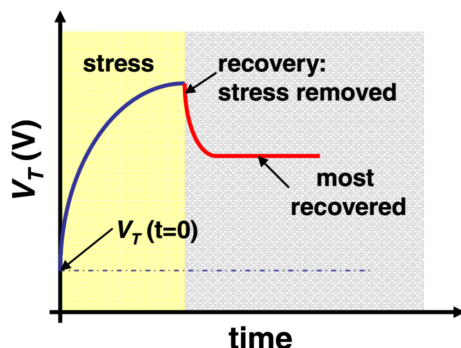


Figure 4: PMOS NBTI vs. Time illustrating both degradation and recovery

PMOS NBTI is recognized in the industry as a major reliability mechanism in advanced logic technologies. Degradation of maximum operating Frequency (Fmax) and circuit margin, in particular at Minimum Operating Voltage (Vmin), must be addressed within product design and testing to ensure an adequate margin to specifications over operating lifetimes.

A particularly important circuit case is SRAM memory. Transistors within the SRAM cells are typically amongst the smallest within a technology, and the SRAM Static Noise Margin (SNM) is highly sensitive to device mismatch. The scaling of SRAM memory arrays has increased the sensitivity to NBTI-induced transistor V_T mismatch, which can degrade Vmin characteristics over time. 6T SRAM cell area has traditionally reduced 2X every two years, as shown in Figure 5, which means bit counts are also increasing at a corresponding rate. In addition to design and layout approaches to improve Vmin margin, error correction techniques are often leveraged in cache designs [6].

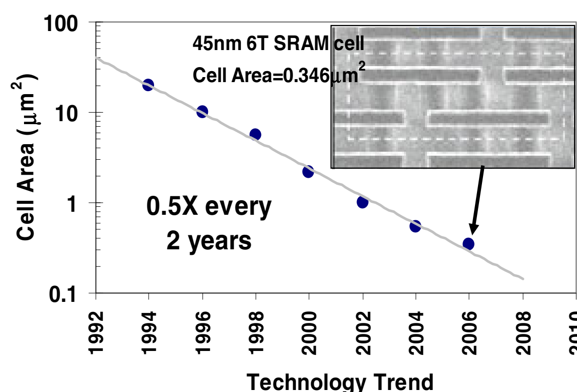


Figure 5: 6T SRAM cell size scaling trend showing 2X cell area scaling every two years [7]

Figure 6 shows an example of Vmin dependence on the SRAM cache array size. Both the magnitude of Vmin and the Vmin spread increase with cache array size due to transistor variations. Thus, understanding device variability at both time 0 and over time, given BTI effects, has become increasingly important with cache cell/array size scaling.

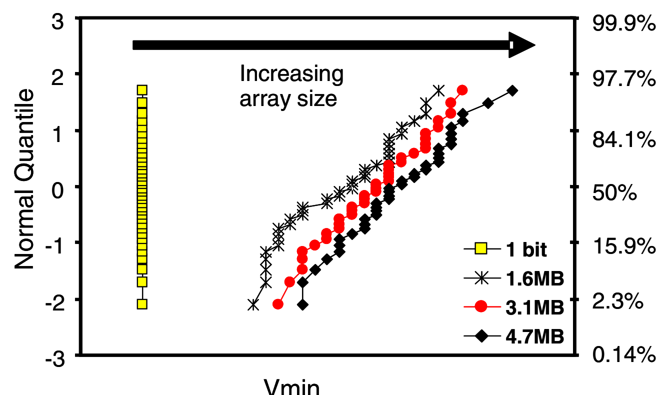


Figure 6: Vmin dependence on cache array size for 6-T SRAM [7]. Transistor aging due to PMOS NBTI will further degrade Vmin characteristics.

PMOS NBTI remains a key concern of HK+MG CMOS transistors, and at the higher operating fields of these transistors compared to SiO_2, NMOS BTI degradation under inversion (PBTI) can also be significant [8]. Unacceptably high levels of BTI degradation for HK+MG on both NMOS and PMOS have been reported. In addition, fast charge trapping/de-trapping has also been reported on HK materials, which complicates characterization and calls the validity of conventional DC stress into question. BTI reliability degradation has been shown to be modulated by processing and integration changes such as thermal treatments, adding dopants, and nitridation techniques [9, 10]. Better charge trapping properties and improved reliability results on transistors fabricated with HK silicate dielectrics rather than HK oxides have also been reported [11].

Extensive BTI experimental data collection was undertaken in the development of Intel's 45nm HK+MG transistor technology to support reliability modeling and process optimization work. A summary of these results and a discussion of the mechanisms responsible for BTI in HK+MG transistors are presented below. We demonstrate that, with appropriate transistor architecture and processing, net BTI degradation that is comparable to, or better than, that observed with traditional SiON dielectrics, can be achieved for HK+MG dielectrics operating at ~30% higher E-fields. The optimized HK film stack used in Intel's 45nm HK+MG process also shows negligible hysteresis and transient trapping associated with fast carriers.

Gate Dielectric Breakdown, Time-Dependent Dielectric Breakdown (TDDB) and Stress-Induced Leakage Current (SILC)

The transistor gate dielectric provides isolation of the gate electrode from the conducting channel, providing the high input impedance of CMOS transistors. The reliability of the gate is, therefore, of primary importance in transistor reliability. Multiple evaluation techniques exist for assessment of gate dielectric integrity, with Time Dependent Dielectric Breakdown (TDDB) testing being the standard methodology for developing operating lifetime reliability projections. TDDB characterization is performed with elevated voltage and temperature, with either constant voltage (CVS) or constant current (CCS) on transistors or capacitors, until a failure is observed. Failure is typically based on an increase in gate current Ig, but definitions vary and can significantly impact projections.

TDDB can occur on NMOS and PMOS under all operating bias conditions (inversion, accumulation); however, the rate of dielectric damage is very strongly modulated by the band structure of the material system and, traditionally, NMOS in inversion mode tends to be the limiter for TDDB lifetime.

Although there is no rigid consensus in the literature on the exact physical mechanisms that dominate gate dielectric breakdown, it is generally attributed to a combination of several mechanisms—charge injection, interface, bulk trap state generation, and trap-assisted conduction. During operation, the electric field across the gate dielectric causes the generation of electrical defects or "traps." These traps modify the local electric field and enhance leakage current in the dielectric through various hopping and tunneling processes. With cumulative stress, more trap states are created and, consequently, a gradual increase of the gate current is observed: this is known as Stress Induced Leakage Current (SILC) degradation. Eventually, a point is reached where a conductive "chain" of traps is established between the cathode and the anode as depicted in Figure 7. The statistical theory that describes this process is called the Percolation Theory [12]. The completion of this chain results in a large increase in current flow and potentially collateral damage to the device, which may critically impact the circuit.

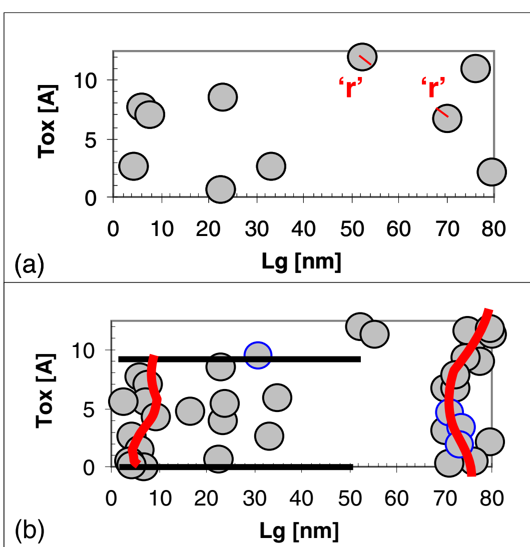


Figure 7: Percolation Theory describes traps as spheres of radius "r. When several of them form a complete chain from anode to cathode, breakdown (BD) occurs. The thinner the dielectric, the fewer the traps needed to cause BD [12].

The use of HK+MG stacks to overcome scaling limitations of conventional SiO_2 dielectrics introduces additional complexities in the form of materials, band structure, and interfaces that can significantly impact the TDDB mechanics and performance. Problematic HK dielectric lifetimes, SILC degradation, and interface and bulk-trap densities have been reported extensively in the literature [13, 14], and these issues need to be overcome to match the high reliability standards that have been established with conventional dielectrics.

Unless specified otherwise, TDDB stresses reported in this work were carried out with DC CVS. Monitoring of the gate leakage was performed by interrupting the stress with negligible measurement delay between stress and measurement. Care was taken to ensure that the measurement phase did not result in additional trap creation or degradation. The monitor measurements were conducted at two bias conditions corresponding to nominal and low voltage of operating conditions of products. The results focus on reliability of the optimized process flow, referred to as *Final,* but the affects of process optimizations are illustrated with results of material from early unoptimized process architectures and flows, referred to as *Initial.* Results for Intel's 65nm process are also referenced as benchmarks for mature ultra-thin SiON+PolySi devices [2].

The devices evaluated in this work are single transistors as well as arrays of transistors tied together electrically in parallel to generate large gate area structures with realistic transistor-like layouts. Each leg of the transistor arrays has a drawn gate length of 40nm while the electrical length is much smaller. The SRAM cache data reported here were collected on a fully integrated 4.5Mbit cache array. Acceleration factors were extracted through such testing to understand the sensitivity of the TDDB lifetimes to voltage and temperature. To minimize the extrapolation uncertainties in TDDB models, large sample sizes were accumulated at multiple stress condition combinations on test structures with a gate area range of over seven decades.

It will be demonstrated that, with an optimized transistor architecture and process flow, dielectric reliability comparable to that obtained on traditional SiON dielectrics can be achieved for HK+MG dielectrics operating at ~30% higher E-fields with negligible SILC prior to breakdown.

In Process Charging

It is well understood in the industry that dielectric quality as well as transistor parametric characteristics can be degraded due to process-charging induced damage from plasma processes within the fabrication flow. The charge that may accumulate on interconnect 'antennae' connected to transistor gates in the course of these processes can result in sufficiently high stress to induce unrecoverable changes to the transistor characteristics, or in extreme cases, even catastrophic device damage. The standard approach to protect against such plasma-induced damage is to provide a discharge path in the form of diodes or transistors. The protection needs are a function of the specific antennae connected to a device as well as the intrinsic leakage of the transistor and the charging characteristics of the fabrication processes. Design rules are defined to ensure sufficient protection to prevent any transistor damage during processing.

Process charging is one concern that has benefited from traditional dielectric scaling; increases in gate oxide leakage have made ultra thin SiO_2 dielectrics less susceptible to damage. With the large reduction in gate leakage that HK dielectrics provide, the charging rules must therefore be tightened to more historical levels.

RESULTS

Introduction to Reliability Results

The results of reliability characterizations of Intel's 45nm HK+MG process are presented below. The first two sections address degradation of the gate dielectric considering progressive increases in leakage current or SILC and dielectric breakdown. The third section considers degradation in transistor operating characteristics due to charge trapping within the bulk of

the dielectric or at interfaces within the stack. The results reported here are for devices with the process minimum ‘drawn’ channel lengths of ~40nm, but devices spanning the permitted layout range were evaluated with similar results. Unless stated otherwise, the data below are for devices on the optimized 45nm HK+MG process flow. Some results from 45nm development process flows as well as for a mature 65nm process are shown for comparative purposes.

Dielectric Reliability

Transistor dielectric reliability was assessed for a wide range of transistor structures ranging from single cache bitcell transistors to 4.5Mb SRAM cache test vehicles. Conventional CVS was employed unless otherwise indicated.

Dielectric Reliability—TDDB

TDDB is associated with a substantial increase in current through the transistor dielectric. In the data below, the definition of failure for extraction of TDDB lifetimes is the point where an abrupt increase in dielectric current is observed or a “hard breakdown” (HBD) occurs. This increase in current due to HBD may be sufficient to, but won’t necessarily, result in circuit failure.

Figure 8 compares matched Electric field TDDB on SiON+PolySi vs. the optimized Intel 45nm HK+MG gate [15].

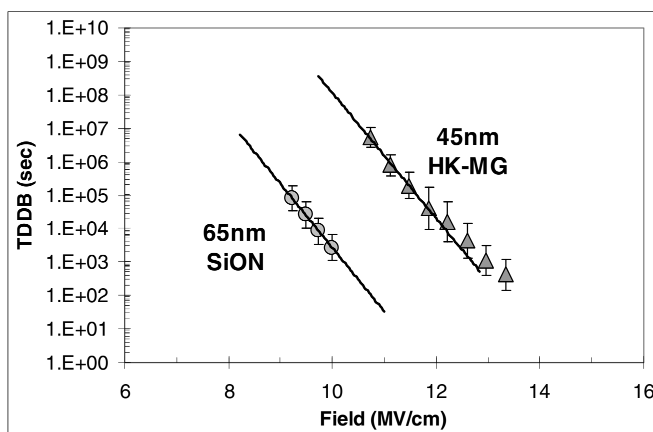


Figure 8: TDDB vs. Electric field comparison of HK+MG [1] and SiON [2] showing that an optimized HK+MG dielectric can support 30% higher field than a mature SiON-based technology at matched TDDB lifetime

Figure 9 shows the median TDDB lifetime data collected on the *Final* optimized process over a much greater range: more than 6 MV/cm and more than seven orders of magnitude in time. Note, the data exhibit a clear transition in the acceleration behavior that occurs at ~12MV/cm.

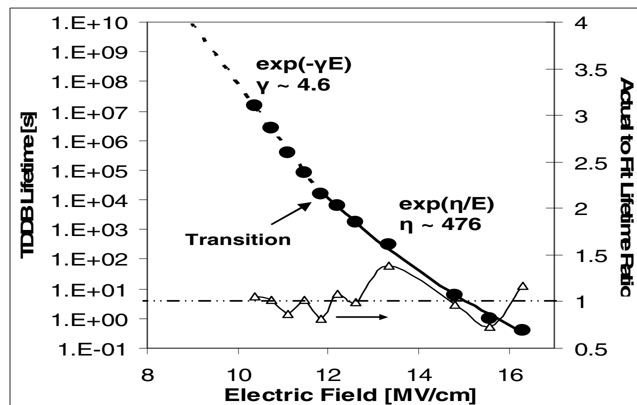


Figure 9: Long-term TDDB measured on the *Final* process flow shows a change in the acceleration slope at ~12MV/cm. Empirical fits to the data show good fitting with fit delta of 1±0.3.

Figure 10 summarizes the scaling of TDDB lifetime with gate area over a range of nearly eight decades. Using a conventional Weibull model, the area-scaling data corresponds to a Beta value of approximately 1.4.

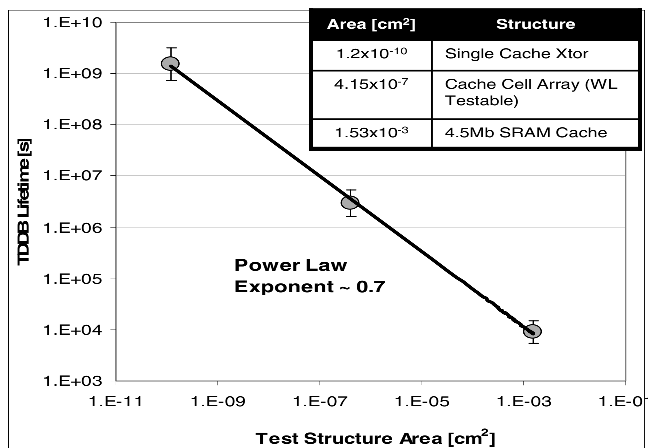


Figure 10: Area scaling of TDDB lifetime measured on single cache bitcell transistors, array cells and 4.5Mb SRAM cache test vehicles demonstrating consistent TDDB scaling with gate area over a range of eight decades

Dielectric Reliability—Stress Induced Leakage (SILC)

Transistor dielectrics can exhibit intrinsic increases in gate leakage prior to dielectric breakdown that may be large enough in aggregate to noticeably degrade the static power of an IC even where there is no impact on circuit functionality or performance. As discussed previously, this SILC effect has been reported to be a major concern for HK dielectrics.

Figure 11 compares early time evolution of Ig under inversion stress of NMOS devices fabricated with an early, unoptimized 45nm HK+MG process flow to that of material from the *Final* optimized process flow and for a conventional SiON stack.

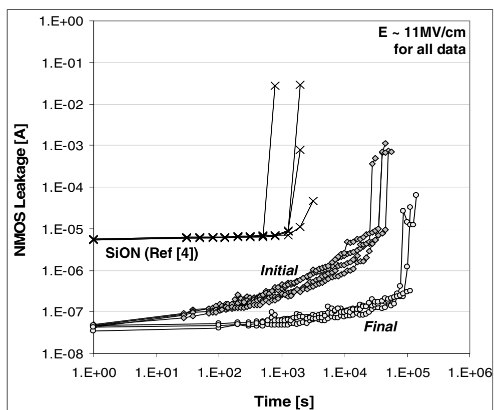


Figure 11. SILC degradation on Initial vs. Final process flows demonstrates improvement through process optimization. The SiO_2 case is shown for reference and exhibits relatively negligible SILC degradation as expected. The Final process exhibits similar levels of SILC degradation as observed on the SiO_2 reference.

Transistor Degradation—Bias Temp Instability (BTI)

Bias Temp Instability (BTI) degradation of 45nm HK+MG transistors was studied over a range of bias and temperature conditions to allow models to be generated and to provide insight into the physical mechanisms and processing interactions.

Unless stated otherwise, the data below are for devices stressed statically (DC) and with fixed delay between completion of stress and device characterization for each stress interval to ensure a consistent level of any recovery due to charge detrapping. During stress, the transistor gates were biased at either positive or negative polarity while all other terminals were grounded. V_T was measured using 50mV on the drain.

The time evolution of degradation in transistor drive (Idsat) for 45nm HK+MG NMOS and PMOS devices at accelerated inversion stress conditions is shown in Figure 12. Both show power law time dependencies: ΔIdsat ~ t^n, with a somewhat lower time slope of .17 observed on the NMOS compared to ~.2 for the PMOS [16].

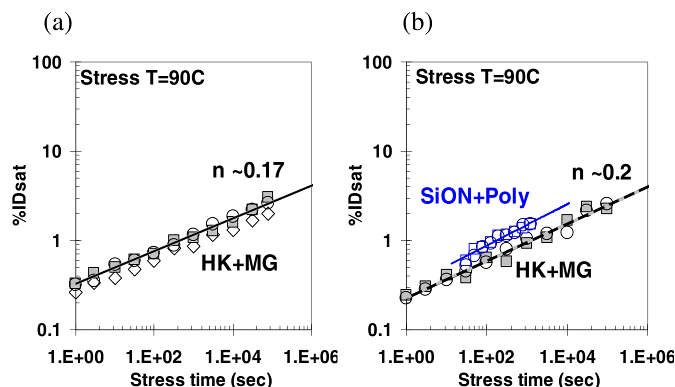


Figure 12: (a) NMOS PBTI time dependence. (b) PMOS NBTI time dependence of HK+MG transistors. Transistors are drawn at W/L=0.9um/0.04um for HK+MG process. Poly/SiON have W/L=1um/0.04um drawn dimensions.

Characterization of transistor degradation under DC stresses over a range of temperatures from 60°C to 110°C shows Arrhenius time dependence as shown in Figure 13:

Time to given TTF(ΔV_T) ~ $e^{Ea/kT}$

with Ea ~ .7eV for PMOS; NMOS shows a lower temperature dependence of ~.46 eV.

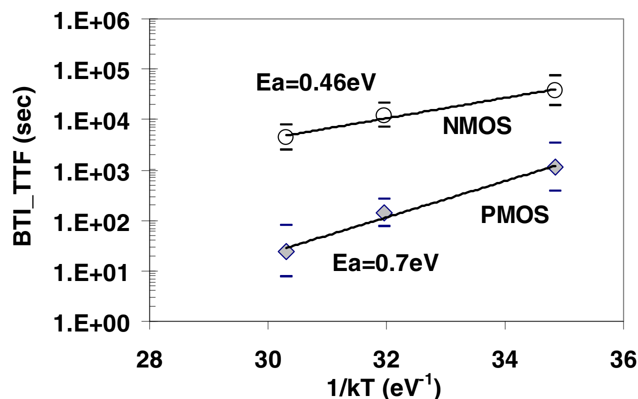


Figure 13: NMOS PBTI and PMOS NBTI activation energy (Ea)

Figures 14 and 15 show the dependence of Bias temp V_T degradation on the applied electrical field for PMOS and NMOS devices, respectively, as well as comparative results for Intel's 65nm SiO_2 technology.

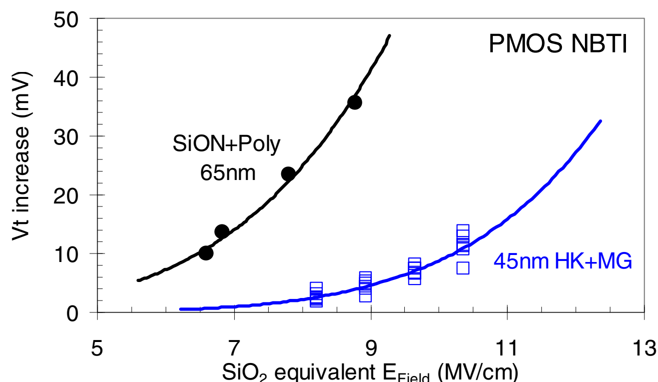


Figure 14: PMOS NBTI V_T shift vs. Electric field

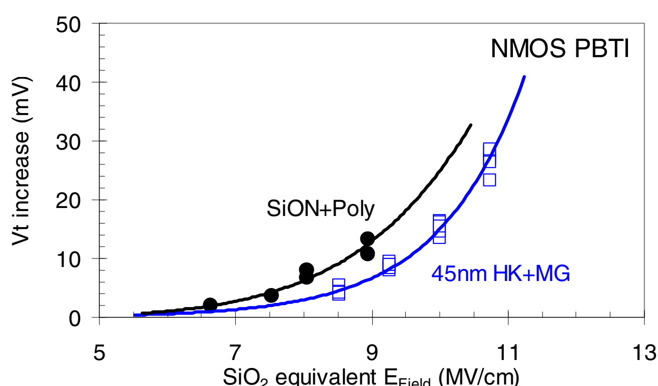


Figure 15: NMOS PBTI V_T shift vs. Electric field

Transistor Tranconductance (G_m) can provide useful insights into the nature of the BTI degradation mechanisms. Figure 16 shows the correlation of degradation in G_m to that of V_T, comparing an un-optimized HK film stack from the early development stage *Initial* and the optimized *Final* process. Note that V_T shift is well correlated to the % G_m degradation for both NMOS and PMOS for the *Initial* HK process, while it only correlates well to the PMOS on the *Final* HK process.

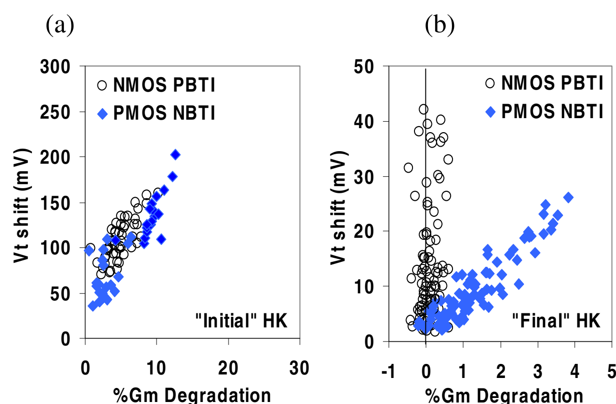
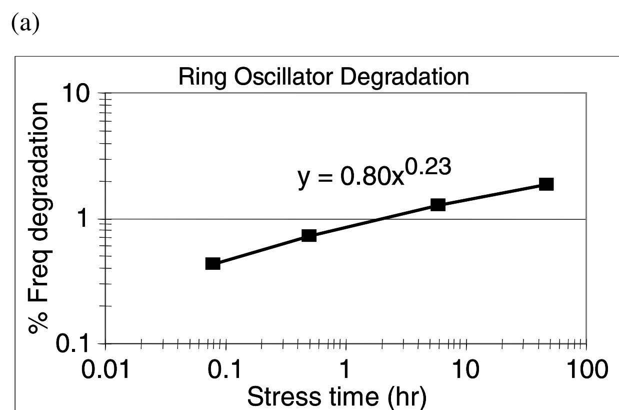


Figure 16: NMOS and PMOS BTI V_T shift vs. % G_m degradation on (a) Initial process vs. (b) Final 45nm HK+MG process.

In addition to discrete transistor test structures, circuits of various complexities are used to validate transistor degradation models. Ring Oscillators (ROs) are particularly useful for validating BTI impact on performance over variations in configuration and layout. Figure 17(a) shows representative 45nm HK+MG RO degradation data with a time slope of ~.2 as expected from device-level BTI. Figure 17(b) shows the RO stress data vs. discrete transistor results showing very good agreement.

(a)



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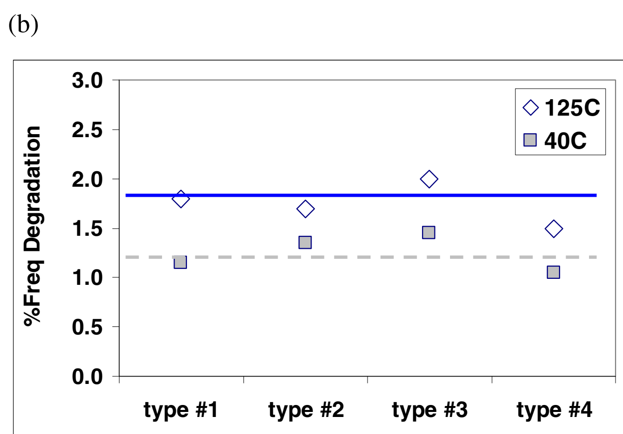


Figure 17: (a) Ring Oscillator (RO) degradation (b) RO stress data against BTI model based on discrete transistors

Transistor Degradation—Fast Traps

Another manifestation of degradation in transistor characteristics due to charge trapping is rapid shifting in device thresholds upon application of bias. This effect is of particular concern for HK dielectrics. Intel's optimized 45nm HK+MG process has negligible fast trapping, but the following comparison to early development process revisions illustrate that this is a potential area of concern: Figure 18 compares NMOS BTI V_T shift over time for the *Initial* and *Final* HK+MG processes. Note the very large, increase in V_T <1 sec. and the relative lack of dependence of V_T degradation on stress voltage for the *Initial* process compared to the mature *Final* process.

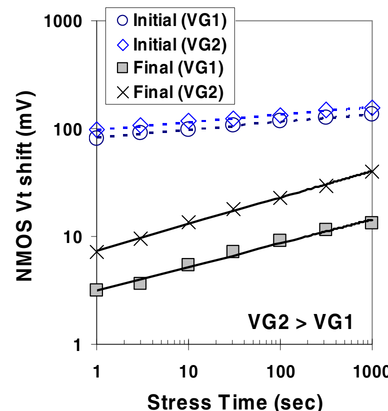


Figure 18: NMOS PBTI V_T shift for Initial and Final HK+MG process

Transistor Degradation—Hot Carrier

Injection of hot carriers can result in degradation in V_T and G_m. The low conduction band offset for Hf-based HK dielectric in contact with a silicon substrate results in a reduced barrier, and it has been suggested in the literature that this poses a potentially increased risk for the hot carrier injection [17]. Figure 19 shows NMOS hot electron reliability comparison between Intel's 45nm HK+MG and 65nm Poly/SiON transistors [2]. The 45nm HK+MG transistors actually show a large improvement in lifetime (>7X at same Isub) relative to 65nm. TTF to impact ionization slope is very similar between the two technologies.

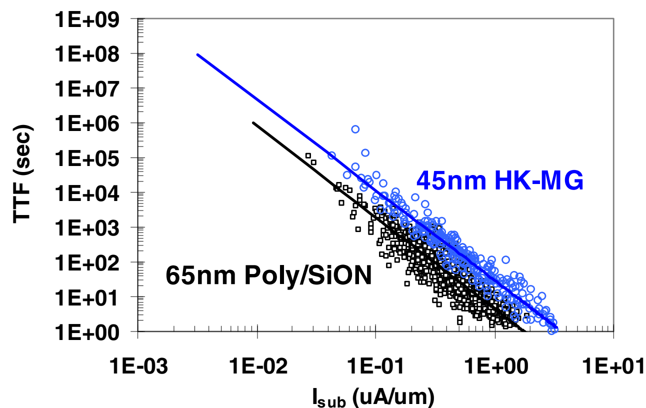


Figure 19: NMOS hot electron performance of 45nm HK+MG and 65nm Poly/SiON transistors

Process Charging

Assessment of process charging damage was conducted using specialized test structures with antennae connected to the gate of 'victim' transistors with varying levels of charging protection. The complete structure set extends beyond that allowed within the process design rules.

Transistor parametric characteristics at the completion of processing are monitored on these structures, and transistor reliability stresses are conducted and compared to reference devices with no antennae. These results confirm no charging degradation on devices compliant to design rule protection requirements.

DISCUSSION

TDDB results show that Intel's 45nm HK+MG transistor delivers equivalent dielectric lifetimes for NMOS devices at a 30% higher electric field. Due to the band offsets, PMOS TDDB has much higher margins. Conventional Gate Oxide (GOX) modeling formulations are largely applicable to these devices; however, the dependence of TTF on the applied electric field is not a constant exponential: the high field regime, above ~12MV/cm, exhibits a shallower acceleration slope. This acceleration factor change is observed to occur at an e-field value similar to the point of transition in gate leakage from a direct tunneling (DT) regime to a Fowler-Nordheim tunneling (FN) regime, as shown in Figure 20.

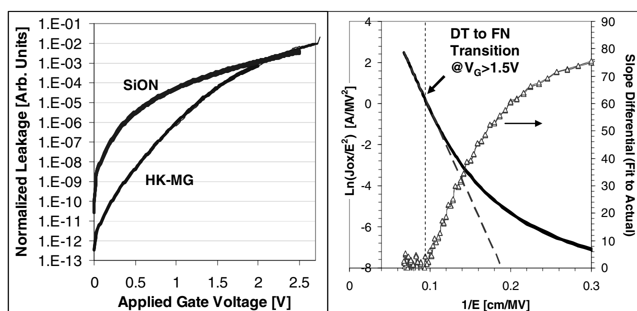


Figure 20. Left plot shows gate leakage vs. bias for HK+MG [1] vs. SiON [2]. At higher V_G values, DT leakage through SiON dominates the net leakage, but at lower biases, leakage through the HK+MG stack drops off rapidly due to DT through the HK layer. Right plot shows DT to FN transition occurs in the HK+MG stack at V_G>1.5V (triangles are delta from fit to actual slope; transition extracted at delta • 0).

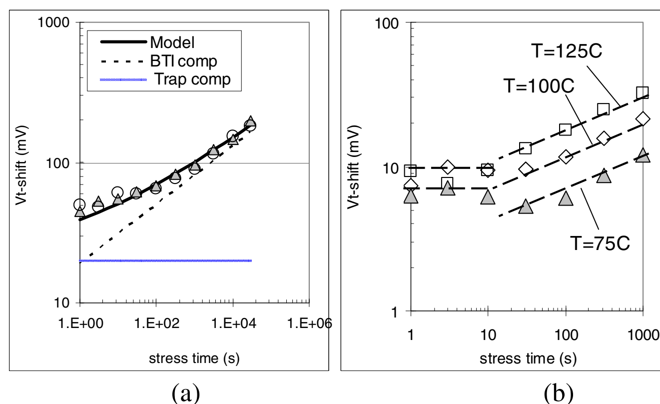
Such a change in the tunneling mechanism is expected for bilayer dielectric stacks and has been predicted for HK+MG by Dunga et al. [18]. At lower biases, direct tunneling through the entire HK+MG stack causes gate fluence to drop rapidly—and Degraeve et al. [19] have used a fluence-driven model to predict a strong increase in TDDB lifetimes at voltages near the operating range. However, very limited data exists in the literature for such low voltage TDDB data on HK+MG stacks. For the Intel HK+MG process, CVS data were collected spanning the low- and high-field regimes—with total stress times exceeding three months duration to provide good resolution. The field dependence was found to follow an exp(E) relation in the low-field regime, and an exp(1/E) relation in the high-field regime, consistent with the results of Hu et al. and McPherson et al. [20, 21]. This is not unique to HK+MG stacks; a similar transition is observed for SiO_2 data at high E-fields. However proper characterization across this range assumes fundamental importance for HK+MG where the typical operating and transistor characterization field span this transition.

The TDDB area scaling for Intel's 45nm HK+MG follows the conventional Weibull formulation. The β is in line with expectations for the thickness of the gate stack and the good agreement of the model out to product-like areas demonstrates an absence of 'defect' TDDB concerns on the *Final* optimized process flow.

The BTI results show that with sufficient optimization, aggregate NMOS+PMOS degradation levels equivalent to those achieved on SiO2 can be achieved on HK+MG operating at 30% higher E-fields. For the final process, PMOS BTI is matched at 50% higher E-field, and the PMOS degradation behavior on Intel's 45nm HK+MG process is found to be very similar to that observed on conventional SiON with equivalent acceleration and time dependence. The correlation of G_m and V_T shifts, the polarity of the V_T shift and charge pumping, and recovery data (not shown) all support that PMOS BTI is similarly driven by positive charge trapping near the Si/dielectric interface (D_{it}). P_b (Si-H dangling bonds at the interface) defects have been proposed for the PMOS IL degradation in NBTI stress [22].

On the other hand, the data show that NMOS BTI is largely driven by electron trapping within the HK bulk on the optimized process with additional contribution from interface traps on the *Initial* process. This explains the lack of NMOS G_m shift on the optimized process (the trap generation is further away from the interface) and the lower observed Ea on NMOS PBTI due to the direct tunneling of electrons from the substrate into the HK bulk [23, 24]. NMOS SILC degradation is also attributed to bulk traps, and a strong correlation is observed to trap density measured with charge pumping. Electron trapping in Hf-based oxides has been attributed to the presence of Oxygen vacancies [25].

The very large initial V_T shifts during BTI stresses observed on the initial HK process are due to high densities of pre-existing fast traps associated with D_{it} generation and/or hole trapping [4, 26]. These traps are very shallow, explaining the low observed temperature dependence, as shown in Figure 21(b).



(a) (b)

Figure 21: (a) BTI model with existing traps for "initial" process. (b) Fast trap component shows very weak temperature effect.

This effect is essentially eliminated with reduction in trap densities on the optimized HK process. This is further illustrated by pulsed IV sweeps on the *Initial* and *Final* processes that show large hysteresis on the former (shown in Figure 22). Fast traps in HK can lead to large instabilities resulting in underestimation of degradation with DC measurements.

(a) (b)

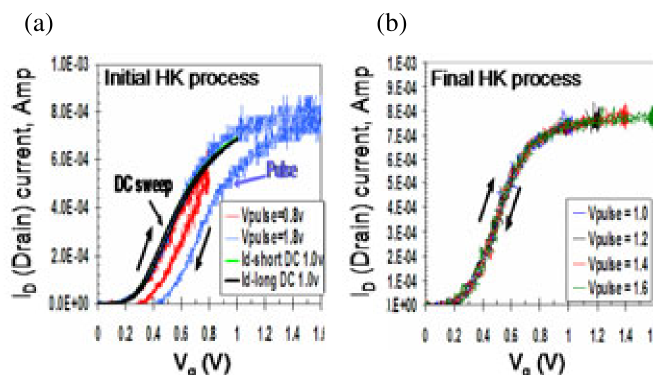


Figure 22: Pulse IV characterization of material with (a) poor reliability and (b) good reliability. Pulse t_r/t_f=100µsec, width=350µs used.

The rate of hot carrier injection for Intel's 45nm HK+MG transistor has been shown to be substantially lower than for conventional devices at the 65nm node. The data suggest that the effect continues to be dominated by that IL trapping with similar dependence on impact ionization induced substrate current. The reduced degradation is likely explained by the lower injection rate of the generated charge for the physically thicker dielectric. Figure 23 shows high temperature AC stressed RO data at several different stress voltages. The power-law time dependence slope increased with stress voltage implying that hot carrier degradation is contributing to BTI degradation during RO stress only at biases well in excess of real application conditions, and therefore hot carrier degradation is not a significant reliability consideration at any realistic use condition for this 45nm technology.

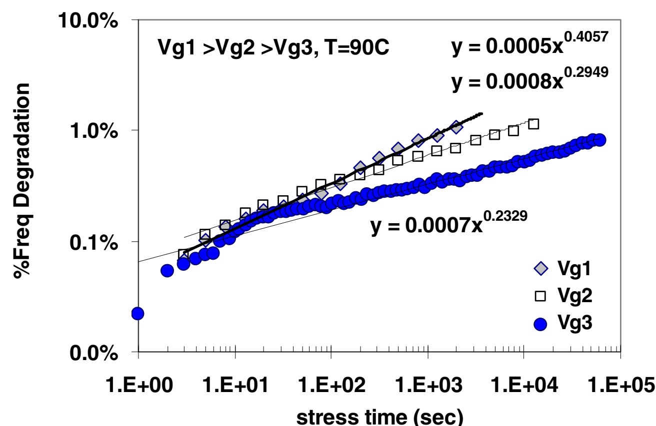


Figure 23: 45nm HK+MG Ring Oscillator (RO) stressed in AC at high temperature

CONCLUSIONS

This paper provides an overview of the reliability of Intel's 45nm HK+MG transistors demonstrating that these devices deliver reliability comparable to conventional SiO_2 devices at ~30% higher operating fields with negligible SILC degradation.

All of the major transistor reliability modes have been discussed with particular focus on those of greatest potential concern for HK+MG devices. The data for non-optimized material from early stages of technology development demonstrate that the reliability concerns for HK transistors raised in the literature are well founded. TDDB and BTI, the two modes which traditionally constrain transistor reliability, required dramatic improvement from the early experimental process revisions, for e.g., a>3X reduction in BTI V_T shifts. Similarly SILC and fast trapping are legitimate concerns but can be engineered out.

The primary HK reliability impact for TDDB, BTI, fast trapping, and SILC are all shown to relate to the potential for high trap densities in the HK stack. Controlling the trap densities within the HK and at the interfaces within the stack is critical to achieving the level of reliability demonstrated here.

The data also illustrate some challenges and potential pitfalls in characterizing the reliability of HK+MG transistors. In particular, accurate modeling of TDDB requires data collection over longer durations to properly calibrate the field dependence, and the presence of fast traps can result in underestimation of degradation using conventional DC measurements.

The overriding message is that although the revolutionary change represented by HK+MG poses daunting reliability challenges, these can all be addressed with appropriate transistor architecture and process optimizations, delivering the same reliability as conventional SiO_2 devices with compelling power/performance advantages.

ACKNOWLEDGMENTS

M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, J. Kavalieros, K. Kuhn, M. Kuhn, M. Metz, K. Mistry, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer.

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