BTI RELIABILITY OF 45 NM HIGH-K + METAL-GATE PROCESS TECHNOLOGY

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ABSTRACT

In this paper, Bias-temperature instability (BTI) characterization on 45nm high-K + metal-gate (HK+MG) transistors is presented and degradation mechanism is discussed. Transistors with an un-optimized HK film stack in the early development phase exhibited pre-existing traps and large amount of hysteresis that was consistent with literature. The optimized and final HK process demonstrated NMOS and PMOS BTI on HK+MG transistors that are better than that of SiON at matched E-fields and comparable at targeted 30% higher use fields. The final process also showed no hysteresis due to fast traps thereby allowing us to characterize its intrinsic degradation mechanism. On the optimized process, NMOS BTI is attributed primarily to electron trapping in the HK bulk and HK/SiON interfacial layer (IL) regions. PMOS BTI degradation, on the other hand, is mainly interface driven and is found to be very similar to that observed on conventional SiON transistors. [*Keywords:* BTI, High-K, Metal gate, Transistors, Reliability.]

INTRODUCTION

Transistor BTI degradation is a key reliability mechanism in HK+MG process technology. In addition to the PMOS NBTI, NMOS PBTI degradation has been observed [1]. Unacceptably high levels of BTI degradation in both NMOS and PMOS are observed on HK with pre-existing defects and of poor quality. Fast charge trapping/de-trapping has also been reported on HK materials which complicates characterization and calls the validity of conventional DC stress into question. BTI reliability degradation has been shown to be modulated by processing and integration changes such as thermal treatments, adding dopants, and nitridation [2-3]. Better charge trapping properties and improved reliability results on transistors fabricated with silicates dielectrics rather than oxide HK has been also reported [4]. In this paper, we identify intrinsic degradation mechanisms through extensive experimental observations and modeling support. Processing conditions were optimized to achieve BTI degradation on HK+MG that is comparable or better than with SiON dielectrics at 15% to 50% higher E-fields for both NMOS and PMOS respectively. The optimized HK film stack used in 45nm HK+MG process also showed negligible hysteresis and transient trapping associated with fast carriers.

EXPERIMENTAL RESULTS

The 45nm HK+MG transistors studied in this work have a Hafnium based gate dielectric and dual workfunction metal gate electrodes for NMOS and PMOS. The transistor formation involves HK first and MG last process as detailed in [5]. In this flow, HK is deposited using an ALD process and polysilicon is used for the gate patterning. After ILD0 deposition, a polish step exposes poly gates and the dummy poly is removed. Then, workfunction metal electrodes are deposited followed by a gate fill process. The SiO_2 EOT of the HK plus the Interface Layer (IL) that forms between the HK and the silicon is ~1.0nm. Fig. 1 describes the gate stack, with its SiO_2 like interface layer (IL) and the HK dielectric proper.

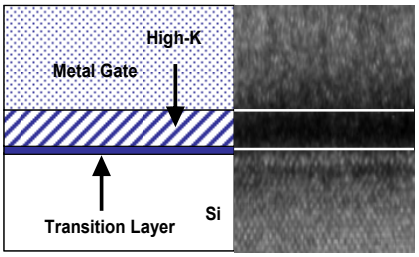
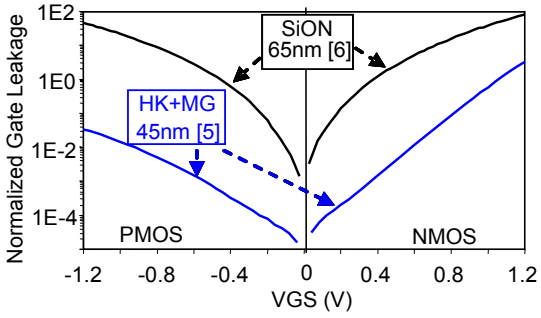


Figure 1. TEM of High-K and Metal gate (HK+MG) transistor stack.

Fig. 2(a) shows the typical gate leakage behavior of these 45nm HK+MG transistors measured in inversion, compared to the leakages of 65nm Poly/SiON transistors [6]. Substantial reduction (by 25-1000X) in gate leakage stems from the fact that physically thicker HK film is used while still maintaining a historical inversion Tox scaling trend of ~0.7X per technology generation. Fig. 2(b) shows the appropriate band diagrams for these HK+MG transistors. Lower inversion gate leakage current on the HK+MG PMOS is due to larger band offset than HK+MG NMOS (as indicated by the direction of arrows of the tunneling current).

(a)



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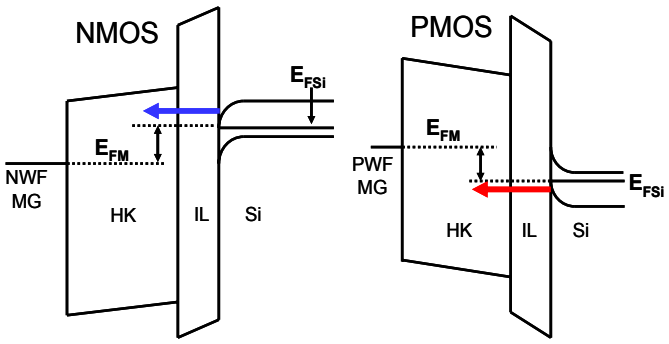

Figure 2. (a) 45nm HK+MG leakage comparison to that of 65nm Poly/SiON transistors. HK+MG process enables 25-1000X gate leakage reduction. (b) Band diagrams of HK+MG transistors.

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Unless stated otherwise, transistor BTI parameters were evaluated under conventional DC conditions with fixed measurement delay between stress and measurement (SMS). Care was taken such that the measurement phase did not result in additional trap creation. Any recovery due to charge detrapping is kept similar by using the same fixed delay in stress, measurement, and stress cycle. V_T was measured using 50mV on the drain. During stress, the gate was biased either with positive or negative polarity while all other terminals were grounded. All of the device results reported for 45nm HK+MG are from the devices that have drawn channel length of 40nm. The actual printed CD was well below 40nm.

The time evolution of 45nm HK+MG NMOS PBTI and PMOS NBTI is shown in Fig. 3. Both HK+MG NMOS and PMOS BTI degradation over time behavior was similar. NMOS showed slightly lower time slope of 0.17 as compared to PMOS NBTI. PMOS NBTI behavior is very similar to that observed in SiON with power-law time coefficient n of ~0.2 (from the typical NBTI equation of $\Delta V_T \sim t^n$). The time slope value is not too different than 1/6 (=0.17) reported for H_2 diffusion RD model [7] and other reports for HK-based PMOS devices [8]. PMOS with Poly/SiON reference data shown was stressed at different field than HK+MG PMOS and was used to simply illustrate the similarity of the time dependence behavior.

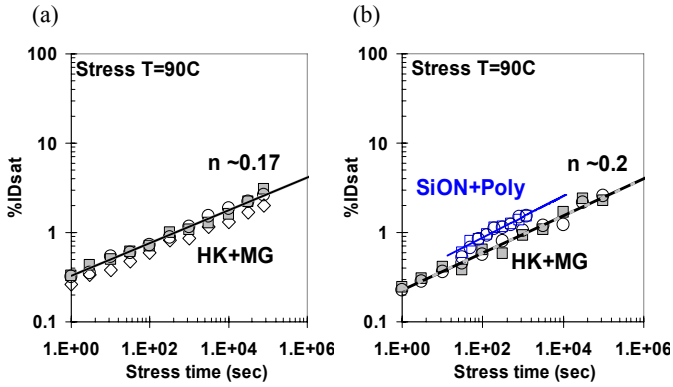


Figure 3. (a) NMOS PBTI time dependence. (b) PMOS NBTI time dependence of HK+MG transistors. Transistors are drawn at W/L=0.9um/0.04um for HK+MG process. Poly/SiON have W/L=1um/0.04um drawn dimensions.

From the temperature dependence of ΔV_T shift, a thermal activation energy (Ea) of 0.7eV was measured on HK+MG PMOS NBTI. Other reports have measured similar Ea of 0.8eV for SiO_2 [9]. Smaller Ea of 0.45eV was measured on NMOS. Ea was calculated from the TTF vs. 1/kT Arrhenius relationship using the temperature range of 60°C to 110°C as shown in Fig. 4. These values correspond to NMOS PBTI Ea'=0.08eV and PMOS NBTI Ea'=0.15eV when Ea' is re-calculated using the ΔV_T vs. 1/kT relationship, at fixed stress times. Lower Ea' (or Ea) on NMOS PBTI is expected from the direct tunneling of electrons from the substrate into the HK bulk and causing the V_T shift. This low Ea value is consistent with other reports on NMOS PBTI V_T shift due to electron trapping in the HK bulk [10-11]. Again, HK+MG PMOS NBTI has similar Ea values to SiO_2 of 0.68eV (data not shown), implying the similar mechanism, and therefore degradation is dominated at the IL.

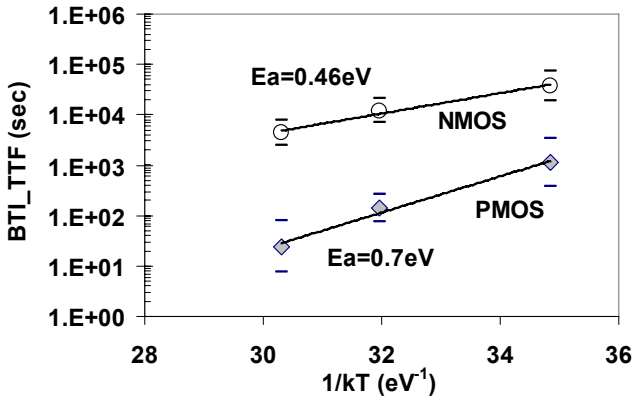


Figure 4. NMOS PBTI and PMOS NBTI activation energy (Ea).

Fig. 5 shows NMOS and PMOS BTI V_T shift vs. %Gm (transconductance) degradation comparing the un-optimized HK film stack in the early development stage ("initial") and the optimized ("final") process. Note that V_T shift is well-correlated to the %Gm degradation for both NMOS and PMOS for the "initial" HK process while it only correlates well to the PMOS on the "final" HK process. This implies that (i) high density of traps in the HK bulk as well as interface influenced the mobility on the "initial" process. (ii) For the optimized "final" HK process, the PMOS V_T shift is mainly interface driven. For the NMOS V_T shift in this case, the trap generation is further away from the interface not influencing the %Gm change, suggesting that the traps are HK bulk traps. Based on the polarities of the observed V_T shifts, electron trapping in the HK is responsible for the NMOS V_T shifts, while the PMOS V_T shifts are attributed to the positive charge traps generated near the IL (also validated from the charge-pumping results). Oxygen vacancy was shown to be responsible for the defects in the Hf-based oxides that lead to the high electron trapping rate [12]. P_b (Si-H dangling bonds at the interface) defects were responsible for the PMOS IL degradation upon NBTI stress [13].

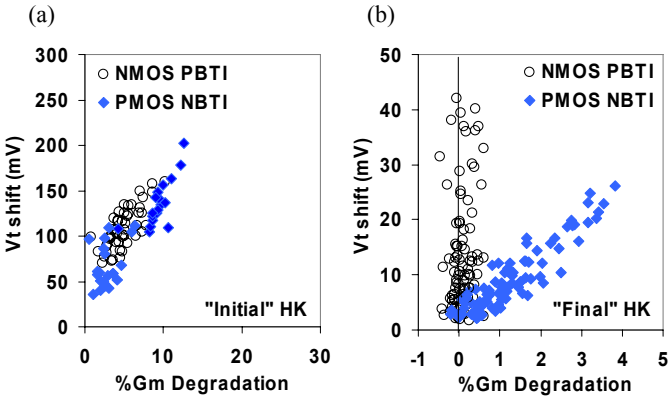


Figure 5. NMOS and PMOS BTI V_T shift vs. %Gm degradation on an (a) "Initial" process vs. (b) "Final" 45nm HK+MG process.

Fig. 6 shows NMOS PBTI V_T shift over time for the "initial" and "final" HK+MG processes. The initial HK process has a very large V_T shift even after 1sec of stress and its time dependence is very flat (with time slope ~0.07). This implies that the dielectric is of very poor quality. Increasing the stress voltage (from VG1 to VG2,

VG2>VG1, VG2 being much greater) did not change the degradation behavior. Both showed similar flat time dependence. This further confirms that the BTI degradation of this HK dielectric is dominated by very efficient electron filling of high density pre-existing defects/traps. On the other hand, the optimized HK process showed intrinsic BTI behavior similar to that in Fig 3(a) and the observed degradation magnitude depended on the stress voltage, i.e., higher V_T degradation was observed with higher gate stress bias. The time dependence is similar for both of the stress conditions on optimized HK process. The reliability differences observed in BTI is also manifested in the gate leakage measurements. Gate leakage is very flat on the "final" HK+MG process, while the "initial" HK+MG process showed early movement and even large increase of leakage current at higher stress biases.

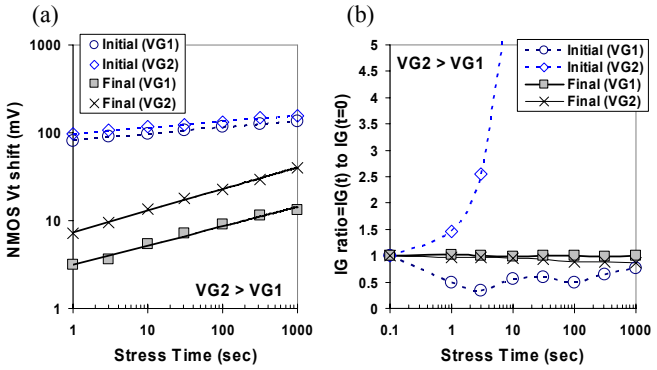


Figure 6. (a) NMOS PBTI V_T shift and (b) IG characteristics for "initial" and "final" HK+MG process.

Fig. 7 shows results on HK+MG PMOS NBTI supporting similar conclusions to the HK+MG NMOS BTI discussion above and shown in Fig. 6; except that on PMOS, there's literally no IG movement. This is again supported by the fact that the traps are mostly interfacial (D_{it}) and do not distort the field in the dielectric stack at these stress conditions. Again, very high V_T shift after only 1sec stress suggests fast trapping mechanism for the initial HK process. These fast trapping was associated with D_{it} generation and/or hole trapping on the PMOSFET [8, 14]. Initial HK process with higher voltage stress (VG2) showed some sign of IG movement and V_T shift was larger.

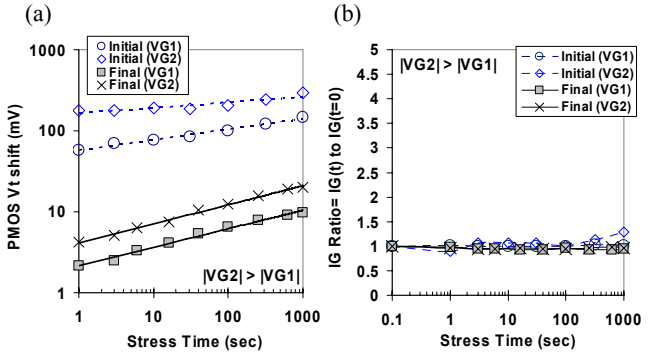


Figure 7. (a) PMOS NBTI V_T shift and (b) IG characteristics for "initial" and "final" HK+MG process.

Based on the above discussions, in summary, the degradation associated with NMOS PBTI is dominated by the bulk HK (the HK/IL interface may also play a role) whereas PMOS NBTI behavior is very similar to SiON, suggesting defect generation close to the interfacial (IL) regions. Further supporting these conclusion are the results of "initial" HK PMOS stressed in accumulation which showed electron trapping behavior similar to HK+MG NMOS PBTI results. Fig. 8 shows PMOS stressed with highly accelerated positive polarity, i.e., PMOS PBTI stress. The results showing an absolute reduction in PMOS V_T is consistent with electron trapping in the bulk HK for the "initial" HK process. For the "final" HK process, negligible V_T shift was observed even though the stress +Vg was 40% higher and stress times were longer. This further suggested that the HK dielectric was very robust and reliable on the PMOS after all the integrated flows.

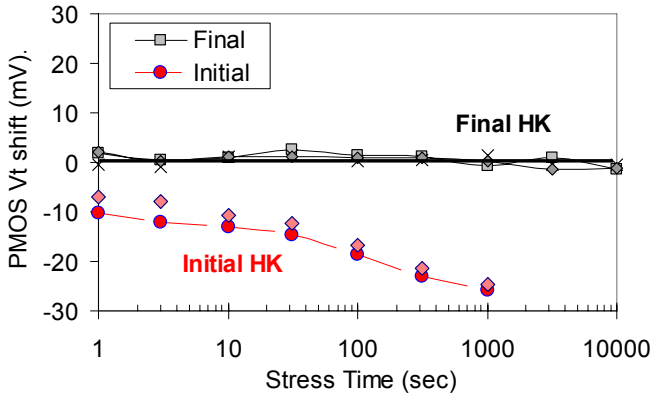


Figure 8. PMOS PBTI V_T shift for "initial" and "final" HK+MG process. The +Vg used for "final" HK is 40% higher than "initial" HK process. PBTI stress was done at T=125C.

PMOS NBTI in SiO_2 exhibits a recovery behavior upon removal of stress. This recovery behavior has been explained within the frame work of RD model by others where dissociated hydrogen from NBTI stress is back-diffused to the interface [15]. More recently, others have suggested a hole detrapping mechanisms for the NBTI recovery [8, 14]. We've examined the recovery behavior of the HK+MG PMOS and compared to the PMOS NBTI of SiON. The recovery behavior was very similar (not shown). Similarities in both degradation and recovery mechanism in HK+MG PMOS to SiON PMOS behavior validates that the NBTI mechanism is related to IL degradation. Recovery on NMOS was also examined and showed smaller recovery rate than the PMOS. More study is needed to understand the NMOS recovery mechanism and differences to the PMOS recovery behavior.

Table I summarizes key intrinsic characteristics of NMOS vs. PMOS BTI mechanisms as discussed.

TABLE 1. COMPARISON OF NMOS AND PMOS BTI RESULTS

NMOS PBTI	PMOS NBTI
(i) PBTI Vt-shift not correlated to %Gm	(i) NBTI Vt-shift vs. %Gm degradation
(ii) Vtn increase suggests electon(-) trap	(ii) Vtp increase suggest (+)chg trap
(iii) Strong signal on HK quality/change	(iii) Similar time slope, Ea vs. SiON
	(v) Recovery similar to SiON (not shown)

Fast traps in HK can lead to large instabilities and DC measurements can underestimate the actual degradation in these cases. Fig. 9 shows pulsed IV characteristics for the (a) "initial" HK and (b) "final" HK process. "Initial" HK that showed high BTI degradation in DC stress also exhibited very large hysteresis in pulsed measurements. For the "final" HK process, hysteresis was negligible and unchanged with pulsed bias demonstrating that fast traps have been virtually eliminated with process improvements. Therefore, conventional DC techniques may be used to characterize BTI.

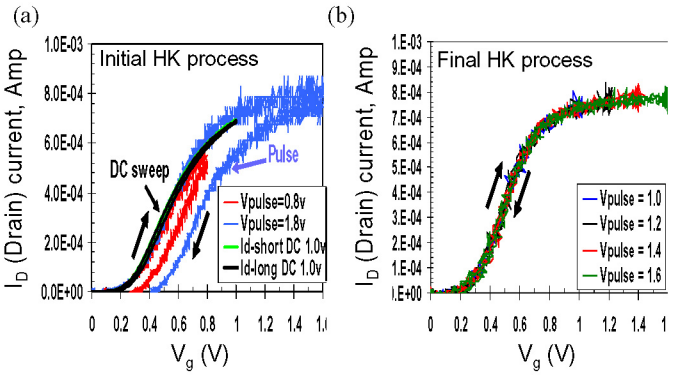


Figure 9. Pulse IV characterization of material with (a) poor reliability and (b) good reliability. Pulse t_r/t_f=100µsec, width=350µs used.

Fig. 10 shows the BTI characteristic on material with some hysteresis. The change in time dependence with stress can be explained by the presence of fast traps. For simplistic modeling, ΔV_T shift can be expressed as $\Delta V_T = A + B \bullet t^n$, where A=fast trap component, B=true BTI component. Fig. 10b shows that fast traps are not very sensitive to temperature, consistent with [16], and true BTI degradation can be estimated with longer stress on material with non-negligible hysteresis. The fast trap component A is negligible on the final optimized process. In [8], the fast trapping component is described by using logarithmic time dependence. Our fast trapping component can also be fit well with logarithmic time dependence. This fast trapping component is either significantly suppressed or eliminated on a high-quality dielectric [17-18]. Intrinsic degradation (or permanent component of the degradation) can be probed at longer stress times, which is critical for the accurate lifetime assessment [19].

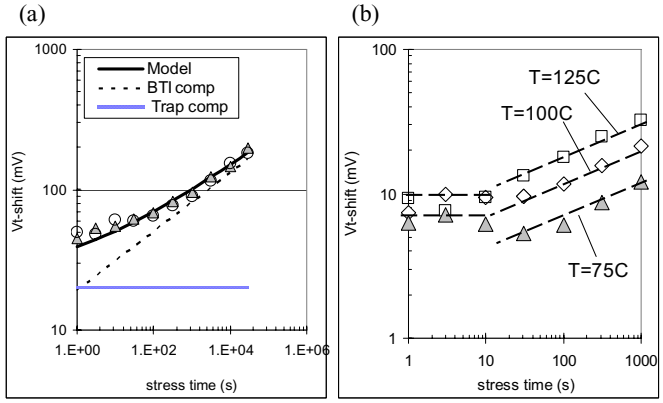


Figure 10. (a) BTI model with existing traps for "initial" process. (b) Fast trap component shows very weak temperature effect.

Fig. 11-12 shows HK+MG BTI better than in SiON can be achieved with the "final" HK process. PMOS NBTI is matched at 50% higher E-field (Fig. 11) while NMOS PBTI is matched at 15% higher E-field (Fig. 12). The net NMOS + PMOS BTI shift is matched at 30% higher E-field compared to SiON. E-field is calculated using Vg over inversion Tox for both 65nm and 45nm transistors. For comparison purposes, NMOS PBTI on SiON is stressed at much higher than the normal operating fields. The dramatic improvement in BTI results from a high quality HK film stack coupled with significant reduction in charge fluence during stress (Fig. 2).

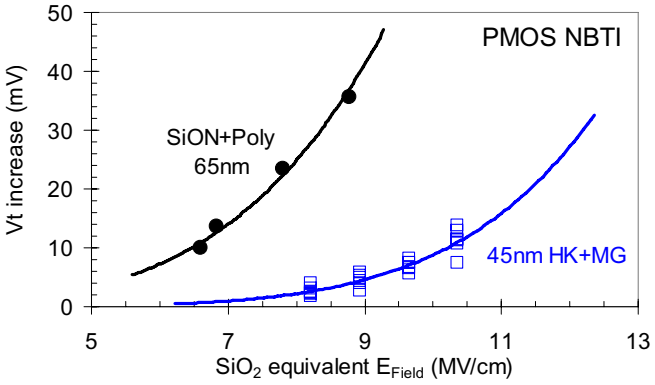


Figure 11. PMOS NBTI V_T shift vs. Electric field.

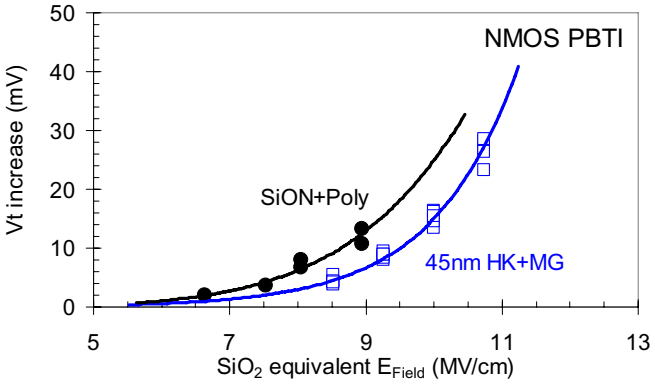
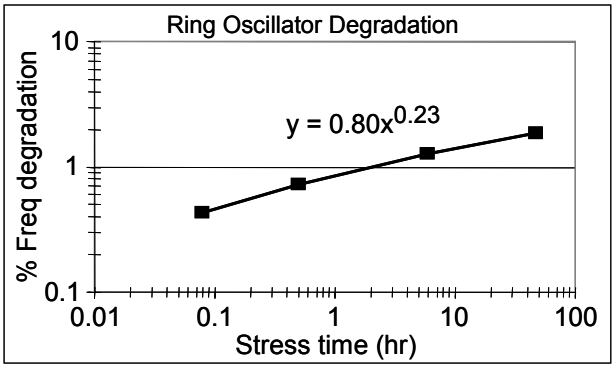


Figure 12. NMOS PBTI V_T shift vs. Electric field.

Fig. 13a shows 45nm HK+MG Ring Oscillator (RO) stress data with time slope of ~0.2 similar to the device level BTI. Fig. 13b shows the RO stress data vs BTI model based on device level data showing very good agreement.

(a)



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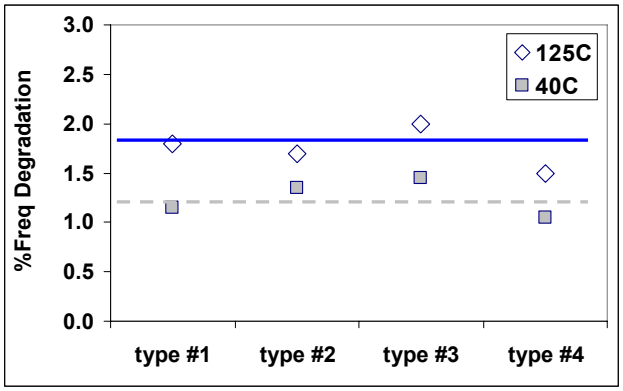

Figure 13. (a) Ring Oscillator degradation. (b) RO stress data against BTI model based on discrete transistors.

Hf-based HK dielectric has low conduction band offset in contact with silicon substrate. This reduced barrier has potential risk against the hot carrier injection [20]. Fig. 14 shows NMOS hot electron reliability comparison between the 45nm HK+MG and 65nm Poly/SiON transistors [6]. 45nm HK+MG transistors showed huge improvement in lifetime (>7X at same Isub) over 65nm transistors. TTF to impact ionization slope is very similar between the two technologies suggesting that interfacial layer (IL) is playing an important role.

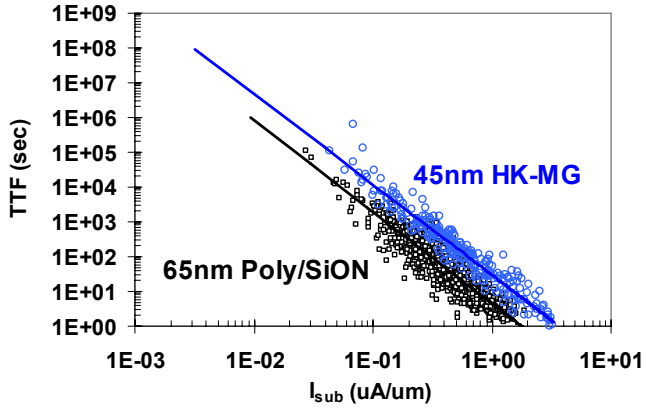

Figure 14. NMOS hot electron performance of 45nm HK+MG and 65nm Poly/SiON transistors.

Fig. 15 shows high temperature AC stressed Ring Oscillator data performed at several different stress voltages. The power-law time dependence slope is higher with higher Vcc indicating hot carrier mechanism is coming into play in addition to the BTI degradation during RO stress. NMOS hot-electron degradation typically shows a time slope of >0.3-0.4. With reduced stress bias (Vg3 still being much greater than the operation and burn-in voltage), only BTI degradation is apparent with a time slope of ~0.2. This suggests that hot carrier degradation is not likely the reliability limiter for the typical inverter type logic circuits based on 45nm HK+MG process.

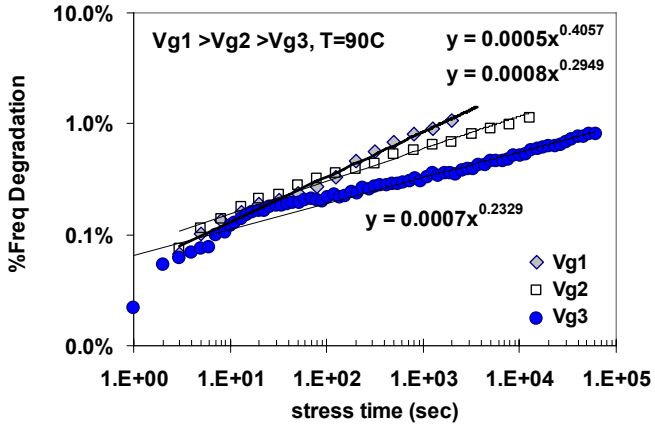

Figure 15. 45nm HK+MG Ring Oscillator stressed in AC at high temperature.

CONCLUSION

Dramatic improvement in the BTI characteristics of 45nm HK+MG transistors has been demonstrated with net BTI comparable to that observed on SiON at a targeted 30% higher operating field. BTI mechanisms for NMOS and PMOS devices on 45nm HK+MG were extensively studied with DC and pulsed current techniques. Bulk trapping in the HK is found to be the dominant mechanism responsible for NMOS PBTI, whereas PMOS NBTI degradation is interface driven. Both HK bulk and well as IL improvements are therefore needed to address reliability of HK+MG CMOS transistors.

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