Ultrathin Gate Oxide Reliability: Physical Models, Statistics, and Characterization

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***Abstract*—The present understanding of wear-out and breakdown in ultrathin ($t_{ox} < 5.0$ nm) SiO_2 gate dielectric films and issues relating to reliability projection are reviewed in this article. Recent evidence supporting a voltage-driven model for defect generation and breakdown, where energetic tunneling electrons induce defect generation and breakdown will be discussed. The concept of a critical number of defects required to cause breakdown and percolation theory will be used to describe the observed statistical failure distributions for ultrathin gate dielectric breakdown. Recent observations of a voltage dependent voltage acceleration parameter and non-Arrhenius temperature dependence will be presented. The current understanding of soft breakdown will be discussed and proposed techniques for detecting breakdown presented. Finally, the implications of soft breakdown on circuit functionality and the applicability of applying current reliability characterization and analysis techniques to project the reliability of future alternative gate dielectrics will be discussed.**

***Index Terms*—CMOS, defect generation, reliability, silicon dioxide, time-dependent dielectric breakdown.**

I. Introduction

AGGRESSIVE scaling in microelectronics to achieve higher performance and circuit density necessitates the thinning of the SiO_2 gate dielectric. This thinning is necessary to maintain the MOSFET gate capacitance such that there is adequate drive current for proper circuit operation. Two of the most critical factors that may limit the future scaling of the thickness of SiO_2 is the gate leakage current (which contributes to unacceptable standby power consumption) and the intrinsic reliability of the film.

The maximum acceptable gate leakage has been suggested to be between 1 A/cm^2 and 10 A/cm^2 [1], [2]. This corresponds to an oxide thickness between 1.2 nm and 1.5 nm [2]. However, another concern is that intrinsic reliability (oxide wear-out and eventual breakdown) may limit the further scaling of oxide thickness. In fact, a recent projection of oxide lifetime based on data available at the time of the report indicated that oxides thinner than 2.2 nm may not have the required reliability [3].

It has always been crucial to use the correct physical model, breakdown statistics, and acceleration parameters (for voltage and temperature) to accurately project oxide life from accelerated stress tests. For projecting the life of current generation ultrathin gate oxides where the reliability margin appears to be shrinking, it is even more important to use the proper models and parameters. Accelerated stress tests used to obtain the necessary parameters for projection must be robust, valid, and performed on statistically significant sample sizes.

This article reviews the current understanding of defect generation, wear-out, and, breakdown of ultrathin ($t_{ox} < 5$ nm) SiO_2 films. Section II discusses the proposed physical models of breakdown and recent analysis of breakdown data that suggests a change of an electric field-driven wear-out process to a voltage-driven process as oxide thickness is decreased. The statistics and the use of percolation theory to describe the changes in breakdown statistics and defect generation for thinner oxide films will be discussed in Section III.

Reliability characterization of ultrathin oxides has become extremely challenging due to the difficulty of detecting and interpreting soft breakdown. Issues relating to characterizing soft breakdown and its impact on reliability projection will be discussed in Section IV. Finally, Section V will present conclusions and implications for future alternative gate dielectric systems.

II. Physical Models for Defect Generation and Oxide Wear-Out

A. Early Models and Breakdown in Thin Oxides

Time-dependent dielectric breakdown (TDDB) or "wear-out" of thin silicon dioxide films was observed over three decades ago [4]–[7]. Although the exact physical mechanism responsible for wear-out and eventual breakdown is still an open question, it is generally assumed that a driving force such as the applied voltage or the resulting tunneling electrons create defects in the volume of the oxide film. The defects accumulate with time and eventually reach a critical density triggering a sudden loss of dielectric properties. A surge of current produces a large localized rise in temperature leading to permanent structural damage in the silicon-oxide film.

Several physical mechanisms have been identified as the most probable in causing defect generation in thin SiO_2 films. First, an empirical model for breakdown was developed by observing the electric field dependence of TDDB data [8]–[10]. When the logarithm of the time-to-failure was plotted against applied electric field a straight line was observed, i.e., $t_{BD} \sim \exp(-\gamma E)$, where E is the electric field and γ is the electric field acceleration factor. Acceleration parameters for the electric field and temperature could be extracted from the model to allow extrapolation of oxide lifetime from accelerated stress conditions. Later, a physical model known as the Thermochemical model was hypothesized based on an electric field driven defect generation

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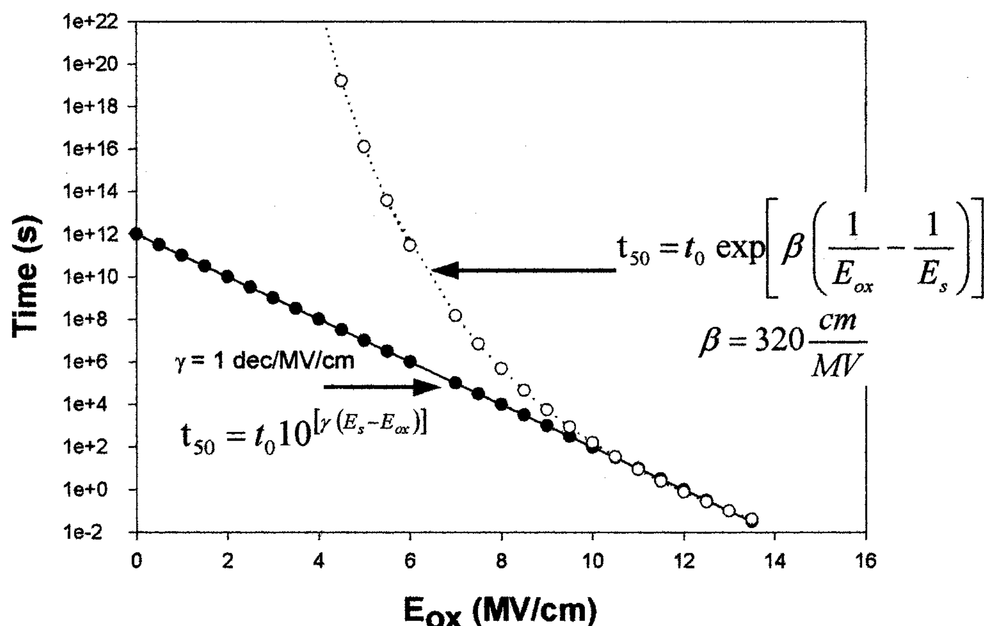

Fig. 1. Lifetime extrapolations based on the linear E and the reciprocal $1/E$ models illustrating the very large discrepancies at the lower electric fields. Both models are indistinguishable for electric fields above 9 MV/cm for the field acceleration values (γ for the E model and β for the $1/E$ model) indicated in the figure.

process that yielded the same observed dependence of oxide lifetime on electric field [11]. This model known as the E model indicated that the applied electric field interacts with the weak Si–Si bonds associated with oxygen vacancies in the amorphous SiO_2 film. The applied electric field eventually breaks the weak bond and creates a permanent defect or trap [12]–[14]. This defect is referred to as the E' center, which is a structure in the SiO_2 having an unpaired electron localized on a silicon atom which is bonded to three oxygen atoms [15]. Tunneling electrons are not necessary (to the first order) in the thermochemical model to create defects.

A second mechanism (known as the $1/E$ model) was proposed based on anode hole injection [16]–[18]. In this case, tunneling electrons (based on Fowler–Nordheim conduction) transferred energy to holes in the anode, where they are injected into the oxide film. An earlier version of the model was based on a feedback mechanism where injected holes became trapped and modified the oxide potential barrier to enhance additional electron injection. Eventually, the positive feedback process caused a current runaway leading to breakdown. In this case the time-to-failure was proportional to the inverse of applied electric field [i.e., $t_{BD} \sim \exp(\beta/E)$]. Where β is the electric field acceleration factor. The reciprocal field dependence is a consequence of the Fowler–Nordheim tunneling current, which is the driving force for the defect generation. At higher voltages (~9 V), holes can be generated in the oxide by impact ionization processes and subsequently trapped, leading to breakdown [19].

The two models (E and $1/E$) can lead to very different extrapolations-based accelerated stress data as depicted in Fig. 1. Note that the reciprocal field model is extremely optimistic compared to the thermochemical model at lower electric fields (close to circuit operation conditions) for the assumed values of β and γ. Both models have been the subject of debate over the past three decades since there is large discrepancy in the lifetime projection for electric fields close to use conditions. One of the difficulties in validating the models is that both models give a reasonably good fit to data for high electric fields as shown in Fig. 1. Researchers attempted to validate the models by conducting tests over long periods of time [20]–[22] and accelerated temperatures [23], [24] to facilitate the collection of breakdown data at lower electric fields. The data reported in [20], [22]–[24] indicated that the logarithm of the time-to-failure was linear with electric fields closer to operating conditions. It was pointed out, however, that the values of the electric field acceleration parameters reported in the studies were greater than what the thermochemical model predicted [25]. Fig. 2 is data from [24] and shows a deviation of the log (t_{BD}) from the $1/E$ dependence at electric fields below 7 MV/cm.

Both the E and the $1/E$ models assumed a temperature dependence of the form $t_{BD} \sim A\exp(E_a/kT)$, where E_a is referred to as the thermal activation energy, k is Boltzmann's constant, T is the absolute temperature, and A is a constant. E_a is due to different physical processes depending on the model assumed. In the E model E_a is related to the enthalpy of activation for oxide breakdown or it is related to the temperature dependence of the hole-generation coefficient and the slope of the Fowler–Nordheim tunneling characteristic in the $1/E$ model [26]. Experimental data for thicker oxides ($t_{ox} > 5.0$ nm) have shown that the temperature dependence for the same stress electric field follows an Arrhenius behavior. Both the E and $1/E$ predict that E_a changes as a function of electric field, which has been shown experimentally. Section III-B will discuss recent experimental results for temperature acceleration in the breakdown of ultrathin oxides.

It will be discussed later that simply observing an empirical dependence of breakdown time on electric field is not conclusive evidence for a particular physical model. In fact, an anode hole injection process does not necessarily require

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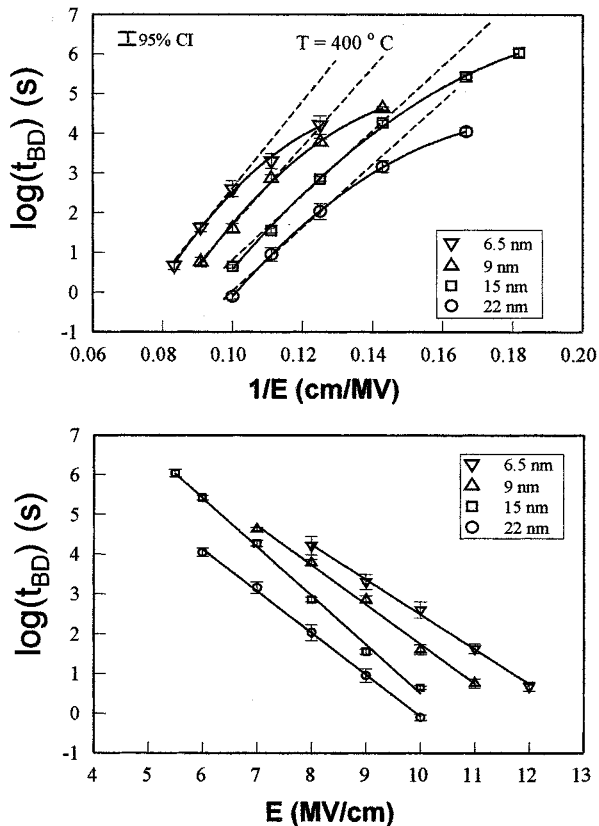

Fig. 2. Plots showing log (t_{BD}) as a function of electric field and reciprocal electric field from [24]. Low electric field TDDB data was obtained by conducting measurements at very high temperatures. The data deviate from the $1/E$ dependence at electric fields below 7 MV/cm.

a $1/E$ dependence, especially when considering the defect generation process in the direct tunneling regime for ultrathin gate dielectrics.

B. Voltage Driven Models for Breakdown in Ultrathin Films

The validity of an electric field driven model becomes questionable after the observation of results from substrate hot electron injection experiments (SHEI) [27]–[30] and the thickness and polarity dependence of ultrathin gate oxide breakdown [31], [32]. As discussed earlier, a thermochemical wear-out process should only be related to the magnitude of the electric field and the length of time it is applied to the gate, not to the amount of charge injected. The experimental setup is shown in the left frame of Fig. 3, where a separate n^+p junction is forward biased by increasing V_{inj} to inject carriers into the channel of an n-channel MOSFET biased into inversion. This structure allows independent control of the gate voltage (and gate electric field) and the density and energy of carriers (determined in part by the substrate bias, V_b) injected into the gate. Therefore, the gate voltage can be held constant and the number and energy of injected carriers can be varied to determine if there is any effect on device lifetime. The results from the study reported in [30] for oxides with a thickness range between 2.0 nm and 3.0 nm are also shown in the right frame of Fig. 3. Note that a significant reduction in oxide life from constant voltage stress conditions (shown by solid symbols) is observed if electrons are also injected by increasing V_{inj} for the same gate voltage stress (data shown as open symbols). An important result of the study indicated that t_{BD} is proportional to the inverse of the injected current density (modeled by the solid and dashed lines).

Other experiments were conducted where the electric field can be modulated by changing the polysilicon gate doping while maintaining a fixed gate voltage [32]–[34]. The study presented in [32] used oxides having various polysilicon gate doping levels such that the gate electric field was varied by 2.5 MV/cm for a fixed gate voltage. Fig. 4 shows the t_{BD} of 2.6 nm capacitors stressed with a gate voltage of 3.6 V for a variety of gate electrode doping levels. The results show that the lifetime is nearly independent of polysilicon doping. An electric field driven model would predict a change of 20 000× over the same doping range as indicated in the figure.

Another important observation was that thinner oxides exhibited much lower lifetimes at the same electric field. This trend was compiled by McPherson [13] and is shown in Fig. 5 for a constant electric field of 8 MV/cm. The oxide lifetime dramatically decreases for a thickness below 4 nm. It was noted in [13] that the lifetime decrease scales with the increase in direct tunneling current as a function of oxide thickness. Increased tunneling current may enhance the injection of holes which are subsequently captured by a Si–O bond. Such a capture could enhance the bond breakage rate by a field driven mechanism. In this case, a link to the involvement of tunneling current in the breakdown process is necessary.

C. Energy and Electron-Induced Defect Generation

Anode Hole Injection (AHI): In the previous section, it was established that there is strong evidence that tunneling electrons must be the driving force for wear-out and breakdown in ultrathin SiO_2. In the direct tunneling regime, the energy of the tunneling electrons is proportional to the applied gate voltage [35]. When considering a physical process for defect creation in thin oxides it is important to consider the energy required for such a process to occur. At energies below those required for anode impact ionization (~9 ev), anode hole injection (AHI) was believed to take place via surface plasmon processes [36], [37]. This process requires electrons with energies greater than 7 eV for hot-hole injection and subsequent trapping [36], [38]. The high carrier energy would appear to preclude AHI from taking place at lower voltages, especially at circuit operating voltages. An additional physical process involving minority ionization [39], [40] of holes in p-type anode material or lightly doped inverted n-type material was proposed that would allow hole injection at low voltages. This modification to the model and the experimental evidence that a critical hole fluence (Q_p) was required for oxide breakdown [17] substantiated the AHI model. Q_p was inferred from substrate current measurements on n-channel MOSFETs biased in inversion. The value of Q_p was determined to be approximately 0.1 C/cm^2 and was independent of stress conditions. Schuegraf [41] later showed that the value of Q_p decreased for decreasing oxide thickness. It was also shown that Q_p exhibited a temperature dependence [42] and was not constant under low electron injection conditions for substrate hot hole injection experiments [43].

The AHI model was questioned when the origin of substrate current could be linked to physical mechanisms other than tun-

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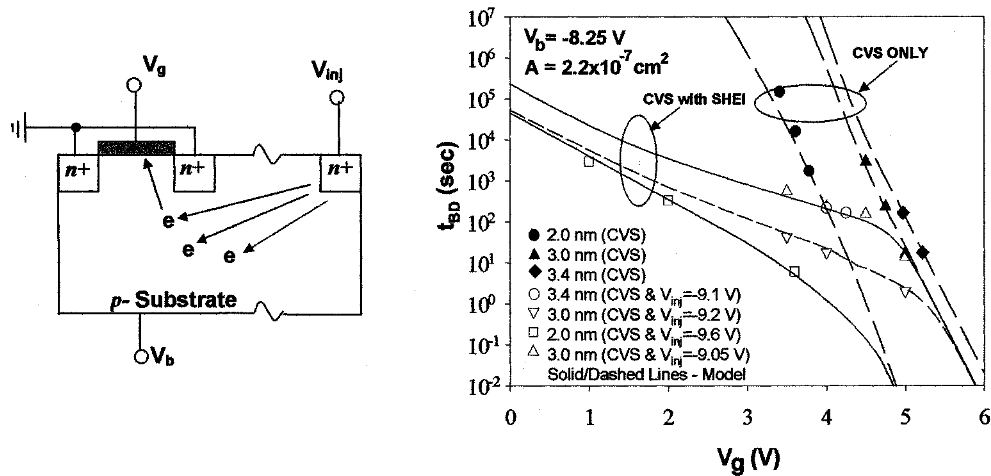

Fig. 3. Time-to-breakdown (t_{BD}) versus (right figure) gate voltage for combined constant voltage stress and substrate hot-electron injection from [30]. A schematic of the experimental set up is illustrated in the left figure. The solid symbols are data for constant voltage stress only. The open symbols are data when substrate electrons are injected simultaneously with constant voltage stress. The solid and dashed lines are the result of a model that accounts for injected currents due to the constant voltage stress and the SHEI. Note that t_{BD} is significantly degraded indicating that injected electrons play an important role in the degradation of thin-gate oxides.

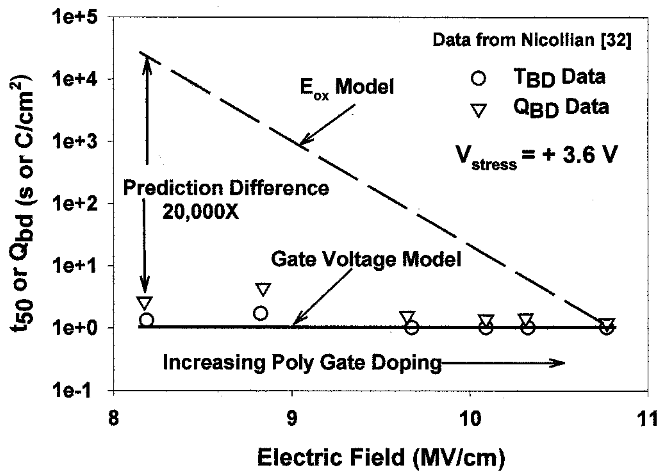

Fig. 4. Data and model reported by Nicollian [32] illustrating a voltage driven model for time-dependent dielectric breakdown. The electric field was change by altering the polysilicon doping in the gate electrode while maintaining the same stress gate voltage. The time-to-breakdown does not change as the electric field is modified precluding an electric field acceleration model for breakdown.

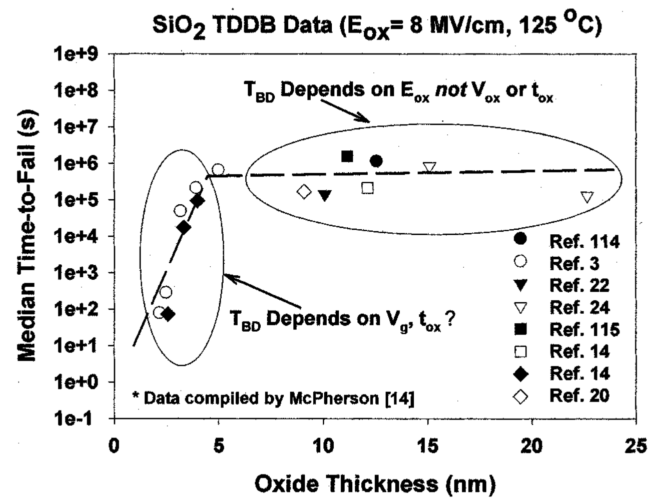

Fig. 5. Plot and data compiled by McPherson [13] illustrating the trend of decreasing reliability for ultrathin oxides at the same electric field. The trend suggests a voltage-driven breakdown model. Data is derived from [3], [13], [20], [22], [24], [114], [115].

neling holes. These mechanisms include generation-recombination processes in the substrate [38] and photo-excitation processes due to photons generated by energetic electrons in the gate region [44]. Another question concerning the AHI model was the value of 0.1 C/cm^2 obtained for the critical hole fluence. For low voltages the hole current is many orders of magnitude lower than the electron current. The oxide defect generation rate for energetic electrons and holes were directly measured by DiMaria [45]. The defect generation rate was determined by monitoring the stress-induced change of electrically active defects such as interface trap density (D_{it}) or stress-induced leakage current (SILC). It was reported that the rate at which these defects were generated is correlated to the rate of oxide wear-out since the number of defects at breakdown (N_{BD}) remained constant independent of stress conditions [3], [46]. The number of defects generated per injected hole was shown to be similar to the number generated per injected electron provided the energy of the injected carriers are similar [45]. It therefore appears that the hole fluence is too low to cause appreciable defect generation at low voltages. Recent studies using substrate hot hole injection (SHHI) in a manner similar to SHEI shown in Fig. 3, indicate that Q_p must be six to eight orders of magnitude greater than 0.1 C/cm^2 to cause dielectric breakdown [47]–[49]. It was also shown that the N_{BD} for hole injection was over one order of magnitude greater than electron injection indicating that holes are very efficient in producing measurable electrically active defects but inefficient in producing defects that lead to oxide wear-out [49].

However, recent experimental evidence and modeling have demonstrated that AHI can indeed be operative in ultrathin oxides at low gate voltages. Nicollian [32] showed that bulk defect generation is increased significantly and Q_{BD} decreased for devices with lightly doped n$^+$ polysilicon gate electrodes. The devices were biased to invert the polysilicon anode re-

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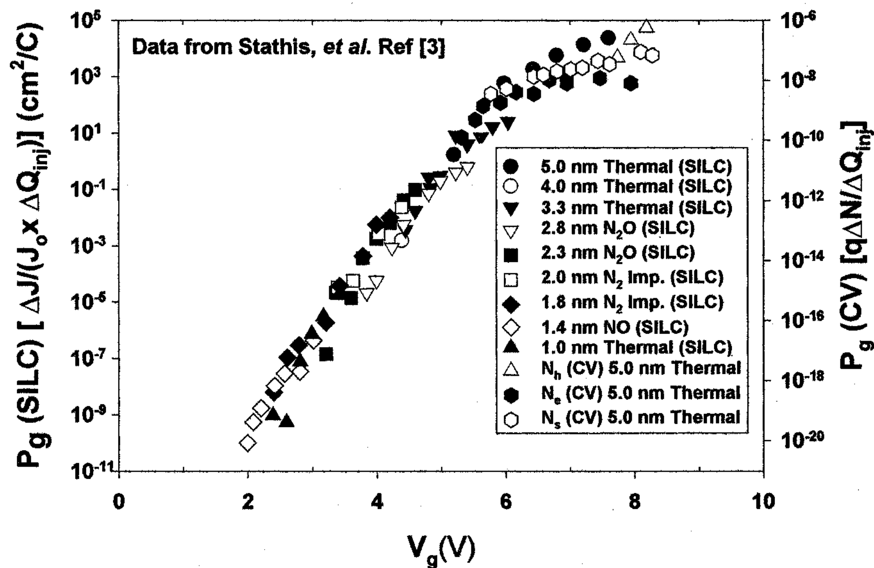

Fig. 6. Data reported from [3] showing the universality of the defect generation rate (P_g) as a function of gate voltage for ultrathin dielectrics of varying thickness and from different technologies. The data is derived from SILC measurements and capacitance–voltage characteristics. The voltage dependence (electron energy) correlates to experiments measuring the desorption rate of atomic hydrogen from a silicon surface as explained in the text.

sulting in mechanisms that favor the injection of free holes at the poly-SiO_2 interface. The holes could be injected through or over the oxide energy barrier. An important result from a detailed AHI model developed by Alam [50] predicted the voltage dependence of the voltage acceleration factor [the slope of the $\ln(t_{BD})$ versus V_g characteristic] observed by others [21], [40], [51] for ultrathin SiO_2 films and will be discussed in more detail in Section III-B.

Anode Hydrogen Release (AHR): There is evidence for a defect generation mechanism involving the release of atomic hydrogen from the anode by energetic tunneling electrons [52]. It has been known for some time that hydrogen can induce a number of defects in silicon dioxide films by intentionally exposing MOS devices to hydrogen [53]–[55]. A trap creation process attributed to the release of atomic from the Si/SiO_2 interface has been shown to have a threshold voltage of approximately 5 V [52]. The process has been shown to continue at voltages as low as 1.2 V, which includes the regime of circuit operating voltages [46], [56].

The model known as the defect generation model relates the charge-to-breakdown (Q_{BD}) to the number of defects at breakdown (N_{BD}) divided by the defect generation rate (P_g) or $Q_{BD} = qN_{BD}/P_g$. The time-to-breakdown or t_{BD} is simply equal to the tunneling current (J_g) divided by Q_{BD} or $t_{BD} = J_gP_g/qN_{BD}$. N_{BD} is independent of stress conditions but exhibits a thickness dependence which will be discussed in Section III. P_g is a strong function of the applied gate voltage or electron energy. Fig. 6 shows a plot of P_g as a function of applied gate voltage for a range of gate oxide thickness [3]. The deviation of the data from the exponential trend above 6 V illustrates the change from ballistic to quasi steady state transport of the tunneling carriers [52]. It is also interesting to note that an experiment measuring the desorption rate of atomic hydrogen from a silicon surface as a function of incident electron energy provided a dependence very similar to the P_g voltage dependence shown in Fig. 6 [57].

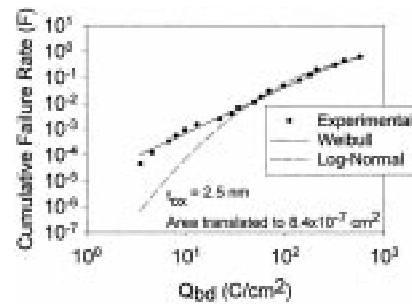

Fig. 7. Weibull and log-normal distributions fitted to breakdown data from 2.5-nm gate oxides [61]. The Weibull exhibits a much better fit, especially at the lower failure percentiles where reliability extrapolations are typically performed.

The primary argument against the hydrogen release process for oxide breakdown is the observation that Q_{BD} (or t_{BD}) does not appear to improve if an isotope of hydrogen (like deuterium) is used to passivate the Si/SiO_2 interface [58]. It has been reported that deuterated oxide films have suppressed hydrogen desorption from the interface with silicon and consequently improved immunity to interfacial trap generation due to channel hot-carrier injection [59]. Suppression of SILC has also been reported [60].

It should be mentioned that defect generation model ($Q_{BD} = qN_{BD}/P_g$) does not necessarily imply an AHR mechanism. The physical mechanism incorporated in the P_g term could also be other processes such as AHI which has been shown to have a similar gate voltage dependence at lower voltage [50]. The observed thickness dependence of N_{BD} in ultrathin oxides has provided a key insight into the statistical behavior of defect generation and breakdown.

There is still considerable controversy concerning the physical model of breakdown in SiO_2. It is still not known definitively whether released species like hydrogen or injected holes cause the defect that eventually leads to breakdown. However,

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it is believed that the microscopic structure of the wear-out defect could be related to the E' center that was discussed in Section II-A. The E' structure has been shown to exhibit electron and hole trapping characteristics as well as complexes associated with hydrogen [15].

The next section will describe the observed thickness dependence of N_{BD} in more detail and how it relates to the concept of percolation theory to predict the shape of cumulative failure distributions as a function of oxide thickness.

III. Statistics and Projection of Breakdown in Ultrathin Films

A. The Weibull Distribution and Percolation Theory

Projection of dielectric lifetime of a product from data collected by stressing test structures under accelerated test conditions requires a number of correct models and assumptions. The voltage and temperature must be accurately extrapolated from the accelerated test conditions. Scaling from the area of the test structure to that of the product must be performed with the proper model. Finally, the choice of the failure distribution must be correct, especially, since the 100 ppm level is usually specified requiring accurate estimation of the low failure rate tails.

Log-normal statistics have been used for some time to fit reliability data from accelerated life tests to induce various failure mechanisms such as electromigration and oxide breakdown. There has been discussion concerning the validity of log-normal statistics for thin oxide breakdown. Although log-normal statistics may fit failure data over a limited sample set, it has been demonstrated that the Weibull distribution more accurately fits large samples of TDDB failure data (>4000 devices), particularly, at low failure rates [31]. Fig. 7 illustrates the differences of the fit between log-normal and Weibull statistics for data reported in [61]. More importantly, log-normal statistics does not predict the observed area dependence of t_{BD} for ultrathin gate oxides. Furthermore, the Weibull shape parameter (β) is experimentally observed to decrease as the oxide thickness is decreased. As will be discussed in the following, a model based on percolation theory has been proposed to explain the oxide thickness dependence of β and how it relates to N_{BD}, the number of defects at breakdown.

One of the real breakthroughs in the understanding of the statistical nature of ultrathin oxide breakdown is the idea that a critical number of defects must be generated in the film before catastrophic failure. The first statistical model was formulated by Suñé [62] and described oxide breakdown and defect generation via a Poisson process. Dumin [63] incorporated the model to describe failure distributions in thin oxides. Degraeve [64] later used percolation theory to describe the statistical process of breakdown. The parameters used to fit experimental data is the trap radius and the fraction of defects effective in initiating breakdown. Stathis [65] used a computer simulation to demonstrate the thickness dependence of N_{BD} using percolation theory.

Fig. 8 illustrates the percolation model where defects are generated randomly throughout the volume of the oxide film (shown by open circles in frame 1). As defect generation continues, defects can connect electrically to the anode, cathode, or to nearest neighbors shown as shaded circles in frame 2. Breakdown occurs when a "percolation filament" is formed that connects the anode and cathode in frame 3. Note it is clear that if the oxide is made thinner a percolation path can result with a lower defect density (for example, if the anode and cathode are drawn closer in frame 2). A device with a larger area would also have a higher probability of having overlapping defects for the same oxide thickness and defect density. Therefore, the observed area dependence of oxide breakdown can also be accounted for in this statistical model.

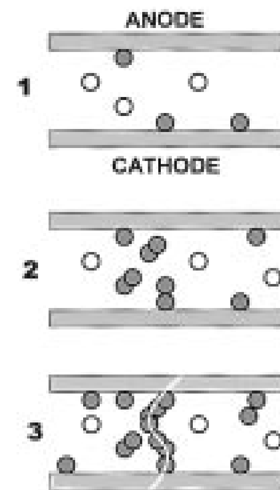

Fig. 8. Series of schematics illustrating the percolation of defects and ultimate breakdown in ultrathin gate oxides. Oxide traps (circles) are generated randomly throughout the volume of the dielectric in step 1. If two neighboring traps overlap or are in contact with one of the electrodes conduction is possible (shaded circles shown in step 2). Breakdown occurs when a conducting path is created from one interface to another shown in step 3.

It should be mentioned that although the percolation concept predicts many of the statistical features of ultrathin oxide breakdown, the parameters chosen such as the defect size and density may not relate to the actual defect's physical dimensions, density, and range of interaction. For example, the defect density used in the percolation model has been shown to differ by a factor of 1000 when compared to the defect density determined by SILC measurements [65]. Also, defect generation may not be truly random in some structures where gate edge effects dominate breakdown.

The effect of oxide thickness on β is shown in Fig. 9. Note that the failure distribution becomes wider (smaller β) as the oxide thickness is reduced. This is a direct result of the value of N_{BD} decreasing with oxide thickness [65]. The smaller Weibull slope for thinner oxides is explained as the conductive path in the thinnest oxides consists of only a few traps (smaller N_{BD}) and therefore has a larger statistical spread. It should be mentioned that percolation theory predicts that only one defect is necessary to initiate breakdown as oxide thickness approaches the diameter of a single defect. Such a circumstance corresponds to a β equal to one [64], [65].

N_{BD} is assumed to be independent of gate voltage, a requirement for extrapolating oxide life from accelerated stress conditions. Reports have demonstrated a voltage independent N_{BD}

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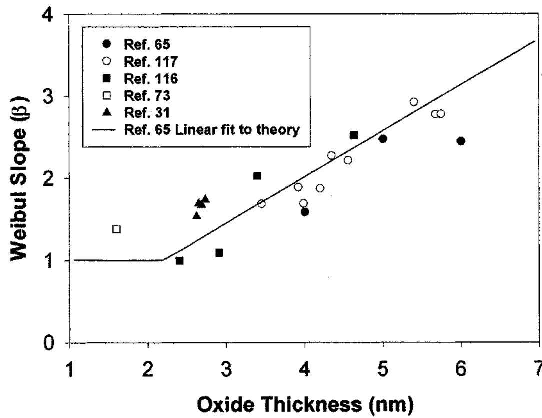

Fig. 9. Weibull shape parameter (B) as a function of oxide thickness from various studies [31], [65], [73], [116], [117]. The B becomes larger as the oxide thickness is decreased. This is a statistical consequence of the number of defects for breakdown becoming less for thinner gate dielectrics resulting in a larger dispersion of the failure distribution.

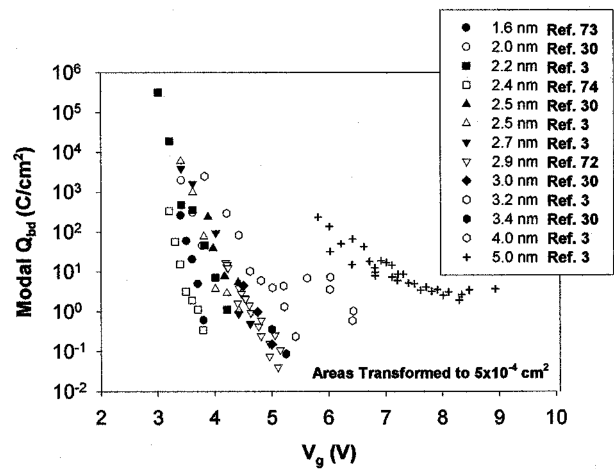

Fig. 10. Charge-to-breakdown (Q_{BD}) plotted as a function of gate voltage compiled from data reported in the literature. The voltage acceleration (or slope of the Q_{BD} versus V_g plot) appears to be increasing for thinner gate oxides. This trend is due to the voltage acceleration increasing for smaller gate voltages, as discussed in the text.

[30], [46], [64], [66] based on measurable electrically active defects such as interface trap density (D_{it}), SILC, etc. Recently, it has been reported that N_{BD} was increased for very long stress times [67] and under alternating bias stress [68]. Other reports indicated a decreasing N_{BD} for decreasing stress voltage [35], [69], [70]. More studies are required to understand the exact relationship between electrically measured defects and those that lead to oxide wear-out and eventual breakdown.

The Weibull distribution is an extreme value distribution and is an acceptable choice for gate oxide breakdown since a microelectronic chip is considered failed if any area of the gate dielectric breaks down (i.e., a weakest link approach). One of the properties of Weibull statistics is a shift of the distribution with device area. Area scaling of charge-to-breakdown Q_{BD} has been defined as follows [64], [65], and [71]:

$$\frac{Q_{BD1}}{Q_{BD2}} = \left[\frac{A_2}{A_1}\right]^{1/\beta}.$$

It is very important to accurately assess the value of β since a large error in extrapolated lifetime can result if an incorrect value is used in the area scaling as indicated above. It has been suggested that β be extracted from the power law dependence of Q_{BD} on area rather than from a single Weibull distribution [25]. Note that the discussion above considers only *intrinsic* or single mode failures. Weibull distributions could exhibit nonlinearity or curvature if *extrinsic* or process-induced defects are present in the population resulting in bimodal or multimodal behavior. In this case, area scaling and reliability extrapolation could be very difficult.

Wu *et al.* [61] showed that a nonlinear Weibull distribution was observed due to nonuniform oxide thickness when area scaling was applied to t_{BD} data collected from test structures of various sizes to produce a single distribution. The effect of variations in oxide thickness in the sample population could be interpreted as a Weibull distribution with a smaller β yielding more pessimistic projections for oxide reliability. Wu *et al.* demonstrated that the nonlinear effect was less when Q_{BD} data was used [61]. The importance of this result is that it indicates that Q_{BD} not t_{BD} is the controlling factor in ultrathin oxide breakdown. The sensitivity of t_{BD} on oxide thickness is due to the exponential dependence of tunneling current J_g on oxide thickness and $t_{BD} = Q_{BD}/J_g$.

B. Voltage and Temperature Acceleration

Developing a correct physical model is not only necessary for establishing the correct functional dependence of oxide life on voltage and temperature but also for determining the dependence of the acceleration parameters on voltage and temperature. For accurate predictions of time-to-breakdown the voltage acceleration parameter must be precisely known regardless of what physical model is assumed. As researchers reported on the results of reliability tests for ultrathin films, a trend emerged which suggested that the voltage acceleration parameter varied with oxide thickness. This trend is illustrated in Fig. 10. The figure shows Q_{BD} plotted as a function of gate voltage for a variety oxide thicknesses obtained from several studies [3], [30], [72]–[74]. The thinner oxides (1.4–1.6 nm) appear to exhibit a larger voltage acceleration. It was later realized that the voltage acceleration parameter was a function of voltage not oxide thickness [40], [75]. Thinner oxides are tested at lower voltages than thicker oxides. Since the voltage acceleration parameter is larger at the lower voltages it appears that thinner oxides have a larger voltage acceleration.

The increasing voltage acceleration parameter with decreasing voltage was predicted in a detailed physical model as the efficiency of the impact ionization process in AHI becoming less for lower voltages [50], [76], [77]. Other researchers have suggested a "universal" model to explain the changing voltage acceleration where processes like AHI attribute to a $1/E$ dependence at high electric fields and another physical process yielding an E dependence at lower electric fields [51], [78]. It is interesting to note that Alam's AHI model also can explain the observed change of an E dependence to a $1/E$ dependence at higher electric fields with a single mechanism [50].

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The larger voltage acceleration at lower voltages was explained as an increased energy-to-breakdown since dissipated energy required for the production of oxide defects decreases dramatically at low voltages [75]. The larger voltage acceleration parameter may also be a consequence of a larger N_{BD} or a smaller defect generation rate at lower voltages [67]. To account for the voltage dependent voltage acceleration parameter, Wu *et al.* demonstrated that t_{BD} had the functional form of $t_{BD} \sim V^{-n}$ where n was independent of thickness [75]. It was the increased voltage acceleration parameter and the fact that the Weibull β was experimentally observed to be larger than 1 (see Fig. 9) that revised earlier predictions that oxide thickness could not be scaled below 2.2 nm [3].

For some time it was assumed that the temperature dependence of time-dependent dielectric breakdown followed an Arrhenius relationship, i.e., $t_{BD} \sim \exp(E_a/kT)$. Where E_a is a thermal activation energy of the defect generation process. Indeed, the dependence was observed in many early studies of oxide breakdown. E_a was observed to decrease for increasing applied gate voltage or electric field [14], [22], [79] which was predicted by the Thermochemical E model [14]. In some reports the E_a was observed to change with temperature [80]. Later studies reported a non-Arrhenius temperature dependence for ultrathin oxides and a steeper temperature dependence compared to results from earlier studies for thicker oxides [25], [81]–[83]. A strong voltage dependence for temperature acceleration was reported in [79] and it was pointed out that the steeper temperature dependence observed for thinner oxides may be due to the lower voltages used to stress thinner oxides.

It is generally accepted that the temperature dependence of oxide breakdown is in the microscopic details of oxide defect formation, not in the temperature dependencies of the driving forces such as energetic carriers or injected anode holes and trapping (these processes depend slightly or moderately on temperature). More studies are required to complete the understanding of oxide defect formation as a function of temperature.

IV. Challenges in the Characterization of Device Breakdown and Circuit Failure

A. Soft Breakdown

Characterizing the integrity and reliability of ultrathin SiO_2 films has become extremely challenging due to the difficulty in detecting breakdown of soft and noisy breakdown behavior in the current/voltage versus time characteristics of the test sample. Unlike "hard" breakdown, where an abrupt increase in gate leakage or as sudden collapse in the gate voltage can be observed, "soft" breakdown is observed only as a slight change in voltage or current, usually accompanied by noise or signal fluctuations.

"Soft" breakdown and current was first observed in sub-5 nm oxide films [84]. There were several explanations for the observed fluctuations in soft breakdown behavior. The noise was explained as multiple tunneling events via electron traps after critical density of traps developed to trigger breakdown [84]. Farmer [85] explained the fluctuations as a result of trap–trap transport of electrons. Lee *et al.* [86] described that a localized damage was formed in the oxide yielding a thinner oxide.

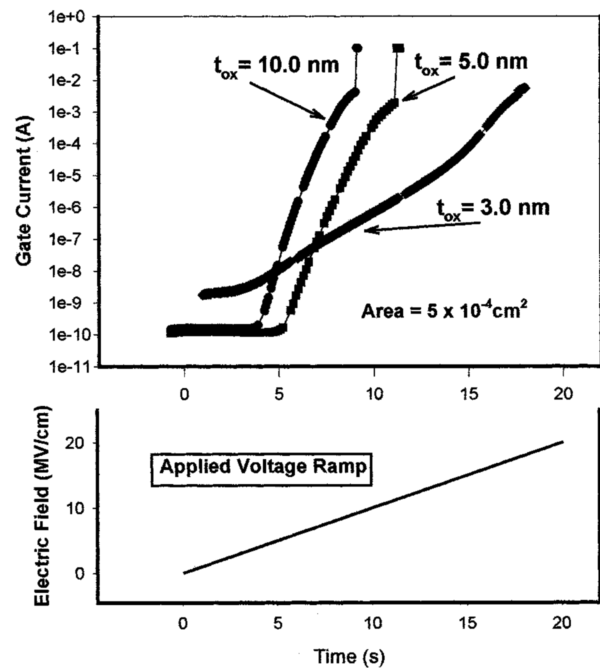

Fig. 11. Top frame of the shows the gate current versus time for a 3.0-nm, 5.0-nm, and a 10.0-nm thick SiO_2 films during a voltage ramp. The voltage ramp is shown in the bottom frame. Note that the breakdown is clearly observed as an abrupt increase in current for the 5.0-nm and 10.0-nm thick films. There does not appear to be an abrupt change in gate current for the 3.0-nm thick film making it very difficult to assign a breakdown voltage.

The noise was the result of dynamic trapping and detrapping. Other models for soft breakdown conduction included variable range hopping [87], a locally modified energy barrier [88], and a network of nonlinear resistors developed through percolation [89]. One of the most successful models for describing post soft-breakdown conduction was proposed by Suñé *et al.* [90]. The model uses a quantum point contact (QPC) to represent the conducting filament that has developed as a result of the percolation of defects. Post breakdown current versus voltage curves have been successfully fitted to the model using two parameters: ϕ, the energy barrier height of the constriction and α, which is correlated to the shape or thickness of the contact [91].

Soft breakdown was described by Bude [39] in the framework of the AHI model as a result of insufficient energy transfer of tunneling electrons to anode holes. A model was also developed by Alam [92] that explains that soft breakdown is the result of limited power dissipation available at the instant of dielectric breakdown. As the oxide ages under constant voltage stress, traps are generated via a percolation process. A percolation path forms after a critical number of traps have been generated that link the gate electrode to the silicon substrate. Current begins to flow through the path and localized joule heating may result in permanent structural damage if the local power dissipation is high enough. The degree of the structural damage is related to the available power dissipation. The occurrence of hard breakdown increases with increasing gate voltage since the power dissipation is related to $V(t)I_{perc}(t)$ [92]. Several experiments illustrated that hard breakdown was more probable in test capacitors if the total stored energy in the test system was increased [93], [94].

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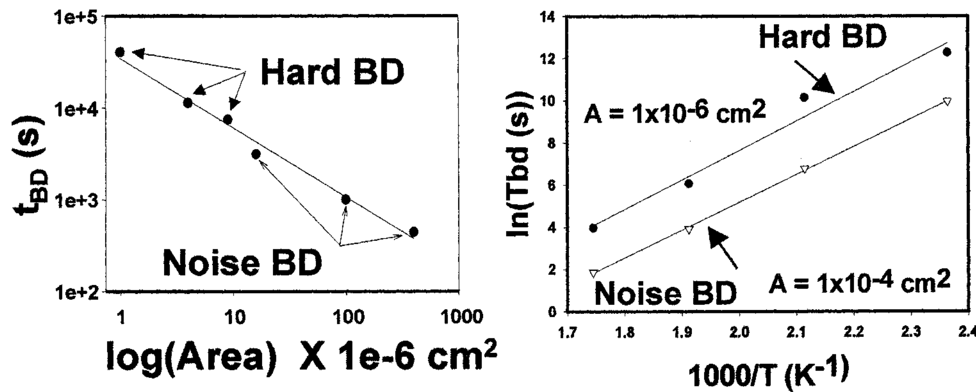

Fig. 12. Left plot shows t_{BD} versus log (Area) for device areas between 1×10^{-6} cm^2 and 4×10^{-4} cm^2. Note that both hard breakdown modes breakdown detected by noise fall on the same line. Right plot shows the thermal acceleration at 2.6 V for the 2.0-nm thick oxide for both thermal breakdown and breakdown detected by the onset of current noise. The plots illustrate that both hard and noisy breakdown modes exhibit the same thermal acceleration and area dependence.

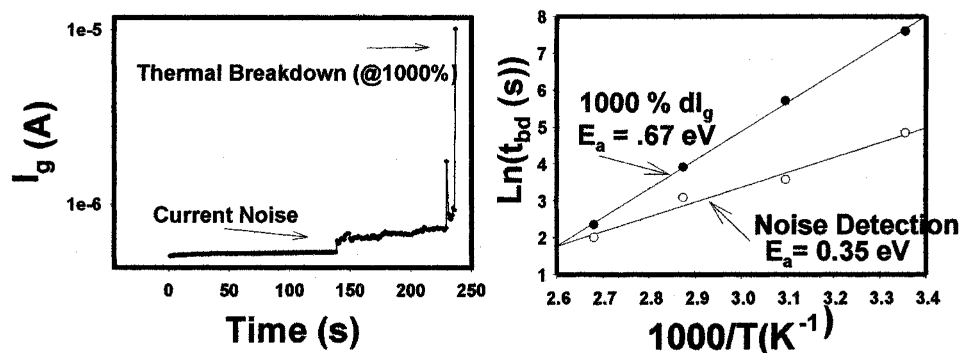

Fig. 13. Left plot shows the occurrence of noise and subsequent thermal breakdown for a 2.5 nm thick device stressed at 4.2 V. Right plot shows the thermal activation energy can be different depending on which failure mode is used to define breakdown.

Fig. 11 illustrates the difficulty in detecting breakdown in ultrathin films in a standard voltage ramp test. The top frame of the figure shows the gate current versus time for a 3.0-nm, 5.0-nm, and a 10.0-nm thick SiO_2 films during a voltage ramp. The voltage ramp is shown in the bottom frame. Note that the breakdown is clearly observed as an abrupt increase in current for the 5.0-nm and 10.0-nm thick films. There does not appear to be an abrupt change in gate current for the 3.0-nm thick film making it very difficult to assign a breakdown voltage.

The occurrence of soft breakdown increases as the stress voltage is decreased and it also seems that the breakdown is harder for devices with smaller areas. Breakdown in smaller area devices is easier to observe since the tunneling current is substantially less than in larger area devices. The increase in current due to the conduction in the percolation path would then be easier to observe. It is assumed that area of percolation defect path (and the amount of current flowing through it) is independent of device area and is only related to the instantaneous power dissipation during the breakdown event [92], [95].

Recently, there has been controversy if soft and hard breakdown resulted from different physical origins. It has been reported that the voltage and temperature acceleration parameters obtained from devices that experienced soft breakdown were different from those obtained from devices that experienced hard breakdown [96], [97]. It was shown by Suñé [98] through statistical analysis that both hard and soft breakdown share a similar origin. The study indicated that soft breakdown was not a pre-cursor to hard breakdown since the hard breakdown conduction spot usually appeared in a different spatial location. Consistent acceleration parameters were obtained if breakdown was defined as the *first* permanent change in the current versus time characteristic regardless if the change was a hard or soft (or noisy) breakdown [31], [79]. Fig. 12 shows the area scaling (left plot) and the temperature acceleration (right plot) for test devices with a 2.0 nm thick oxide. Data from devices that experienced hard and soft breakdown are combined. The figure shows that the temperature dependence is similar for both sets of devices and the there is no change in the slope (which is proportional to the Weibull β for the area scaling). A similar finding was reported in [31].

The acceleration parameters can be different if the breakdown times are not defined as the *first* event in the current versus time characteristics as illustrated in Fig. 13. The plot on the left of the figure shows the current versus time characteristic for a 2.0 nm test capacitor and indicates where current fluctuations are first detected (*first* event) and the point in time where a 1000% increase in current occurs. The right plot shows the temperature dependence that results from defining the breakdown at these points in time. Note the thermal activation energy is very different in both cases.

It is generally accepted that oxide "wear-out" is the development of a percolation defect path and is detectable as the *first* electrical event observed in the current versus time characteristic. The *first* event can be manifested as a hard thermal break-

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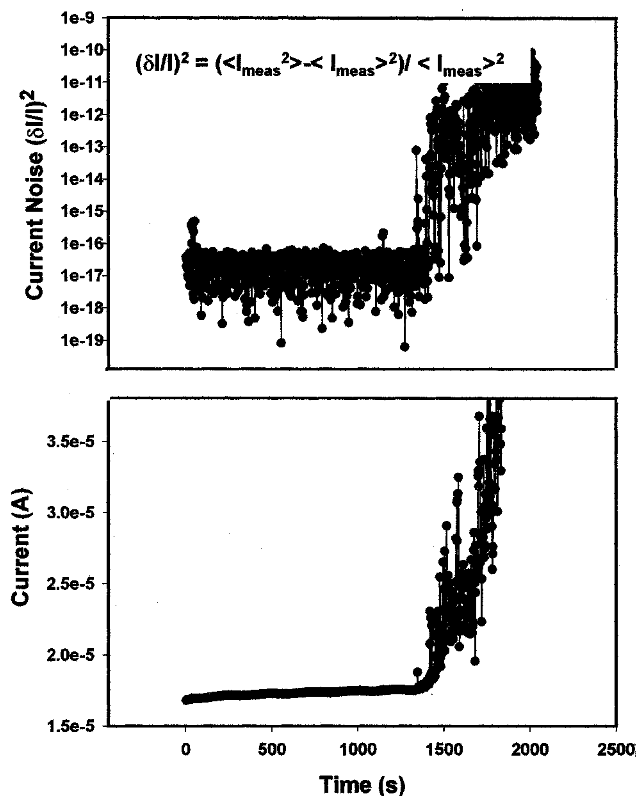

Fig. 14. Top plot shows typical current noise measured during the stress and breakdown of a 2.0-nm film. The noise increases by over four orders of magnitude after breakdown. The bottom plot shows the corresponding current versus time curve. Only a few percent change of gate current is observed at the onset of breakdown.

down or as a soft breakdown depending on stress conditions or device geometry. The implications of soft breakdown on operation of the chip will depend on the application of the device in a particular circuit and will be discussed in Section IV-C.

B. Soft-Breakdown Detection Techniques

The increased occurrence of soft breakdown in ultrathin gate oxides necessitates the development of more sophisticated techniques to detect breakdown, especially in manufacturing environments where system noise levels in automated test equipment may preclude accurate detection by a change of only a few percent in gate current. Weir *et al.* [99] reported that current or voltage noise could be used to reliably detect breakdown. Alers *et al.* [100] used the detection of noise as a robust technique to determine breakdown in current ramp tests. Fig. 14 shows the gate current and accompanying noise as a function of stress time for a 2.0 nm thick gate oxide. Note that the current noise increases by over four orders of magnitude, while the increase in gate current only increases a few percent at the onset of breakdown.

More refined methods for detecting breakdown that eliminate false triggering due to monotonically increasing SILC leakage currents and transient features due to random telegraph signals have been developed [101], [102]. Other techniques based on periodically interrupting the stress voltage and measuring the leakage current at lower voltages have also been successfully used [103]–[105]. The process of periodically interrupting stress did not effect the failure time of the devices [103], [104].

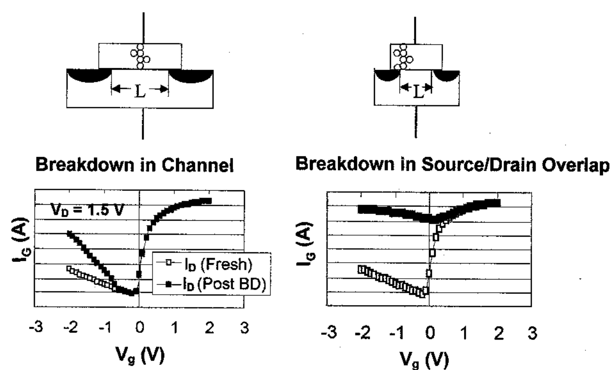

Fig. 15. Drain current versus gate current characteristics reported in [107] for a device experiencing gate to channel breakdown and gate to source/drain overlap region. The gate to source/drain overlap region is much more catastrophic to device operation.

C. Implications of Soft Breakdown for Devices and Circuits

1) Device-Level Failure: There is considerable debate about the implications of soft breakdown on circuit functionality. Weir *et al.* [99] concluded that there was no significant degradation observed in the transistor parameters V_T and g_m following soft breakdown and indicated that perhaps only analog circuitry would be affected by an increased gate current noise. Similar findings were reported on the effect of soft breakdown on transistor performance if the breakdown spot was not located in the device's source or drain region [103], [106], [107]. It was shown in [106] that hard breakdown and catastrophic device failure occurred more frequently as the channel length of the device was decreased. This was explained as a result of the source and drain regions dominating more of the channel area as the channel length is decreased, increasing the probability of a breakdown occurring the source and drain. Degraeve *et al.* [108] also found that only breakdowns that occurred over the source and drain extension regions destroyed device functionality. However, these overlap breakdowns made up only a small fraction all breakdowns suggesting that reliability specifications could be weakened. A breakdown in the MOSFET source or drain has a far greater impact on device operation as shown in Fig. 15 [107]. The reverse leakage current increases by over four orders of magnitude when the breakdown spot is located in the overlap regions of the device. The switching functionality of the device is therefore lost.

2) Circuit-Level Failure: Whether soft breakdown will cause a complex integrated circuit to malfunction is still an open question. Studies performed by Linder *et al.* [109] simulated breakdowns in n-channel MOSFETs that would occur in actual circuit operating conditions by limiting the available current. Such a condition exists in a variety of circuit architectures since most MOSFETs are driven by other MOSFETs. The results showed that the postbreakdown leakage current was a strong function of the current available during breakdown indicating that short channel MOSFETs would probably survive under actual circuit operating conditions.

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Another study performed by Kaczer *et al.* [110] showed that a ring oscillator circuit continued to function even after several devices comprising the circuit experienced breakdown. The increased leakage current in the ruptured devices affected the frequency of oscillation, standby current, and dynamic supply current, however, the logic operation was not destroyed.

Additional studies are required to assess soft-breakdown in complex integrated circuits. Even if the circuit survives the first breakdown event because the conductance of the gate current in the affected device is limited, the continued functionality of the circuit depends on the stability of the leakage path. It is therefore not only important to understand the physical nature of the locally damaged region in the oxide immediately following breakdown, but the voltage and temperature dependence of subsequent postbreakdown changes in oxide conductance. Only after these studies are conducted will the implications of soft breakdown on circuit functionality be fully understood.

V. Conclusions and Implications for Alternative Gate Dielectrics

The present understanding of wear-out and breakdown inltra-thin (<5 nm) SiO_2 gate dielectric films and issues relating to reliability projection have been reviewed. Results from substrate hot-electron injection studies and polysilicon gate electrode doping experiments suggests that tunneling electrons with energy related to the applied gate voltage are the driving force for defect generation and breakdown in ultrathin gate oxides. Accurate reliability projection necessitates the use of a voltage-driven model rather an electric field-driven model.

The theory of percolation has been very successful in describing the breakdown statistics in ultrathin SiO_2 films. The concept of a critical number of defects to initiate breakdown (N_{BD}) has been used to explain the area dependence of breakdown and the decrease of the Weibull shape parameter β with decreasing oxide thickness. It is expected that these concepts can be used successfully when predicting the reliability of alternative (high-κ) dielectric films. Since high-κ films will be thicker than pure SiO_2 for the same equivalent thickness [111], the N_{BD} and the Weibull β may be expected to be larger. However, since some of the alternative gate dielectric systems will involve multiple interfaces, defect generation may occur nonuniformly at different interfaces. It has been shown by Stathis [65] that nonhomogenous defect generation would result in a reduced value of β.

It will also be important to consider polarity effects in the breakdown distributions of multi-stack dielectrics. Vogel *et al.* [112] showed that stacked dielectrics show polarity asymmetry due to the asymmetry of the band diagram. The magnitude of the tunneling current can be very different depending on what energy barrier the electrons encounters first.

Reliability projection will always be as accurate as the voltage and temperature acceleration parameters that must be determined from experimental data. It was shown for ultrathin SiO_2 films that the voltage acceleration increased for decreasing voltage and the temperature acceleration appeared to be non-Arrhenius. It will be necessary to re-examine the voltage acceleration for alternative dielectric systems. As an example, Degraeve *et al.* [113] pointed out that the thin SiO_2 layer determined the reliability characteristics in a Ta_2O_5/SiO_2 stack at high voltages since the electrons were injected over the Ta_2O_5 barrier.

Finally, the implications of gate dielectric breakdown on circuit performance and survivability must be assessed. Soft breakdown in ultrathin dielectric layers will limit the postbreakdown gate conductance. It has been shown that the logic function was not destroyed in some circuits even after several MOSFETs comprising the circuit experienced dielectric breakdown. Soft breakdown in alternative dielectric systems will still be operative since the transient power dissipation available during the breakdown event may be limited by low operating voltages.

In conclusion, ultrathin SiO_2 or oxynitrides will most likely be used for some time as the gate dielectric for advanced microelectronic devices. If the increased tunneling current can be tolerated, films with decreasing thickness should exhibit adequate reliability if the voltage acceleration factor continues to increase as the gate voltage is scaled to lower values. Reliability margins could also increase if the effect of soft breakdown on circuit performance in adequately understood.

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