RFIC Projects


We have some of these parts in plastic packages. Examine pp. 9.42-9.44 of Experimental Methods in RF Design for typical interface circuitry. Draft and lay out a board to be fabricated in the EPL that includes protection circuitry for the ESD sensitive I and Q IF ports and RF and LO ports.

Make a list of specifications that may be tested, and sketch a test plan and associated circuitry.

Design a 360 degree LO phase rotation network using this RFIC.

Design a low power Near Zero IF wireless link to be built using these parts.

Introduction to The FR4IC Project

There are two difficulties with using common semiconductor processes in the classroom in 2013:

1. There are very long time delays between completing an initial design and having actual silicon to test.

2. The industry standard simulation, layout, and validation tools are prohibitively expensive and model libraries are exclusive.

However, once acquired, the basic knowledge and skills required of an analog or RFIC designer may be easily transferred between processes. A skilled CMOS designer quickly comes up to speed on a BiCMOS process, and a GaAs RFIC designer can attend, understand, and contribute to a design review for RF CMOS. What is needed for education and resume building is an IC process that enables quick-turn designs using accessible and open-source tools.

One way to meet these goals is to treat FR4 with surface mount components as an IC process. We proceed through the design, simulation, layout, parasitic extraction, LVS and DRC, Critical Design Review, fabrication, bench evaluation, compliance matrix, redesign, fab, test etc. steps exactly as with one of the usual semiconductor processes, but much faster and cheaper.