Impact Ionization

I-I occurs at the drain side in the high-field region. Two effects: kink effect and hot electron degradation.

Kink effect not normally found in bulk devices, except at very low temperatures (contacts to wells must be provided). Hot-electrons appear in short channel devices.

Fig for illustration of kink effect. Can be strong in n-channel, but usually absent in p-channel. Device must be PD SOI, i.e. there exists a neutral body region underneath the gate. Due to I-I, e-h pairs are created at drain end. Electrons enter the drain side quickly, but holes go to the place of the lowest potential, which in this cas means the floating body.

Hole current accross S-B junction can be presented as a regular diode current $I_{holes} = I_{so}(\text{exp}(qV_{BS}/(nV_{therm}) - 1$. Not quite that simple to solve since I_{holes} depends on variety of parameters. The potential in the body region must adjust to a level that corresponds to the new hole concentration. Here that means reduction of the barrier S-B. (see figs)

The increase of body potential decreases the threshold voltage (see the eqs for bulk case vs. V_B, i.e. body effect). Instead of back gate bias, it is now the body potential that changes V_{th} . At the point where the body potential is sufficiently increase, V_{th} drops and current suddenly increases.

Things can get worse in PD SOI if transistor action is triggered.

In FD SOI, drain voltage results in smaller fields, and less I-I is present. Holes again move towards source. However, the barier S-B is already low due to full depletion of the body region. The holes can readily recombine in the source. There is no need for potential adjustment and V_{th} does not change with increase in hole current.

FD SOI device does not exhibit kink effect, unless the back interface is accumulated in which case it looks like PD and the kink effect re-appears. p-channel devices better in this respect since the impact ionization coefficient is much smaller for holes (in Si, but not other materials). In bulk devices, generated holes recombine at the substrate or well contact. If wells are not contacted or Si becomes highly resistive (low temp.) kink effect can appear. In PD SOI, body contact alleviates kink effect somewhat. Problem: high resistance.

In addition: S can become smaller than the theoretical minimum. Even small generation can result in charging of the body region and the resulting reduction of the barrier and V_{th} . This results in S reduction (sketch).

Hot Electrons

Very important for reliability. Comes about because of reduction of gate length and accompanying increase in field. Basic argument: field increases since voltages are roughly the same and lengths go down. In addition, doping levels in the body region keep increasing (for V_{th} control etc) resulting in higher fields at junctions.

In saturation mode, high fields exist from the pinch-off point to the drain junction. These accelerate electrons to very high energies and some can overcome the oxide barrier. This results in "damage" to the oxide interface and e.g. V_{th} shifts. High energy also results in I-I; the two are related and hole current can be used to estimate the gate current. The device lifetime

$$\tau \sim \frac{W}{I_D}(M-1)^m \text{ where } I_{body} = (M-1)I_{Dsat} \tag{1}$$

Problem for SOI: what's I_{body}? M can be determined by integrating ionization coefficient (numerically?) to give

$$M - 1 = \frac{A_i}{B_i}(V_{DS} - V_{Dsat}) \exp\left[-\frac{B_i l_c}{V_{DS} - V_{Dsat}}\right] \tag{2}$$

where characteristic length $l_c = t_{Si}\beta C_{Si}/(2C_{ox1}(1+\alpha))$. Accumulated back interface gives $\beta = 1$, and depleted one $\beta = 1 + C_{Si}/(C_{Si} + C_{ox2})$. α is as before.

For results on (M-1) see fig. It indicates that device lifetimes should be longer for FD SOI devices. Back accumulation, however, can screw everything up. Further optimization via Si film thickness. Thicker films better, so long as FD is kept.

Bipolar Effects

Any MOSFET has a parasitic BJT built in. In bulk, base is grounded; in SOI it floats. Results in: anomalous subthreshold slope and BV reduction.

For V_{DS} high ehough, I-I occurs, but for $V_G < V_{th}$ the current is small. The effect proceeds as in previous discussion of kink effect: holes are generated as some small currents starts flowing, they collect around source forward biasing that junction and reducing the body potential, which results in reduction of V_{th} . S becomes smaller than 60 mv/decade. Occurs only in PD or FD with back accumulation.

Additionally, BJT may contribute through current gain β that amplifies the base current (I-I generated hole current). $\Delta I_D = \beta I_{body} = \beta(M-1)I_{ch}$ (see fig.) Possible positive feedback and resulting reduction in S. AKA single transistor latchup.

Further explanation: fig . Under low V_{DS} the current trace is normal in both directions. Trace b is for larger V_{DS} and as explained above results in very steep slope. This does not go indefinetely since as body potential is increased, saturation voltage is increased leading to reduced fields and smaller I-I generation.

On the reverse voltage sweep, large V_{DS} keeps the body voltage high and the V_{th} stays low resulting in high current. Once the feedback cannot be maintained ($\beta(M-1) < 1$) current drops to the curve for larger V_{th}. Hysteresis is observed in the curve. For even larger V_{DS} once the device is turned on it cannot be turned off.

Not observed if body grounded (holes have an exit route), and should be reduced (eliminated?) in the FD device.

Reduced Breakdown

SOI devices show lower drain fields than their bulk counterparts and we may expect improvement in BV. Problem: existance of parasitic BJT.

For PD, BJT has an open base and from BJT theory we know (?) that $BV_{CEO} = BV_{CBO}\beta^{1/n}$ with n between 3 and 6. We can also write $\beta \approx 2(L_n/L_B)^2 - 1$ with base width equal to gate length. Assuming that $BV_{CEO} = BV_{DS}$ we get

$$BV_{DS} = \frac{BV_{CBO}}{\left(\frac{2D_n\tau_n}{L^2} - 1\right)^n} \tag{3}$$

See fig for graphs. Valid only for large β.

Not a problem for bad material! Those have short lifetimes and current gain is low. Problem: FD analysis. Strangely enough, papers have appeared that argue for inverse dependence of β on hole concentration (paper). β and M are both non-linear functions of drain voltage. The dependence is opposite: M increases with V_{DS} while β decreases (high injection)

Suggestions for better BV: LDD/LDS structures, reduced lifetimes, body contacts.

Accumulation-mode p-MOSFET

Complicated devices! While enhancement p-MOSFETs are possible, when n^+ gate and thin oxide is used, V_{th} comes out to be large. To reduce V_{th} , in FD SOI we use p-type substrate. The device is accumulation mode device.

For no gate voltage, body is fully depleted (positive interface charge and negative Φ_{MS}). When gate voltage turned on, accumulation occurs and conduction starts, but not just in the channel!

$\Phi_{MS} = -E_g/2 - V_{therm}\ln(N_a/n_i)$. With more negative V_G hole concentration increases until $\Phi_{s1} = 0$. This is flat band condition for V_{G1}: $V_{th,acc} = \Phi_{MS1} - Q_{ox1}/C_{ox1} = V_{fb1}$.

Along the accumulation channel, charge changes as

$$Q_{acc}(y) = -[V_{G1} - V_{fb1} - V(y)]C_{ox1} \tag{4}$$

From gradual channel approximation:

$$\int_0^{V_{DS}} dV = I_{acc}\int_0^{L} dR(y) \text{ with } dR(y) = \frac{dy}{W\mu_s Q_{acc}} \tag{5}$$

$$I_{acc} = (W/L)\mu_s C_{ox1}\left((V_{G1} - Vfb1)V_{DS} - V_{DS}^2/2\right) \text{ for } V_{DS} > V_{G1} - V_{fb1} \tag{6}$$

$$I_{acc} = (W/L)\mu_s C_{ox1}/2(V_{G1} - Vfb1)^2 \text{ for } V_{DS} < V_{G1} - V_{fb1} \tag{7}$$

There are other components to the total current — body current. Somewhat similar to JFET current since the current flow occurs in the neutral part of the body and the widht of the conduction path is modulated by the depletion zones stemming from top and bottom gates.