From expressions for $Q_{inv}(\Phi_{s1}(y))$ and the integral for I_D:

$$I_{D,acc2} = \frac{W \mu_n C_{ox1}}{L}\left[\left(V_{G1} - V_{th1,acc2}\right) V_{DS} - \left(1 + \frac{C_{Si}}{C_{ox1}}\right)\frac{V_{DS}^2}{2}\right] \tag{1}$$

To obtain drain saturation voltage set $dI_D/dV_{DS} = 0$:

$$V_{DS,acc2} = \frac{V_{G1} - V_{th1,acc2}}{1 + C_{Si}/C_{ox1}} \tag{2}$$

which leads to expression for saturation current:

$$I_{Dsat,acc2} = \frac{W \mu_n C_{ox1}}{2L(1 + C_{Si}/C_{ox1})}\left(V_{G1} - V_{th1,acc2}\right)^2 \tag{3}$$

the denominator can be represented by $(1+\alpha)$, where $\alpha = C_{Si}/C_{ox1}$.

Back interface depleted from source to drain (DS+DD): back gate voltage must be between the voltages for accumulation and inversion $V_{G2,acc} < V_{G2} < V_{G2,inv}$. For inversion on back gate use $\Phi_{s2} = \Phi_{s1} = 2\Phi_F$ and $Q_{s2} = 0$.

$$V_{G2,inv} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox2}} \tag{4}$$

For back surface in depletion: $Q_{s2}(y) = 0$ and from eqs. for $I_D, Q_{inv}, \Phi_{s2}(y)$

$$I_{D,depl2} = \frac{W \mu_n C_{ox1}}{L}\left[\left(V_{G1} - V_{th1,depl2}\right) V_{DS} - \left(1 + \frac{C_{Si} C_{ox2}}{C_{ox1}\left(C_{Si} + C_{ox2}\right)}\right)\frac{V_{DS}^2}{2}\right] \tag{5}$$

Saturation voltage and current are obtained as before:

$$V_{Dsat,depl2} = \frac{V_{G1} - V_{th1,depl2}}{1 + \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si}+C_{ox2})}} \tag{6}$$

$$I_{Dsat,depl2} = \frac{W\mu_n C_{ox1}}{2L\left(1 + \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si}+C_{ox2})}\right)} \left(V_{G1} - V_{th1,depl2}\right)^2 \tag{7}$$

More complicated case: back interface accumulated near source and depleted near drain (AS+DD). Starting point for current calculation:

$$I_{D,AS+DD} = -\frac{W\mu_n}{L}\left[\int_{2\Phi_F}^{\Phi_{s1}(y_t)} Q_{inv1}(y)d\Phi_{s1}(y) + \int_{\Phi_{s1}(y_t)}^{2\Phi_F+V_{DS}} Q_{inv1}(y)d\Phi_{s1}(y)\right] \tag{8}$$

$$\Phi_{s1}(y_t) = 2\Phi_F + \frac{C_{ox2}}{C_{Si}}\left(V_{G2,acc} - V_{G2}\right) \text{ where } \Phi_{s2}(y_t) = Q_{s2}(y_t) = 0 \tag{9}$$

Solving these equations results in long formulas for $I_{D,AS+DD}$ and saturation voltage and saturation current. These depend explicitly on back gate voltage.

A common thread for saturation current in thin film (and bulk) devices (FD with depleted or accumulated back interface):

$$I_{Dsat} = \frac{W\mu_n C_{ox1}}{2L(1+\alpha)}(V_{G1} - V_{th})^2 \tag{10}$$

where $\alpha = C_{Si}/C_{ox1}$ for FD with accumulated back interface, and $\alpha = C_{Si}C_{ox2}/[C_{ox1}(C_{Si} + C_{ox2})]$ for FD with depleted back interface. Similar eqs. for AS+DD back interface. Bulk MOSFET follows the same equation but $\alpha = C_D/C_{ox}$ where C_D is the capacitance of the depleted layer $C_D = \epsilon_{Si}/x_{dmax}$. Threshold voltage depends on the mode of operation, but if that variation is neglected, I_{Dsat} differs primarily through α.

Since $C_D < C_{Si}$ (why?) $\rightarrow \alpha_{bulk} < \alpha SOI, acc2$. Furthermore, $\alpha_{SOI,dep2} <$ $\alpha bulk$ (why?)

α represents the ratio C_b/C_{ox1} where C_b is the capacitance between the front channel and back-gate; it is equal to depletion capacitance for bulk device, to Si layer capacitance for accumulated back interface, and to series combination of Si layer and back gate oxide capacitance for depleted back interface.

$\Rightarrow$ Increased saturation current in FD SOI brings about better current drive and increase in speed! (see fig). We also need to look at g_m and μ.

Transconductance

By definition $g_m = dI_D/dV_G$ with V_D constant and $V_D > V_{Dsat}$ (for saturation region). From expressions for I_{Dsat}:

$$g_m = \frac{W\mu_n C_{ox1}}{L(1+\alpha)}(V_{G1} - V_{th}) \tag{11}$$

Because of the relative magnitudes of α, g_m is largest in FD SOI with depleted back-interface.

Mobility

Experimentally (and theoretically as well) it s found that:

$$\mu_n(y) = \mu_{max}\left(\frac{E_c}{E_{eff}}\right)^c \text{ for } E_{eff}(y) > E_c \tag{12}$$

The parameters will depend on orientation and oxidation, but not on the doping or back-gate bias. E_{eff} is some "effective" field that acts on carriers in inversion channel $E_{eff} = (Q_{depl} + \eta Q_{inv})/\epsilon_{Si} + E_{s2}$. (more coplex stuff in text)

Effective mobility measured from currents at small drain voltages so that $\mu_{eff} = I_D/[Q_{inv}V_D(W/L)]$. (obviously many approximations)

Since Q_{depl} is smaller in FD devices relative to bulk, around the threshold voltage there is a smaller field in SOI devices than in their bulk counterparts $\rightarrow$ higer mobility. Looking at fig for el. fields in FD and bulk device, the difference is obvious.

For depletion on back interface, the real thickness controlled by the front gate is x_1 and not t_{Si}.

For accumulated back interface we cah have large fields than in bulk. As V_{G1} is increased the inversion layer charge takes over and there is no improvement in mobility. Reduced field also means wider channel with resulting decrease in surface scattering and improved mobility.

Subthreshold Slope

Defined as $S = dV_G/d(\log I_D)$ (see fig). By definition, conc. of carriers in channel is much smaller than the background doping $\rightarrow$ minority carrier transport. In this case it is diffusive current (similar to BJT)

$$I_D = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L)}{L} \tag{13}$$

standard expressions for concentrations: $n(0) = n_{p0} \exp(\Phi_s / V_{therm})$, and $n(L) = n_{p0} \exp(\Phi_s - V_D)$.

The thickness through which carriers flow is $d = V_{therm}/E_s = V_{therm}/(-d\Phi_s/dx)$. Plug all this into I_D and use Einstein's relationship $D_n = V_{therm}\mu_n$:

$$I_D = \left(\mu_n (W/L) q V_{therm}^2 \frac{n_i^2}{N_a} \left[1 - e^{V_D / V_{therm}} \right] \right) \frac{e^{\Phi_s / V_{therm}}}{-d\Phi_s/dx} \tag{14}$$

The slope is then given by

$$S = \frac{\ln(10)}{\frac{d \ln I_D}{dV_G}} = \frac{\ln 10}{\frac{1}{I_D}\frac{dI_D}{d\Phi_s}\frac{d\Phi_s}{dV_G}} = \frac{\ln(10)}{C\frac{d\Phi_s}{dV_G}} \tag{15}$$

$$C = V_{therm}^{-1} - \frac{\frac{d}{d\Phi_s}\left(-\frac{d\Phi_s}{dx}\right)}{-\frac{d\Phi_s}{dx}} \tag{16}$$

the second term in C accounts for reduction of I_D increase due to the increase of the surface field with increasing surface current. We will neglect it (for the most part).

For bulk we have $E_s = -d\Phi_s/dx = \sqrt{2qN_a\Phi_s/\epsilon Si} = qN_a/C_D$ where C_D is depletion capacitance. Also, nominator in the correction factor for C is C_D/ϵ_{Si} so that the full C is $1/(2\Phi_s)$.

If we look at eq. circuit for this we have a series combination of C_{ox} and C_D (picture). In ac case, the ratio of $\tilde{\Phi}_s$ to $\tilde{V_G}$ is the ratio of impedance of C_D to the total impedance. that leads to

$$\frac{d\Phi_s}{dV_G} = \frac{C_{ox}}{C_{ox} + C_D} \text{ and } S = V_{therm} \ln(10)\left(1 + \frac{C_D}{C_{ox}}\right) \tag{17}$$

where we have neglected interface charge and the correction factor in C.

For SOI we can start with expressions for V_{G1}, V_{G2} and eliminate Φ_{s2} to get dependence of Φ_{s1} on appl. voltages. This in turn can be used to find $d\Phi_{s1}/dV_{G1}$ (assume no back channel conduction), giving the final expression to plug into S.

Alternatively, represent this with a series combination of C_{ox1}, C_{Si}, C_{ox2} (picture) Same logic as for bulk gives directly

$$\frac{d\Phi_{s1}}{dV_{G1}} = \frac{\frac{1}{C_{ox2}} + \frac{1}{C_{Si}}}{\frac{1}{C_{ox2}} + \frac{1}{C_{Si}} + \frac{1}{C_{ox1}}} \tag{18}$$

Again, C can be neglected. Since $C_{ox2} \ll C_{ox1}$ and $C_{ox2} \ll C_{Si}$, above expression goes to unity so that $S \approx V_{therm} \ln 10$.

S lower (i.e. better) in FD SOI. Theoretical minimum $S = 60$ mV/decade. Here we have perfect coupling between V_{G1} and Φ_{s1}. (see fig.) What about accumlated back interface? Look at the capacitances again.

Generally, $S = V_{therm} \ln(10)(1 + \alpha)$ as for the saturation currents. With maller S we can afford lower threshold voltages.