For back surface depleted $\Phi_{s2} \epsilon (0, 2\Phi_F)$. To evaluate V_{th} we need the voltage $V_{G2,acc}$ where the back surface becomes accumulated $(\Phi_{s1} = 2\Phi_F, \Phi_{s2} = 0, Q_{s2} = 0)$:

$$V_{G2,acc} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} - \frac{C_{Si}}{C_{ox2}} 2\Phi_F - \frac{Q_{depl}}{2C_{ox2}} \tag{1}$$

We also need the voltage at which back surface is inverted $(Q_{s2} = 0, \Phi_{s1} = \Phi_{s2} = 2\Phi_F)$:

$$V_{G2,inv} = \Phi_{MS2} - \frac{Q_{ox2}}{C_{ox2}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox2}} \tag{2}$$

When $V_{G2,acc} < V_{G2} < V_{G2,inv}$, front V_{th} varies as:

$$V_{th1,depl2} = Vth1, acc2 - \frac{C_{Si} C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} (V_{G2} - V_{G2,acc}) \tag{3}$$

Assumption: inversion and accumulation layers are neglegibly thin. See fig for whole range of V_{th} .

Qualitative behavior of I_D vs. V_{G1} with V_{G2} as parameter is shown on fig. V_{DS} is small (linear regime).

In the left part: back surface is inverted (no use). Back surface potential $\Phi_{s2} \approx 2\Phi_F$ and V_{th1} is independent of V_{G2} and fixed. The curves shift UP (not left) since current at back surface increases with increase of V_{G2}.

At the far right: back surface accumulated ($\Phi_{s2} \approx 0$) and V_{th1} is constant and independent of V_{G2}. No more shifts to right can be obtained.

In region B (depleted back surface): V_{th1} depends linearly on V_{G2} and the curves shift to the right as V_{th1} increases with more negative V_{G2}.

One additional effect: just as V_{G2} changes V_{th1}, so does V_{G1} change V_{th2}! What happens in region a is that while the front surfrace is in depletion region V_{th2} is reduced by increase of V_{G1} and the back surface may start conducting. Interaction works both ways!

Body Effect

For bulk devices: dependence of V_{th} on substrate bias. For SOI: dependence of V_{th} on back-gate bias.

$$V_{th} = \Phi_{MS} + 2\Phi_F + \frac{Q_b - Q_{ox}}{C_{ox}} = \Phi_{MS} + 2\Phi_F + \frac{\sqrt{2\epsilon_{Si} q N_a (2\Phi_F - V_B)} - Q_{ox}}{C_{ox}} \tag{4}$$

Define $\gamma = \sqrt{2\epsilon_{Si} q N_a}/C_{ox}$ so that $V_{th} = V_{th,0} + \gamma(\sqrt{2\Phi_F - V_B} - \sqrt{2\Phi_F})$. γ is body-effect parameter in $\sqrt{V}$.

In FD SOI body effect or back-gate effect:

$$\frac{dV_{th1}}{dV_{G2}} = \gamma = \frac{-C_{Si} C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} = \frac{-\epsilon_{Si} C_{ox2}}{C_{ox1}(t_{Si} C_{ox2} + \epsilon_{Si})} \tag{5}$$

γ is dimensionless for SOI. V_{th} dependence above is linear. Approximation: C_{ox2} is very small (relative to other capacitances). Then $\gamma \approx -t_{ox1}/t_{ox2}$. If buried oxide thickness is much larger than gate oxide (which normally the case) γ is very small. Above valid only for back surface depleted. If back surface is inverted or accumulated $\rightarrow \gamma \approx 0$. (in reality, accumulation and inversion cases are slightly more complicated)

γ independent of N_a and if C_{ox1}, C_{ox2} are known it can be used to find Si film thickness. (note on Si substrate)

For comparison of body effect in SOI and bulk devices see fig. Not entirely academic since some devices DO have sources that are not grounded (as we have assumed), e.g. transfer gates, loads, differential inputs.

More specifically: V_{th} fall-off with gate length reduction. Main cause: loss of control by the gate over a part of the depletion zone below it. Normally, gate controls $Q_{depl} = qN_a x_{dmax}/C_{ox}$ in bulk case, which now shrinks to some fraction Q_{d1}.

The reduction of Q is due to the loss to S and D depletion regions. For geometrical interpretation see fig. In long devices, upper and lower base of the trapesoid are roughly equal; not so in short devices. Approximate value

$$Q_{d1} = Q_{depl}\left(1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2x_{dmax}}{r_j}} - 1\right)\right) \tag{6}$$

r_j is source/drain junction depth.

In SOI see fig. $Q_{d1} = Q_{depl}(1 - d/L)$. Calculating d is not trivial, however. Empirical relationship:

$$Q_{d1} = Q_{depl}\left(1 - \alpha\frac{d_S + d_D}{2L}\right) \text{ and } \alpha = \frac{x_1}{x_{dmax}} \tag{7}$$

d_S, d_D are bases of the triangular charge controlled by S and D in a virtual bulk device with same doping concentration N_a as SOI device. (notes on derivation) x_1 is the depth of the potential minimum $x_1 = t_{Si}/2 + \epsilon_{Si}(2\Phi_F - \Phi_{s2})/(qN_a t_{Si})$. Values for d_S, d_D are approx. by depletion layer depths of S and D junctions

$$d = \sqrt{\frac{2\epsilon_{Si}}{qN_a}(E_g/2 + \Phi_F + V_{app})} \tag{8}$$

To find modified V_{th} , substitute Q_{d1} instead of $qN_a x_{dmax}$ in bulk expression for V_{th} . see fig for results.

If the back surface is accumulated, short channel effects are even smaller (basically, depl. layer width is reduced at back surface)

More short channel effects: drain induced conductivity enhancement. Again due to charge sharing between the gate and the junctions. To analyze it, however, we need 2-D solution to Poisson's equation. It is claimed to be lower in SOI than in bulk devices.

I-V Characteristics

Thick film is the same as bulk, except for the kink effect and parasitic bipolar effects (later).

FD devices: analysis based on gradual channel approximation. Mobility is constant in y direction (parallel to surface), uniform doping in Si, no diffusion current. Starting point:

$$I_D = -W\mu_n Q_{inv}(y)\frac{d\Phi_{s1}(y)}{dy} \tag{9}$$

for a small section of the channel. Integrating from source to drain

$$I_D = -\frac{W}{L}\mu_n \int_{2\Phi_F}^{2\Phi_F+V_{DS}} Q_{inv1}(y)d\Phi_{s1}(y) \tag{10}$$

We need Q_{inv1} as a function of y. See eq. for V_{G1}. The result is:

$$-Q_{inv1}(y) = C_{ox1}\left(V_{G1} - \Phi_{MS1} + \frac{Q_{ox1}}{C_{ox1}} - \left(1 + \frac{C_{Si}}{C_{ox1}}\right)\Phi_{s1}(y) + \frac{C_{Si}}{C_{ox1}}\Phi_{s2}(y) + \frac{Q_{depl}}{2C_{ox1}}\right) \tag{11}$$

Expression for V_{G2} can be used to find Φ_{s2} which is needed in the previous expression.

$$\Phi_{s2}(y) = \frac{C_{ox2}}{C_{ox2}+C_{Si}}\left(V_{G2} - \Phi_{MS2} + \frac{Q_{ox2}}{C_{ox2}} + \frac{C_{Si}}{C_{ox2}}\Phi_{s1}(y) + \frac{Q_{depl}}{2C_{ox2}} - \frac{Q_{s2}(y)}{C_{ox2}}\right) \quad (12)$$

Different cases for back interface: DS+DD = depleted source and depleted drain, AS+AD = accumulated source and accumulated drain, AS + DD, etc

1. AS + AD case . To prevent accumulation at drain end $V_{G2} < V_{G2,acc}(L)$ (ie back gate voltage is larger in magnitude than what is needed to accumulate the surface at drain end, but the sign is negative)

$$V_{G2,acc}(L) = V_{G2,acc} - \frac{C_{Si}}{C_{ox2}} V_{DS} \quad (13)$$

For $V_{G2,acc}$ see earlier eq. Above obtained with $\Phi_{s1}(L) = 2\Phi_F + V_{DS}$ (note on band from S to D). Obviously, $V_{G2,acc}(L) < V_{G2,acc}(0)$.