SOI CMOS Technology

Quick comparison bulk vs. SOI processing (figs)

Isolation: locos (fig); bulk vs. SOI; birds beak; channel stop implant; leakage at corners (why?)

Parasitic transistor in parallel with main one, but smaller width; V_{th} of the two determines the I-V characteristics (fig).

Mesa isolation — strip away any unused Si! Nice in principle, but... Problems again with edge device (gate wraps around the whole Si layer) $\rightarrow$ P^+ implant again needed. Also, reduced breakdown. (fig)

Combination of mesa isolation and LOCOS: oxidized mesa. Increased breakdown, edge transistor taken out, and no regions of very thin Si layer.

Doping concerns: V_{th} adjustment and eliminating back-channel leakage. (note on gate material influence).

Thick vs. thin film. The former allows independent treatment, while thin films are usually too thin to allow separate back-channel implants. (see figs). In thin film devices a trade-off is involved: a) insure that the device is fully depleted, and b) V_{th} is high enough. In addition to doping, Si thickness can be varied. (one measure of mode of operation: subthreshold slope)

Contacts: sheet resistance increase with reduction in thickness $\rightarrow$ use silicides (e.g. Ti). Ti thickness limited by possible shorts to gate and between S and D.

SOI MOSFET Design

Various designs: "normal", edgeless, with body contact, H-gate, body contact at source (see figs). In some situations it is important to avoid edge leakage $\rightarrow$ use edgeless device. Problem: uses larger area.

Why body contact? Either to use as a BJT or to control parasitic BJT. Simple design not always efficient (large R) $\rightarrow$ use H-gate which also takes care of edge leakage (edges only from N^+ to P^+). More compact solution: source contact (also no edges). Problem: asymmetrical. Note: Body contacts only for partially depleted devices; no use for fully depleted.

SOI, in principle, offers higher density (figs), stemming mainly from absence of wells and possibility of direct contact of N^+ and P^+ drains.

Difference vs. bulk: body effect, i.e. V_{th} dependence on substrate bias. This is negligible in PD devices, but can be very pronounced in FD devices.

Back-gate bias in SOI is different from substrate bias in bulk (fig). In bulk p- and n-channel device body regions are connected to the same voltages as their respective source regions $\rightarrow V_{sub} = 0$. In SOI, substrate underneath the back gate is common to n- and p-channel devices and is usually grounded. $\rightarrow V_{sub,p} = -V_{DD}$ (say -5V) and p-channel devices need to operate with this back-gate bias.

SOI MOSFET - Introduction

Main advantage: reduction of parasitic capacitance to substrate (fig). It increases in bulk MOSFET as gate lengths are reduced, but it stays constant in SOI. Some other cap. also reduced in SOI (table).

Two types of devices: Thick- and thin-film; also partially and fully depleted (PD and FD). Fig for explanation.

Bulk device: depletion width $x_{dmax} = (4\epsilon_{Si}\Phi_F/qN_a)^{1/2}$, where Fermi level $\Phi_F = kt/q\ln(N_a/n_i)$.

Thick-film (PD): Si layer is $> 2x_{dmax}$ (to ensure that depl. layers do not touch) $\rightarrow$ no interaction between gates. If a body contact is provided it behaves very similarly to bulk device. If body "floats", it is basically a bulk device with two additional effects: "kink effect" and presence of open-base npn transistor (for n-channel).

Thin-film (FD): Si film always $< x_{dmax}$ except for some thin layer of accumulation or inversion at back-gate interface. Exhibits most interesting properties, e.g. low electric fields, high g_m, excellent short-channel behavior and subthreshold slope. For modes of operation, 9 total, see fig. Back-accumulated interface generally to be avoided. Note: channel can be partially depleted and partially accumulated.

Another type of FD devices: accumulation-mode (vs. enhancement-mode discussed so far), aka deep-depletion. N^+ poly gate: n-channel enhancement, p-channel accumulated. Reverse for P^+ gate.

For summary see table. FD devices best suited for ULSI (?).

Threshold Voltage

Enhancement bulk n-MOSFET:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x_{dmax}}{C_{ox}} \tag{1}$$

where $V_{FB} = \Phi_{MS} - Q_{ox}/C_{ox}$ (neglecting surface states) is flat band voltage, Φ_F is Fermi voltage, and x_{dmax} maximum depletion width. The same expression for PD devices.

FD (see fig): solve Poisson's equation under the depletion approx: $\frac{d^2\Phi}{dx^2} = qN_a/\epsilon_{Si}$, which gives:

$$\Phi(x) = \frac{qN_a}{2\epsilon_{Si}} x^2 + \left(\frac{\Phi_{s2} - \Phi_{s1}}{t_{Si}} - \frac{qN_a t_{Si}}{2\epsilon_{Si}} \right) x + \Phi_{s1} \tag{2}$$

$\Phi_{s1,s2}$ are potentials at front and back interfaces. N_a is assumed constant. Electric field follows directly from above, and at $x = 0$ we have

$$E_{s1} = -\left(\frac{\Phi_{s2} - \Phi_{s1}}{t_{Si}} - \frac{qN_a t_{Si}}{2\epsilon_{Si}} \right) x \tag{3}$$

Applying Gauss' theorem at front and back interfaces we get:

$$\Phi_{ox1} = \frac{\epsilon_{Si} E_{s1} - Q_{ox1} - Q_{inv1}}{C_{ox1}} \tag{4}$$

$$\Phi_{ox2} = -\frac{\epsilon_{Si} E_{s1} - qN_a t_{Si} + Q_{ox2} + Q_{s2}}{C_{ox1}} \tag{5}$$

whereQ_{s2} is charge in back inversion or accumulation layer.

The front and back gate voltages $V_{G1} = \Phi_{s1} + \Phi_{ox1} + \Phi_{MS1}$. Plug in the expression for Φ_{s1}:

$$V_{G1} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox1}}\right)\Phi_{s1} - \frac{C_{Si}}{C_{ox1}}\Phi_{s2} - \frac{\frac{1}{2}Q_{depl} + Q_{inv1}}{C_{ox1}} \quad (6)$$

and similarly for V_{G2}.

We need to specify the conditions at the back interface and investigate V_{th} dependence on back-gate voltage.

Accumulated back surface: $\Phi_{s2} \approx 0$V. To find the V_{th} at front surface: $\Phi_{s2} = 0$V, $Q_{inv1} = 0$, $\Phi_{s1} = 2\Phi_F \rightarrow$

$$V_{th1,acc2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox1}}\right)2\Phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (7)$$

all of which are presumed known.

For inverted back surface: $\Phi_{s2} \approx 2\Phi_F$, $Qinv1 = 0$, $\Phi_{s1} = 2\Phi_F$, resulting in

$$V_{th1,inv2} = \Phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\Phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (8)$$

Not particulary useful: device always on!

For back surface deplated, front Φ_{s1} depends on V_{G2}