Introduction to SOI

The first proposed FET device was actually SOI type!

SOI is most important for CMOS applications which are currently dominated by bulk Si technology.

What's the problem? Mainly parasitics and scaling of the dimensions. First see fig for device/technology description.

Interactions with substrate: drain and source capacitance. These increase with increase in doping, which is increased as device dimensions are scaled down. These also include capacitance with channel-stop implant (needed to prevent the channel formation underneath the field oxide)

Latchup: parasitic thyristor structure (pnpn) can be turned on if the internal gain becomes larger than one. Treatable, but increases the complexity and cost.

For ideal SOI see fig. Dielectric isolation prevents most of the parasitic effects. For latchup, the substrate path is taken out and also the parasitic BJTs have low current gains (why and which ones?). (BTW, latchup does not occur under normal operating conditions: node voltage overshoots, displacement current, avalanching or photocurrents are needed to trigger it)

In bulk CMOS: isolation via p-n junctions (or trenches, or field oxide, or... see fig) In bulk n-channel drain is positively biased $[0, +V_{DD}]$ $\rightarrow$ depletion capacitance (with max at 0V). This cap. depends on doping and since scaling demands increased substrate doping it increases. Add to this channel stop implant capacitance.

For SOI: max capacitance between junctions and substrate is cap. of the insulating layer. SiO_2 dielectric constant is smaller than in Si $\rightarrow$ cap. reduction by 3x! Thickness of the insulating layer does not have to be scaled either.

Some manufacturing advantages: realization of shallow junctions and contact much easier. Simply put, the junction thickness is equal to the substrate thickness of Si in SOI, while in bulk special techniques are needed. Furthermore, contacts are easier to form (see fig.) For most SOI technologies, S/D will reach insulating substrate, preventing “punchthrough.”

Additional advantages: radiation hardness, improved transconductance, better (lower) subthreshold slope etc. (caution needed, however!)

SOI Techniques and Materials

A quick overview of various techniques used with special emphasis on SIMOX.

Homo- and hetero-epitaxial techniques. The latter involve different materials for substrates, the best one so far is sapphire. Problem: defect growth is basically out of the question! Not only because of the lattice mismatch, but also due to different thermal expansion coefficients (see table). Thermally generated stresses result in formation of defects.

Despite this, SOS is capable of LSI-VLSI type integration. The main advantage is radiation hardness. Due to defects mobility and lifetime are reduced. (el. mobility is also affected by compressive stress - repopulation and increase of eff. mass; holes have reduced mass). Lifetimes are $\sim$ 1ns, resulting in high leakage currents. With further refinements in technology, mobility can be brought to be closer to the bulk values.

Manufacturing issue: heteroepi techniques are not compatible with standard Si processing facilities (those materials can be viewed as contaminants). Also, SOS substrate are brittle and transparent making characterization difficult.

Alternative: poly-Si recrystalization. Laser, E-beam, zone-melting (ZMR) (show figs). Ideally we'd like to see (100) surface everywhere — not easily done; requires seeding.

Homoepitaxial Techniques

Idea: crystal growth extends laterally over SiO_2 layer (see fig.). The best known: epitaxial lateral overgrowth (ELO). Growth both laterally and vertically - main disadvantage necessitating additional polishing etc. Variations on the theme exist.

(Whatever happened to FIPOS?)

SIMOX is the most important and widely used technology. (Separation by IMplanted OXygen). For a short history and a basic idea see fig.

Simple idea: implant oxygen into Si to form SiO_2 layer! Problem: we need to implant two oxygen atoms for every Si atom — much, much larger quantity than in doping implantation ($10^{18} cm^{-2} vs. 10^{16} cm^{-2}$). Early problems were overcome with availability of a new implanter and by increasing the anneal temperatures to near melting point of Si ($1405°$C). Now atomically sharp interfaces are possible.

Oxygen dose: problem if low doses are used - formation of oxide precipitates instead of continuous oxide layer. For this we need cca $1.8 \cdot 10^{18} cm^{-2}$. This results in 400 nm thick oxide layer after annealing. (fig for variations) SiO_2 occupies larger volume than Si resulting in swelling. Remember that Si layer above implanted oxygen is amorphous.

Implantation temperature is also important parameter. For too low T, annealing results in poly-Si, but for T$> 500°$C self-annealing occurs, i.e. crystallinity of the top Si layer is maintained even though the layer is very defective. For T$> 700°$C oxide precipitates form.

Annealing absolutely crucial for device quality material (see fig). Standard procedure calls for 6 hour annealing at $1300°$C in argon on nitrogen atmosphere. This takes out the oxygen precipitates and makes very sharp interface. It does not take care of dislocations, however.

Dislocations seem related to contamination (carbon) introduced during implantation. It was observed that their density falls off dramatically for doses below $4 \cdot 10^{17} cm^{-2}$. Problem: this does is subcritical. Solution: multiple implant/anneal cycles such that the cumulative dose exceeds the critical one. Dislocation densities fall down to $10^{3} cm^{-2}$ while preserving sharpness.

Trend: low-dose, low-energy implants. Three reasons: hardness of buried oxide (?), direct fabrication of thin Si films (for e.g. fully depleted devices), cost proportional to energy and dose. The results: 57 nm thick Si layers on 47 nm layer oxide layer.

For dislocations over the years, see fig. Finally, metal contamination can present a problem. They come from various metal parts used in implanter. Can be controlled, down to $10^{17} cm^{-3}$, with 10^{15} expected (?). (see fig)

One final technique: wafer bonding and etch-back. Basic idea is to "glue" or "bond" two wafers via their oxidized surfaces. One of the surfaces is then thinned down to SOI requirement. Bonding is not trivial, but it is much easier than oxygen implantation. Voids are the main problem.

Once the bonded wafer has been created, use grinding/polishing/ etching to get the thickness right. Better: initial grinding and then etch-back with etch-stops. Etch stop is obtained by using different dopants and etchants that are very selective with respect to dopant concentration.

In one of the wafers implant p^{++}, grow low-doped epi, grow or deposit oxide, then bond. After that, etch to p^{++}, stop, etch p^{++}, and you have SOI wafer. Better than 12 nm thickness uniformity is possible. Excellent crystal quality, comparable to the starting wafers. Defect density increases but is still $< 10^3 cm^{-2}$. Excellent lifetimes.

For comparison of various wafer technologies, see fig. Generalizing: radiation hardness and VLSI CMOS apps $\longrightarrow$ use SIMOX, possibly ZMR and wafer bonding; power and bipolar apps $\longrightarrow$ use wafer bonding, maybe ZMR; 3-D integration $\longrightarrow$?? laser, e-beam recrystalization

SOI Characterization

Crystal defects: TEM is powerful, but limited by small observation area and long preparation. Destructive.

Grain boundaries: typically occur in re-crystallized material. Definitely bad if they happen to be between S and D (enhanced diffusion of dopants and associated increase in leakage current (fig)). For perpendicular boundary, interface traps result in increased threshold voltage, as well as reduce mobility.

Oxygen contamination (SIMOX): some oxygen is still present in Si film and can result in modifications in film resistance. Four point probe measurement used.

Carrier lifetime: τ_g can be extracted from leakage current measurements, by measuring capacitance and current. Current = diffusion current, bulk generation current, surface gen. current, and other currents (field-enhanced generation current). V_r applied such that depletion layer does not reach buried oxide. It uses dependance of depl. layer width on applied voltage.

Capacitance measurements: classic method can be used, but interpretation is difficult. Contribution from accumulation, depletion and inversion states and both front and back interfaces and also from Si substrate. Best solution: simulation and comparison. Also, direct measurements on special C structures (fig).

Charge pumping: efficient for characterization of Si/ SiO_2 interfaces and it yields the distribution of interface states in the band gap. For SOI, front and back interf. are characterized separately. S and D are connected (fig) and slightly reverse biased with respect to substrate. A periodic triangular signal is applied with frequency f. Amplitude is large enough to switch the surface from accumulation to strong inversion. Acc. $\rightarrow$ inv., minority carriers are provided by S and D, and some are trapped. For inverse process, minority carriers exit quickly, but not the ones that are trapped. Those recombine with holes and this current is the so called charge-pumping current. By measuring this current average interface trap density can be obtained.

For SOI similar technique is used, but on gated pin diode. (figs)