Microwave Semiconductors

First division: active, and b) passive. Active devices used in amplifiers and oscillators and passive in mixers.

Microwave Circuit Design II

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MESFETs

Fermi level must line up in equilibrium (for reverse bias), and is the vacuum level must be continuous (see diagrams).

\[ \frac{M}{(\Lambda - \frac{\eta \Lambda}{2})} = \frac{u}{Z} \]

where \( \Lambda \) is applied voltage (for forward bias, for reverse bias), and \( Z \) is the maximum field in the depletion layer.

Electric field and space charge are zero outside the depletion layer.

Standard approximation: abrupt junction, which means that the band edge is the Fermi level between Fermi level and conduction band.

Analysis is similar to p-n junction and we need to determine the barrier height:

\[ (\Lambda - \frac{\eta \Lambda}{2}) \frac{dN b}{\varepsilon Z} = M \]

Measured barrier heights are different from the above equation. Reasons: surface states in the forbidden bandgap.

Barrier height (\( \chi \)) in n-type semiconductor (see diagrams).

\[ (\chi - u) b = \frac{d}{E} b \]

Fermi levels must line up in equilibrium. In addition, vacuum level must be continuous.
Another important characteristic of Schottky diode is its capacitance, which is defined as change of charge per change of voltage:

\[
\frac{dQ}{dv} = \frac{\Delta Q}{(A - \eta A)^2} = \frac{\Delta Q}{1}
\]

This can be further rewritten as:

\[
\frac{\Delta Q}{\Delta v} = \frac{M}{s} = \frac{(A - \eta A)^2}{\frac{dN^{s\phi b}}{C}} = \frac{\Lambda \theta}{s} = \theta
\]

The measurement of the capacitance \( C \) per unit area as a function of voltage provides:

\[
\begin{align*}
\frac{dN^{s\phi b}}{\Delta v} &= \frac{\Delta Q}{(A - \eta A)^2} = \frac{\Delta Q}{\Delta v} \\
\end{align*}
\]
\[ \left( \frac{J_m}{(A \Phi - uB \phi) B} \right) dx \eta \alpha N = (s) u \]

In equilibrium to the above equation for \( u \), change relative to equilibrium. On the other hand, \( J_m \) change quite dramatically. From the metal, the barrier does not change which implies that \( J_m \) does not cancel. However, the barrier for electron flow is very different, depending on whether the electron is coming from metal or from semiconductor. If the electron is reduced (increased); however, the barrier for electron flow is very different, depending on whether the electron is coming from metal or from semiconductor. If the electron is coming from metal, the barrier does not change which implies that \( J_m \) does not cancel each other. On the other hand, \( J_m \) change quite dramatically.

When forward (reverse) bias is applied, the potential difference between two sides is

\[ \left( \frac{J_m}{uB \phi B} \right) dx \eta \alpha N = \left| \frac{u \alpha \eta}{\alpha \eta} \right| = \left| \frac{s \alpha \eta}{\alpha \eta} \right| \]

where \( C \) is a proportionality constant.

Outside of equilibrium, we must have some dependence of \( n_s \) on applied voltage. Not surprisingly, this dependence is again exponential.

When forward (reverse) bias is applied, the potential difference between two sides is

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and can, therefore, write:

\[ \frac{uB \phi B}{dx \eta \alpha N} = \frac{dA}{dx \eta \alpha N} \]

At the surface of Schottky and conduction band edge, \( \eta \alpha N \) and exponentially dependent on difference between Fermi level the density of states and exponentially dependent on difference between Fermi level to the semiconductor surface \( u \). Remember that electron concentration is proportional to the semiconductor surface concentration. Both of these components are proportional to the electron concentration at

\[ \left( \frac{u \alpha \eta}{\alpha \eta} \right) \alpha \eta \alpha N = \left| \frac{s \alpha \eta}{\alpha \eta} \right| \]

in equilibrium to the above equation for \( u \).
The net current across the junction is

$$J = J_{s \rightarrow m} - J_{m \rightarrow s} = C_1 N_C \exp \left( -\frac{q\phi_{Bn}}{kT} \right) \left[ \exp \left( \frac{qV_F}{kT} \right) - 1 \right]$$  \hspace{1cm} (8)$$

For reverse bias, $V_F$ is replaced by $-V_R$. Furthermore, the coefficient $C_1 N_C$ is equal to $A^* T^2$, where $A^*$ is called the effective Richardson constant and $T$ is temperature. The constant terms can be collected in one constant resulting in

$$J = J_s \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right] \quad \text{and} \quad J_s \equiv A^* T^2 \exp \left( -\frac{q\phi_{Bn}}{kT} \right)$$  \hspace{1cm} (9)$$

In Schottky diodes there is a hole current which is due to hole injection from the metal to the semiconductor. This injection is the same as in $p^+ - n$ junction. In normal operation conditions it is much smaller than the electron component (why?) resulting in a unipolar operation.

Ideal ohmic contact should conduct in either direction and should not have any voltage drop across the metal-semiconductor interface. This is only approximately true in real ohmic contacts. Two techniques are used: 1. utilizing a metal with low barrier height ($\phi_{Bn}$), and 2. high doping. The conduction can be dominated by either thermionic emission or tunneling.
MESFETs

The JFET

Why bother with JFET? It is good introduction to MESFETs which are much more common and the principle of operation is very similar.

**Case a:** Keep $V_G$ and $V_D$ small. Then $I_D$ is very small. Voltage applied at the control gate, $V_G$, shrinks or opens up the channel for electron flow. The wider the channel, the smaller the resistance and vice versa. The output electrode shrinks or opens up the channel for electron flow through it. The output electrode is basically a resistor that has a control gate. Voltage applied at the control gate changes the output voltage, $V_D$, which is the drain voltage.

Under normal operating conditions, the channel in the equilibrium:

$$I_D = \frac{(M - p)ZA}{dN^{n+1}b} = \frac{V}{T} = \frac{V_d}{\tau}$$

Where $n$ is donor concentration, $A$ is the cross-sectional area for current flow, $N^+ = N_D$, $M = \frac{W}{2d}$, $Z$ is depletion layer width of upper and lower p-n-junctions, $p$ is p-channel device, and $V_G$ is control gate voltage.

$V_G = 0$ and $V_D = 0$, $I_D$ is very small. Then $I_D = V_D/R$. Output current varies $dI_D/dV_D = 1/R$. Then $I_D$ is very small.

$V_G = 0$ and $V_D$ small, $I_D$ small. Then $I_D$ is very small. Voltage applied at the control gate, $V_G$, shrinks or opens up the channel for electron flow. The wider the channel, the smaller the resistance and vice versa. The output electrode shrinks or opens up the channel for electron flow through it. The wider the channel, the smaller the resistance and vice versa.

**The JFET**
Case b/#29./: 

\[ V_{G} \] is allowed to change up to "pinch-off". The following must be taken into account: the voltage difference between drain and source must occur along the channel. This results in variable resistance \( R \), and we can expect that the rate of change of current should decrease as drain voltage is increased, i.e. \( R \) increases with \( V_{D} \).

Therefore Case b) results in variable resistance \( R \), and we can expect that the rate of change of current should decrease as drain voltage is increased, i.e. \( R \) increases with \( V_{D} \).

Case c): the two depletion regions touch at the drain side. This is called pinch-off, and the device enters the saturation region. Voltage at which this happens is called saturation voltage \( V_{D,sat} \) and is calculated from:

\[
0 = \frac{q}{e} \Lambda - \frac{qE_{\infty}}{eD_{N}b} = \frac{qE_{\infty}}{eD_{N}b}
\]

The voltage difference between channel and gate is going to vary near the drain contact. Since we now allow \( V_{D} \) to increase \( \Lambda_{D} \) to increase will, the potential near the source contact. This results in higher potential near the drain contact and lower potential near the channel. This is called pinch-off. The following must be taken into account: the voltage difference between drain and source must occur along the channel. This results in variable resistance \( R \), and we can expect that the rate of change of current should decrease as drain voltage is increased, i.e. \( R \) increases with \( V_{D} \).

Case b): \( V_{G} \approx 0, V_{D} \approx \frac{q}{e} \Lambda_{D} \) is allowed to change up to "pinch-off".
Gate voltage.

Gate voltage is used to mean the magnitude of the applied voltage, but from now on, when $V_G$ is used it means the magnitude of the applied voltage from source to gate in the channel device. Important: Gate voltage is actually negative with respect to the source in n-channel devices. Therefore, saturation voltage decreases with increase in magnitude of $V_D$ for reverse bias, saturation voltage decreases with increase in magnitude of $V_A$ for depletion of $V_D$. The value of $I_D$ must be subtracted.

If the gate is reverse biased, that only makes the starting resistance $R$ larger, but the same reasoning as above applies. To obtain $I_D$, the starting value of $I_D$ must be subtracted.

At pinch-off, a large drain current flows, called saturation current $I_D$ and drain and source are completely (almost) isolated from each other by a depletion region. This is similar to the situation in BJT, where electrons, after traversing the base region, are isolated from each other by a depletion region. This is similar to the situation in BJT. 

Beyond the pinch-off, increase in $I_D$ cannot increase anymore. The potential drop is from point $P$ to source is still the same and the resistance length is still long channel approximation. Therefore, the current is still going to be $I_D$.

Important: Gate voltage is actually negative with respect to the source, but from now on, when $V_G$ is used it means the magnitude of the applied voltage.
(15) \[ MPM \frac{s_{\varepsilon}}{d_N b} = \Lambda P \]

above, take total differential of both sides

3. Variations of voltage and depletion layer width are related through (take square of

(14) \[ \frac{d_N b}{[\Lambda + \varepsilon \Lambda + (\Lambda) \Lambda] s_{\varepsilon}} = (\Lambda) M \]

2. For abrupt junction the depletion layer width is

\[ \Lambda P [\Lambda] M - v] Z d_N u_{hf} h = \hbar p d_I \]

(13) \[ \frac{(\Lambda) M - v] Z d_N u_{hf} h}{\hbar p d_I} = \Lambda P \]

1. Find the voltage drop across a small cross-section of the channel

\[ \text{Deviation of } I \text{ vs. } V \text{ follows as follows: } \]

I-V Characteristics
where

\[ I_D = \frac{1}{2} L Z W_2 W_1 \frac{q}{n_N D} \]

\[ V_P = \frac{q N D}{2} \]

\[ V_P \] is called pinch-off voltage, i.e., it is the voltage across the junction at the drain end when \( W_2 = a \). This results in

Two distinct regions: (a) Linear region, and (b) Saturation region.

Linear region:

Assumption is \( \eta \Lambda + \zeta \Lambda \gg \Lambda \) and the full equation can be approximated by

\[ \left( \frac{d \Lambda}{\eta \Lambda + \zeta \Lambda} \right) - 1 \right] \frac{d \Lambda}{d I} \approx d I \]

Implied by

\[ I_{D}' = I_P \left( \frac{V_G + V_{bi}}{V_P} \right)^{2/3} \]

 substituted for current and integrate or, think of it as summation.

\[ \int_{0}^{L} \left( \frac{d \Lambda}{\eta \Lambda + \zeta \Lambda} \right) \frac{\zeta}{\zeta} + \frac{d \Lambda}{\eta \Lambda + \zeta \Lambda + \zeta \Lambda} \frac{\zeta}{\zeta} - \frac{d \Lambda}{d \Lambda} \right] d I = \]

\[ \int_{0}^{L} \left( \frac{d \Lambda}{\eta \Lambda + \zeta \Lambda} \right) \frac{\zeta}{\zeta} + \frac{d \Lambda}{\eta \Lambda + \zeta \Lambda + \zeta \Lambda} \frac{\zeta}{\zeta} - \frac{d \Lambda}{d \Lambda} \right] d I = \]

\[ M \bar{a} \bar{b} \bar{N} \int_{0}^{L} (\bar{M} - \bar{v}) Z \bar{a} \bar{b} \bar{N} \bar{b} \bar{c} \bar{e} \bar{f} \bar{g} \bar{h} \bar{i} \bar{j} = \]

4. Substitute \( d \Lambda \) into eq. for current and integrate (or, think of it as summation).
Another important parameter is transconductance \( \frac{d\Lambda}{dI} \) with \( \frac{\partial L}{\partial I} \) constant.

(91)

\[
\left[ \frac{d\Lambda}{\eta\Lambda + C\Lambda} \right] - I \frac{d\Lambda}{dI} = w_b
\]

Saturation region: evaluated drain current at pinch-off point — it stays constant for any above saturation voltage \( d\Lambda = \eta_s d\Lambda \) for any above saturation voltage.

What is the value of beyond pinch-off?

(92)

\[
\left[ \frac{d\Lambda}{\eta\Lambda + C\Lambda} \right] - I \frac{d\Lambda}{dI} = d\Lambda
\]

Another interesting parameter: output (channel) conductance, defined as with \( \frac{\partial L}{\partial I} \).
First we have to find out a.c. currents and voltages based on our knowledge of d.c.

\[
\begin{align*}
\frac{d\tilde{v}_G}{d\tilde{i}} &= g_{m} + \frac{g_D}{2} \\
\frac{d\tilde{v}_{DS}}{d\tilde{i}} &= \frac{2}{3} g_{m} + \frac{g_D}{3} \\
\end{align*}
\]
Checkout the equivalent circuits: idealized and more realistic (low/high frequency).

Unity current gain frequency ($f_T$) — name describes it all. It is, quite generally,

\[ f_T = \frac{\mu C_{in}}{2} \]

Expressed as:

\[ f_{max} \]

For power amplification we will use model, we can easily see that $C_{GS} + C_{GD} = C_{in}$. Total input capacitance as seen by signal at gate contact. In our simplified model, we can easily see that $C_{in}$ is total input capacitance as seen by signal at gate contact. In our simplified model, we can easily see that $C_{in}$ is total input capacitance as seen by signal at gate contact. In our simplified model, we can easily see that $C_{in}$ is total input capacitance as seen by signal at gate contact. In our simplified model, we can easily see that $C_{in}$ is total input capacitance as seen by signal at gate contact.
Further components: output conductance and capacitance.

\[ \frac{1}{g_m} = \frac{s \frac{\partial \Delta V_{gs}}{\partial \Delta V_{ds}}}{s \frac{\partial \Delta I}{\partial \Delta V_{ds}}} = \frac{s \frac{\partial \Delta V_{gs}}{\partial \Delta V_{ds}}}{s \frac{\partial \Delta I}{\partial \Delta V_{gs}}} = \frac{1}{g_{m_{intrinsic}}}. \]

Intrinsic components: \( g_{m_{intrinsic}} = \) intrinsic transconductance.

\[ \frac{s \frac{\partial \Delta V_{gs}}{\partial \Delta V_{ds}}}{s \frac{\partial \Delta I}{\partial \Delta V_{ds}}} \quad \text{and} \quad \frac{s \frac{\partial \Delta V_{gs}}{\partial \Delta V_{gs}}}{s \frac{\partial \Delta I}{\partial \Delta V_{gs}}} = \frac{1}{g_{m_{intrinsic}}}. \]

Capacitor components: \( C_{DG} \) contains both intrinsic and parasitic components: intrinsic for the part that is across depletion layer, parasitic that is not.

See Circuit 9 for simple example circuit. In addition to intrinsics, some parasitic elements: \( C_{gs} \) gate-source capacitance; \( R_s \) source resistance; \( g_{m} \) measure of leakage current on the gate; \( R_g \) gate resistance.
As for JFETs, pinch-off voltage \( V_{P} \) is given by 
\[
V_{P} = \frac{qD}{a} \approx \frac{V_{T}}{2}
\]
which is the voltage needed to deplete the channel of thickness \( a \).

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The max gate voltage for both cases is limited by forward biasing the gate.

Saturation region in Fig. Saturation current for \( V_{DS} \) is called \( I_{DS} \).

Different model for small devices, based on velocity saturation (Fig.)

\[
\begin{align*}
(29) & \quad \frac{S_\varphi \Lambda - \eta \Lambda}{s e d N \bar{b}} Z^s \dot{a} = \frac{S_\varphi \Lambda - \eta \Lambda}{d \Lambda} Z^s \dot{e} \dot{a} = \eta m \ddot{b} \\
(30) & \quad \left( \frac{d \Lambda}{S_\varphi \Lambda - \eta \Lambda} - 1 \right) d N Z^s \dot{a} \dot{b} = (\eta - \nu) d N Z^s \dot{a} \dot{b} = S d I
\end{align*}
\]

which gives expressions for transconductance.

They also, depletion formation.

Diagnostic Circuit Design II

Microwave Circuit Design II