CS577 Modern Language Processors
Spring 2018
Lecture Interpreters
VM programs have an explicitly specified binary representation, typically called **bytecode**.

Most VM’s can execute bytecode directly by **interpretation**.

Interpretation is typically 1-2 orders of magnitude slower than compilation (but of course this depends on interpreter, compiler, target machine)

So serious VM’s usually do JIT compilation too

Still, it is worthwhile to make interpreters **efficient**

But it is also desirable to keep them **portable**
TARGET HARDWARE: FACTS OF LIFE

Accessing memory is slow!

- Even a L1 cache hit typically costs several cycles.
- Cache misses cost 10’s-100’s of cycles.
- Must try to keep data in registers if possible.
- Small changes in data, code layout can have big effects

Machines are deeply pipelined!

- Conditional branches are bad.
- Dynamic-target branches are probably worse.
- Should try to utilize hardware support tricks (e.g. branch target buffers).
- Recent machines (last 5 years) may have significantly improved branch prediction.
Interpreting an instruction requires:

- Dispatching the instruction: getting control to the code corresponding to the instruction
- Accessing the operands: getting the values of the parameters and arguments (and storing the result)
- Actually performing the computation. (Note: the longer this takes, the smaller the percentage overhead of interpretation!)
u4 stack[STACKSIZE];

void interp (Method *method) {
  u1 *pc = method->code;
  while (1) {
    switch (*pc) {
    case ICONST_0:
      { *(++sp) = (u4) 0;
        pc++;
        break; }
    case ISTORE_0:
      { locals[0] = *(sp--);
        pc++;
        break; }
    case IADD:
      { int32 v2 = (int32) (*(sp--));
        int32 v1 = (int32) (*sp);
        *sp = (u4) (v1 + v2);
        pc++;
        break; }
    ...
    }
  }
}
First, let’s consider just the cost of accessing stack elements:
loads/stores to memory and \(sp\) adjustment.

C code:

```c
    case ICONST_0: { *(++sp) = (u4) 0; pc++; break; }
```

X86 (32-bit) machine code (obtained using gcc -S)

```assembly
    // initially -64(%%ebp) = pc
    movl _sp, %eax          // load value of sp from C global
    leal 4(%eax), %ebx     // new sp
    movl %ebx, _sp          // save new sp value into C global
    movl $0, 4(%eax)        // *(new sp) = 0
    incl -64(%%ebp)         // pc++
    jmp top                 // break
```
RISCV-32 machine code (obtained using gcc -S)

```assembly
// initially s11 has %hi(sp) s9 has pc
lw a5,%lo(sp)(s11)  // load value of sp from C global
addi s9,s9,1        // pc++
addi a2,a5,4         // new sp
sw a2,%lo(sp)(s11)   // store new sp into C global
sw zero,4(a5)        // *(new sp) = 0
j top
```

RISCV features:
- load/store architecture
- about 30 registers
Utilizing Registers

Keeping $sp$ in a global memory location looks like a terrible idea, since it requires one load and one store per bytecode executed.

Let’s make it a local of $interp$ instead. Then C compiler should be able to keep it in a register (if there are any available).

New RISCV machine code:

```
// initially s9 = pc, s11 = sp
sw zero,4(s11) // *(new sp) = 0
addi s9,s9,1   // pc++
addi s11,s11,4 // new sp = sp + 4
j top          // break
```
New X86-32 machine code:

```plaintext
// initially -28(%ebp) = sp   -64(%ebp) = pc
addl  $4, -28(%ebp)         // ++sp
movl  -28(%ebp), %ecx      // load value of sp
movl  $0, (%ecx)           // *sp = 0;
incl -64(%ebp)             // pc++
jmp   top                   
```

Now sp lives in the local stack frame rather than in a global, but there still isn’t a free register for it.
C code:

```c
    case IADD: { int32 v2 = (int32) (*(sp--));
                  int32 v1 = (int32) (*sp);
                  *sp = (u4) (v1 + v2);
                  pc++; break; }
```

RISCV code:

```riscv
    // initially s11 = sp    s9 = pc
    lw      a5,-4(s11)    // ld *(sp-1)
    lw      a2,0(s11)    // ld *sp
    addi    s11,s11,-4    // sp--
    addi    s9,s9,1      // pc++
    add      a5,a5,a2     // add
    sw      a5,0(s11)    // store to *(new sp)
    j       top          // break
```

Next obvious problem is that nearly every instruction loads and/or stores stack entries.
Idea: what if we **cache** the top-of-stack in a local variable $s0$?

(Assume that $sp$ points to the top of the *remainder* of the stack.)

This saves one load and one store for IADD:

```c
    case IADD: {int32 v2 = (int32) s0; int32 v1 = (int32) (*(sp--));
                 s0 = (u4) (v1+v2); pc++; break; }
```

Approximate RISCV code:

```c
    // initially s11 = sp   s9 = pc   x9 = slot0
    lw      a2,0(s11)   // ld *sp
    addi    s11,s11,-4  // sp--
    addi    s9,s9,1   // pc++
    add      x9,x9,a2  // slot0 += a2
    j        top       // break
```
CACHING ONE SLOT

But it is a wash for the other two instructions because we have to keep \( s_0 \) up-to-date.

```c
    case ICONST_0: { *(++sp) = s0; s0 = (u4) 0; pc++; break; }
```

Approximate RISCV code (still one store)

```c
    // initially s11 = sp  s9 = pc  x9 = slot0
    sw      x9,4(s11)  // *(new sp) = slot0
    addi    s9,s9,1    // pc++
    addi    s11,s11,4   // new sp = sp + 4
    mv      x9,zero    // slot0 = 0
    j       top        // break
```
case ISTORE_0: { locals[0] = s0; s0 = *(sp--); pc++; break; }

Approximate RISCV code (still one load and one store)

// initially s11 = sp s9 = pc x8 = base of locals x9 = slot0
sw  x9,0(x8)  // locals[0] = slot0
addi s9,s9,1  // pc++
lw  x9,0(s11)  // slot0 = *sp
addi s11,s11,-4  // sp--
j    top        // break
What if we keep two elements in local variables (registers) named $s_1$ (top of stack) and $s_0$ (next-to-top of stack)?

```java
  case ISTORE_0: { locals[0] = s1; s1 = s0; s0 = *(sp--); pc++; break; }

  case ICONST_0: { *(++sp) = s0; s0 = s1; s1 = (u4) 0; pc++; break; }

  case IADD: { int32 v2 = (int32) s1; int32 v1 = (int32) s0;
               s1 = (u4) (v1+v2); s0 = *(sp--); pc++; break; }
```

This just pushes off the problem: no improvement in number of loads and stores needed.

New idea: let’s keep a different number of cached stack slots at different points during execution.
GENERALIZED STACK CACHING

- Interpreter operates in one several different states corresponding to how many stack slots are cached.
- Each instruction (potentially) causes transition to a different state, according to what it does to the stack.
- For example:

  ICONST_0 moves to a state where more slots are cached;
  ISTORE_0 moves to one where fewer slots are cached.
  IADD moves to a state where one slot is cached.
GENERALIZED STACK CACHING (2)

For JVM, 3 states are sufficient to handle all instruction types.
State 0: no slots cached.
State 1: top of stack is cached in variable \(s_0\).
State 2: top of stack is cached in variable \(s_1\); next-to-top in \(s_0\).
In all states, \(sp\) points to remainder of stack beyond cached slots.
Sample code follows (in practice we may organize it differently)...
case IADD: {
    switch (state) {
    case 0: { int32 v2 = (int32) (*(sp--)); int32 v1 = (int32) (*(sp--));
            s0 = (u4) (v1+v2); state = 1; break; }
    case 1: { int32 v2 = (int32) s0; int32 v1 = (int32) (*(sp--));
              s0 = (u4) (v1+v2); state = 1; break; }
    case 2: { int32 v2 = (int32) s1; int32 v1 = (int32) s0;
              s0 = (u4) (v1+v2); state = 1; break; }
    pc++; break; }

    case ICONST_0: {
    switch (state) {
    case 0: s0 = 0; state = 1; break;
    case 1: s1 = 0; state = 2; break;
    case 2: *(++sp) = s0; s0 = s1; s1 = 0; state = 2; break; }
    pc++; break; }

    case ISTORE_0: {
    switch (state) {
    case 0: locals[0] = *(sp--); state = 0; break;
    case 1: locals[0] = s0; state = 0; break;
    case 2: locals[0] = s1; state = 1; break; }
    pc++; break; }

Consider a typical expression like

\[ b = a + 3 \]

where we assume \( a \) is local variable 0 and \( b \) is local variable 1.

(Assume we start with state = 0.)

<table>
<thead>
<tr>
<th>Bytecode</th>
<th>Corresponding executed code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILOAD_0</td>
<td><code>s0 = locals[0]; state = 1;</code></td>
</tr>
<tr>
<td>ICONST_3</td>
<td><code>s1 = 3; state = 2;</code></td>
</tr>
<tr>
<td>IADD</td>
<td><code>s0 = s1 + s0; state = 1;</code></td>
</tr>
<tr>
<td>ISTORE_1</td>
<td><code>locals[1] = s0; state = 0;</code></td>
</tr>
</tbody>
</table>

We do only the essential loads and stores – no stack traffic at all!
More generally, instructions are classified by a pair:
(# of stack slots they consume, # of stack slots they produce)

For example:

ISTORE_0    1,0
ICONST_0    0,1
IADD        2,1
So far we’ve described **dynamic** stack caching, where the interpreter keeps track of its current state.

- In practice, we implement this by having three complete sets of instruction implementations and dispatching to the correct one based on current state as well as opcode (more on this later).

- But it may seem like we should be able to predict the state at each program point **statically** (before execution). If so, we could simply have three variants of each opcode, and select the right one at compile time. This would be more efficient.

- Only problem: at **join points** in the code, the state may differ depending on the path by which the join point was reached. Must choose a convention for which state to use there, and add **compensation code** to the other branches; this is complex in practice.
Aside: Why use stack-based VM’s?

Nearly all hardware processors use **registers**

- Each HW instruction is parameterized by its argument/result registers.
- Why is this good for hardware? Because the opcode and the argument registers can be decoded in **parallel**, and values can quickly be fetched from a small, fast register file.

Why not try this in software machines too?

- Parameters must be fetched from the byte stream and decoded **serially**; for stack instructions, parameters are implicit.
- Instructions with parameters take more space.
- Software registers cannot easily be stored in hardware registers, because the latter can’t be indexed. So software registers end up living in an in-memory array (just like stack slots).
- On the other hand, register architectures require fewer instructions; hence less **dispatch**. So maybe a worthwhile idea after all...
What does RISCV code look like now?

```assembly
// s10 = table  s9 = pc
    top: lbu      a1,0(s9)     // *pc
        li       a5,184
        bgtu     a1,a5,undefined // if > 184 or < 0, branch to "undefined"
        slli     a5,a1,2        // scale *4
        add      a5,s10,a5      // add base of table
        lw       a5,0(a5)       // get snippet address
        jr        a5            // jump to snippet

    table:
        .word nop_snippet
        .word aconst_null_snippet
        .word iconst_m1_snippet
        .word iconst_0_snippet
        ...
        .word goto_w_snippet

    undefined:
        ...issue error and die...
```
Obvious performance problems:

- Unnecessary bounds check.
- Two jumps per dispatch (counting the one back to top at the end of the previous instruction).

First fix: **(Indirect) Threaded Code**

If we can code our own indirect jumps, could

- Remove bounds check.
- Replicate dispatch at end of every snippet, thus removing one jump.
- This is not possible in ANSI Standard C, but can do in gcc using the && operator.
interp(Method method) {
    static void *dispatch_table[] =
    {&NOP,
     &ACONST_NULL,
     &ICONST_M1,
     ..., 
     &JSR_W};
    u1 *pc = method->code;
    ...
    goto *(dispatch_table[*pc]);

    NOP:
    pc++;
    goto *(dispatch_table[*pc]);

    ACONST_NULL:
    *(++sp) = (u4) 0;
    pc++;
    goto *(dispatch_table[*pc]);
    ...
}
One extra reason why indirect threaded code improves performance may be that it makes better use of hardware support for branch predication.

Many pipelined processors contain a branch target buffer (BTB) that dynamically remembers the last target for each branch instruction (including conditional and indirect branches). The next time the branch instruction is executed, the processor pre-fetches from the address predicted by the buffer.

- A naive interpreter makes terrible use of this feature, because a single instruction dispatches to all the snippets, so prediction accuracy is \( \approx 0 \).
- The indirect threaded code version does somewhat better, because the dispatches are distributed, and certain bytecode instruction sequences are quite common, so prediction accuracy may be \( > 0 \).

But a fundamental prediction mismatch between the VM and the target hardware remains.
Each instruction dispatch still requires two fetches: one to get the byte code and a second to get the snippet address.

New idea: what if we represent each instruction opcode by the address of its snippet?

```c
interp() {
    char *codeaddrs[] = ...; /* fill this with snippet addrs */
    char *pc = codeaddrs;    /* initialize to start */
    goto **pc;

    ACONST_NULL:
        *(++sp) = (u4) 0;
        pc++;
        goto **pc;
    ...
```

Now need only one fetch per instruction!
But notice that we’re no longer interpreting the original bytecode any more.

Must rewrite before execution

Simple in principle, but there are details. e.g.

- What should we do with the parameter bytes following the opcode?

If we’re going to rewrite the bytecode, there are many opportunities to improve things, e.g.

- Combine code for similar opcodes (e.g. constant loading).
- Short-circuit constant pool references (important in full language)
- Perform static stack caching
- Etc, etc.

A more radical rewrite idea: dispatch to each snippet using a subroutine call instruction. May pay off on processors that pre-fetch from the return address on the hardware stack!
Another way to reduce dispatch time is to do fewer dispatches.

One basic approach is to combine sequences of instructions that occur frequently into into “macro” or “super”-instructions.

For example, the following sequence pattern is very common:

\[
\text{ILOAD } n \\
\text{ICONST } i \\
\text{IADD} \\
\text{ISTORE } n
\]

In fact, the JVM designers already invented a combined instruction for this (IINC) but the same idea works for other sequences.

Another approach is to use a register architecture, which typically requires many fewer instructions (although each instruction gets more parameters).
This can be done in several ways:

- Statically, for multiple programs:
  - Essentially a refinement of the VM definition, possibly tuned to workload from a particular set of programs.
  - Can construct such specialized VM’s semi-automatically from a generic VM.
  - Specialized VM can be compiled with “cross-snippet” optimization.

- Statically, for a single program
  - Encoding is sent with the program.
  - Static encodings also have the benefit of reducing the program size, allowing quicker transmission.

- Dynamically, by building superinstructions “on the fly” from snippet code.
  - This is beginning to resemble a compiler!