## Revised Schedule

All dates, including assignment deadlines, are tentative and subject to change.

| Date | | Assignment Due | Reading | Topics |
|---|---|---|---|---|
| Feb | 14 | | 3.2, 4.1 | Logic Circuit Review; ALU Basics |
| | 16 | HW6 | ARITH | Computer Arithmetic; Floating Point |
| | 21 | | 4.1-2 | IJVM ISA; Mic-1 JVM Microarchitecture |
| | 23 | HW7 | 4.3 | IJVM Implementation on Mic-1 |
| | 28 | Lab3 | 4.4-6 | Improved Microarchitectures |
| Mar | 1 | HW8 | 2.2, 3.3, 4.5.1 | Memory Hierarchy; Primary Memory Design; Caches |
| | 6 | | 2.3,6.1 | Secondary Memory; Virtual Memory |
| | 8 | Lab4;HW9 | 8.1 | Parallel Architectures |
| | 13 | | | **Final Exam** (starting at **7:30 pm**) |

Key: All readings specified as numbers are sections from the Tanenbaum textbook; for example "7.1;7.3-4" means sections 1,3, and 4 from Tanenbaum Chapter 7. ARITH is an extra reading that will be made available on the course web page.

Additional readings may be assigned from time to time. Assigned selections should be read *before* the associated date.