CS 201 Section 1 Homework 7 – due 6pm, Wednesday, February 23, 2000

1. Consider three different ways of constructing a 16-bit adder:

- A ripple-carry adder built from 16 one-bit full adders.
- A two-level carry-lookahead adder built from 4 4-bit carry-lookahead adders (as described in class).
- A 5-level adder in which each level is a carry-select adder as described by Tanenbaum. (That is, the 16-bit adder is built using 3 8-bit adders, each 8-bit adder is built using 3 4-bit adders, each 4-bit adder is built using 3 2-bit adders, and each 2-bit adder is built using 3 1-bit full adders.)

For each type of adder, calculate

(a) the worst-case delay, measured in number of gates, required to calculate the overflow bit (the carry out of bit 16); and

(b) the total number of gates required.

2. Using the third, most efficient, multiplier described in class, show the steps involved in multiplying $0101_2 \times 0110_2$. For each step, say what happens, and show the contents of the product register.

3. Show the precise bit patterns for the IEEE single *and* double representations of the following numbers:

(a) 10.0_{10}

(b) 0.1_{10}

4. Suppose a single-precision IEEE number is stored in memory at address X. Write a sequence of SPARC instructions to multiply the number at X by 2 and store the result back at X. Accomplish this *without* using any floating-point instructions (don't worry about overflow).

5. Do Tanenbaum Exercise 4.3.

6. Do Tanenbaum Exercise 4.8.