

Portland State University
ECE 588/688

Chip Multiprocessors (Multicore Processors)

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Why CMPs?

- It is now possible to implement a single-chip multiprocessor in the same area as a wide issue superscalar
- Motivation
 - ◆ Area and Power has been increasing at rates greater than single-thread performance
 - ◆ Under-utilized superscalar execution resources
 - Branch mispredictions
 - Data dependences
 - Cache misses

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Comparing CMPs to Superscalar Processors

- Performance comparison depends on application
- Wall's classification
 - ◆ Applications with low to moderate parallelism
 - IPC < 10
 - Mostly integer applications
 - ◆ Applications with large amount of parallelism
 - IPC > 40
 - Mostly floating point applications

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Two Microarchitectures: 6-way SS vs. 4 2-way CMP

- For fair comparison, we need almost equal areas (die sizes) for SS and CMP
- Superscalar: 6-way R10000-like machine
 - ◆ More ports, bigger structures compared to the 4-way R10000
- CMP: 4 cores, each 2-way superscalar
 - ◆ Each core similar to the Alpha 21064 (1992)
 - ◆ Shared L2 cache
 - ◆ Clock speed?
- Design parameters: Paper Table 1
- Floor plans: Paper Figures 2 and 3

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Results: CMP vs. Superscalar

- Paper tables 4-7, figures 4-6
- CMP or Superscalar?
 - ◆ Low parallelism favors superscalar
 - ◆ Medium parallelism about even
 - ◆ High parallelism favors CMP

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Discussion: CMP Issues

- For CMPs, focus is less on core and more on “uncore”
 - ◆ Cache hierarchy and organization
 - ◆ Interconnection network
 - ◆ Bus interface
- Increased demand for bus bandwidth
- Cache miss latency
- Programmability
- Amdahl's law

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Reading Assignment

- Deborah T. Marr et al., "Hyper-Threading Technology Architecture and Microarchitecture," Intel Technology Journal, 2001 (Review)
- Alaa Alameldeen and David Wood, "IPC Considered Harmful for Multiprocessor Workloads," IEEE Micro, 2006 (Read)