Cray-1

- A successful Vector processor from the 1970s
  - Vector instructions are examples of SIMD
- Contains vector and scalar functional units
  - At the time, was the world’s fastest scalar processor (recall Amdahl’s law)
- Can have up to 1 million words of memory (64-bit words)
  - 10,500 pounds, consumes 115 kilowatts of power
  - Physical dimensions in paper figures 1, 2, 3, 4

Cray-1 Architecture

- Has both scalar and vector processing modes
- 12.5 ns clock (80 MHz)
- Word size: 64-bits
- Twelve functional units
- Register types and count (paper figure 5)
  - 24-bit address (A) registers: 8
  - 24-bit intermediate address (B) registers: 24
  - 64-bit scalar (S) registers: 8
  - 64-bit intermediate scalar (T) registers: 64
  - 64-element vector (V) registers, each element is 64-bits: 8
  - Vector length and vector mask registers
  - 64-bit real time clock (RT) register: 1
- 4 instruction buffers, each 64 parcels (16 bits per parcel)

Cray-1 Memory and I/O

- 1 M words \((2^{20})\), each word containing 64-bits + 8 check bits
- 16 independent memory banks, each 64K words
- 4 clock period bank cycle time (20 MHz)
- Bandwidth:
  - Transfer 1 word per cycle for B, T, and V registers
  - Transfer 1 word every 2 cycles for A and S registers
  - Transfer 4 words every cycle to instruction buffers
- Cray-1 doesn’t have caches – why?
- I/O
  - Four 6-channel groups of I/O channels
  - Each channel group served by memory every 4 cycles

Cray-1 Implementation Details

- Instruction formats (paper Table II)
- Register types and supporting registers
- A vector operation can have the following sources
  - Two vector register operands
  - One vector register operand and one scalar register operand
- Parallel vector operations can be processed in two ways
  - Using different functional units and V registers
  - Chaining: Using the result stream to one vector register simultaneously as the operand set for another operation in a different functional unit
    - Avoids overhead of storing intermediate results

Cray T3E Multiprocessor

- Implements logical shared address space over a distributed memory architecture
- Each processing element contains (paper figure 1)
  - DEC Alpha 21164 processor
    - 8KB L1 I-cache, 8KB L1 D-cache
    - 96 KB 3-way L2 cache
    - Allows two outstanding 64-byte cache line fills
  - Control chip
  - Router
    - 64 MB to 2 GB of memory
    - T3E has up to 2K processors connected by a 3D torus
Cray T3E E-Registers

- Memory interface is augmented with external (E) registers
  - 512 user + 128 system registers
  - Explicitly managed
  - All remote synchronization and communication done between E registers and memory
  - E registers extend the physical address space of a processor to cover full machine physical memory
- E-register operations:
  - Direct loads and stores between E regs & processor regs
  - Global E-register operations
    - Transfer data to/from remote or local memory
    - Perform messaging and atomic operation synchronization
- E registers extend cache space up to 2164 has cacheable memory space & non-cacheable I/O space
  - Most significant bit of 40-bit address distinguishes two types
  - I/O space used to access memory-mapped registers, including E registers

Cray T3E Global Communication

- Global virtual address (GVA) components: paper figure 2
- Address translation for global references: paper figure 4
- Global operations on E registers:
  - Gets: read memory into E-register
  - Puts: write E-register to memory
  - Both can operate on single word (32-bit or 64-bit) or vector (8 words) with arbitrary stride
    - Gets and Puts can be highly pipelined due to large number of E-registers
  - Maximum transfer rate between two nodes using vector Gets or Puts is 480 MB/s

Cray T3E Synchronization

- Atomic memory operations: paper Table 1
- Barriers and Eurekas synchronization
  - Barriers allow a set of participating processors to determine when all processors have signaled some event (e.g., reached a certain point in program execution)
  - Eurekas allow a set of processors to determine when any one processor has signaled an event (e.g., completion of parallel search)
- T3E has 32 barrier/eureka synchronization units (BSU) at each processor
  - Accessed as memory-mapped registers
  - States and events: paper Table 2 & 3
  - State transition diagrams: paper figure 6

Reading Assignment

- Thursday
  - B. Sinharoy et al., “Power5 System Microarchitecture,” IBM Journal of Research and Development, 2005 (Skim)
  - HW 4 due Thursday
  - Project progress report due Thursday Feb 18