Chip Multiprocessors (Multicore Processors)
Why CMPs?

- It is now possible to implement a single-chip multiprocessor in the same area as a wide issue superscalar

**Motivation**

- Area and Power has been increasing at rates greater than single-thread performance
- Under-utilized superscalar execution resources
  - Branch mispredictions
  - Data dependences
  - Cache misses
Comparing CMPs to Superscalar Processors

- Performance comparison depends on application

- Wall’s classification
  - Applications with low to moderate parallelism
    - IPC < 10
    - Mostly integer applications
  - Applications with large amount of parallelism
    - IPC > 40
    - Mostly floating point applications
Two Microarchitectures: 6-way SS vs. 4 2-way CMP

- For fair comparison, we need almost equal areas (die sizes) for SS and CMP
- Superscalar: 6-way R10000-like machine
  - More ports, bigger structures compared to the 4-way R10000
- CMP: 4 cores, each 2-way superscalar
  - Each core similar to the Alpha 21064 (1992)
  - Shared L2 cache
  - Clock speed?
- Design parameters: Paper Table 1
- Floor plans: Paper Figures 1 and 2
Results: CMP vs. Superscalar

- Paper tables 5-7, figures 4-6
- CMP or Superscalar?
  - Low parallelism favors superscalar
  - Medium parallelism about even
  - High parallelism favors CMP
Discussion: CMP Issues

- For CMPs, focus is less on core and more on “uncore”
  - Cache hierarchy and organization
  - Interconnection network
  - Bus interface
- Increased demand for bus bandwidth
- Cache miss latency
- Programmability
- Amdahl’s law
Reading Assignment