Project

- Due Friday, December 7
- Report should include
  - Description of your code
  - Results on all spec95 integer benchmarks
    - 100 million fast forward, 20 million timing simulations
  - Compare
    - baseline
    - 16 wide superscalar with trace cache
    - 16 wide superscalar with conventional instruction cache
  - Size up buffers and all pipe stages appropriately for 16 wide configuration
  - Report IPC, ICache, and trace cache hit rates