RISC I

- RISC == Reduced Instruction Set Computer
- Alternative to Complex Instruction Set Computer
- Simple instructions and addressing modes
  - High effective throughput (low CPI)
    - Effective pipeline since most instructions execute in one cycle
  - Short cycle time
  - Short design cycle
- But larger programs
  - 2x larger than VAX 11/780
RISC Instruction Format

- Most instructions execute in one cycle
- Fixed size
- Only loads and stores access memory
  - Rest of instructions operate between registers
- Support high level languages (HLL)
RISC I Design Approach

- New architectures should be designed for HLL
- Does not matter which part of the system is in hardware and which is in software
- Architect makes tradeoffs to build a cost effective system
  - Which language constructs are used frequently
  - What is the distribution of various instructions
  - Dedicate available area for the most frequent constructs and operations
    - Amdahl’s law
Amdahl’s Law

Overall speedup = \( \frac{1}{((1 - P) + \frac{P}{S})} \)

\( P = \) proportion of computation improved

\( S = \) improvement speedup
RISC I Performance Features

- Large number of registers addressable by instructions
  - 32 general purpose registers (GPRs)
- Register windows for fast call and return operations
- Delayed branch
Delayed Branch

Static Program

I1
Jump Target
I2

Target: I3

Branch execution sequence: I1, I3
Delayed branch execution sequence: I1, I2, I3
Reading Assignment