Due November 14

1. Out-of-order superscalar architecture is one approach for achieving high performance on general purpose, non-numeric programs.

   Another approach is to use very long instruction word (VLIW) architectures, a recent reincarnation of which is explicitly parallel instruction computers (EPIC) implemented in Intel Itanium processors.

   a) Describe the ideas and the technology behind VLIW and EPIC architectures.
   b) Write a comparative analysis of the VLIW/EPIC vs. out-of-order superscalar architectures. Compare the mechanisms used for overcoming various performance bottlenecks in the pipeline in both architectures, emphasizing the pros and cons of each approach. Consider technical as well as business factors, e.g. deployment cost, time to market, etc... in your analysis.

2. Out-of-order superscalar processors achieve performance in the presence of long latency operations such as loads that miss the first level cache and floating point operations, by issuing independent instructions that can execute immediately, while buffering instructions that depend on the long latency operations. The out of order hardware looks ahead in the dynamic instruction stream for parallel instructions that can issue, thus keeping the pipeline busy.

   Conventional out-of-order processors however have limited hardware capacity to buffer waiting instructions, and fetch and commit instructions in program order. As a result, severe limitation on the performance of many applications is frequently observed due to branch mispredictions and extremely long latency to DRAM.

   Various researchers have recently proposed new architectures that relax in-order fetch and in-order commit restrictions of conventional superscalars. Write a survey of these new architectures and describe how they propose to improve performance in the presence of branch mispredictions and cache misses to DRAM.