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Design and experimentation of BSFQ logic devices

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Abstract. Rapid single flux quantum (RSFQ) logic needs synchronous pulses for each gate, so the clock-wiring problem is more serious when designing larger scale circuits with this logic. So we have proposed a new SFQ logic which follows Boolean algebra perfectly by using set and reset pulses. With this logic, the level information of current input is transmitted with these pulses generated by level-to-pulse converters, and each gate calculates logic using its phase level made by these pulses. Therefore, our logic needs no clock in each gate. We called this logic 'Boolean SFQ (BSFQ) logic'. In this paper, we report design and experimentation for an AND gate with inverting input based on BSFQ logic. The experimental results for OR and XOR gates are also reported.

1. Introduction

The primary logic for single flux quantum circuits is the rapid single flux quantum (RSFQ) logic that has been proposed by Likharev's group [1]. Many approaches have been made with this logic, and it is not too much to say that RSFQ supports today's superconductive electronics. Recently T flip–flops operating at 370 GHz and fundamental logic gates operating at several tens of gigahertz were reported. However, this is pulse logic which recognizes a '1' state when an SFQ pulse comes and '0' state when no pulses come at a certain time. Therefore each fundamental logic gate needs synchronous pulses and has 1 clock delay. Several studies have been proposed such as DDST [2] and dual-rail logic for asynchronous circuits [3] to improve this logic, but the problem that each gate needs clock timing remains.

So we have proposed a new SFQ logic which follows Boolean algebra perfectly by using set and reset pulses [4]. We called this logic 'Boolean SFQ (BSFQ) logic'. This logic is a level logic like CMOS and does not need a clock for each gate. A clock is required for each block of the combination circuit when sequential circuits are made up, but the number of clock wires is much less than for RSFQ logic and the delay is 1 clock for each block of the combination circuit.

2. BSFQ logic

2.1. Level to pulse converter

This was called 'dc-to-SFQ converter' previously, but the old name often led to confusion with the RSFQ dc-to-SFQ converter and the operation seems to be difficult to understand by that name. Therefore we renamed ours to the above-mentioned 'level-to-pulse converter'.

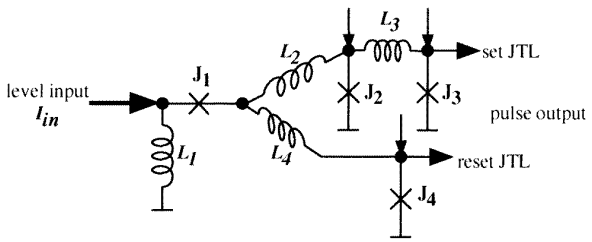

Figure 1. Level-to-pulse converter.

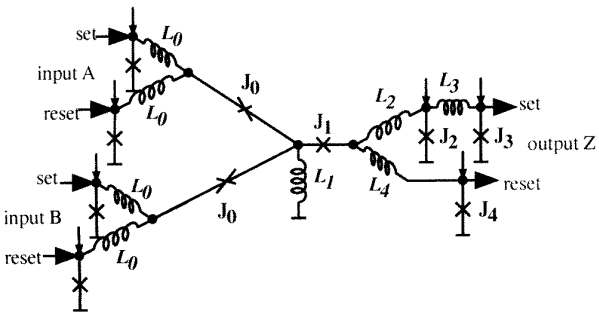

Figure 2. Two-input AND, OR gate.

This circuit (figure 1) converts the level information of input current I_{in} to SFQ pulses. If I_{in} changes its state from low to high, the phase level of inductance L_1 increases, and a pair of SFQs is generated under L_2 and L_4. An SFQ on the side of L_2 is only transmitted to set JTL because I_{c2} is smaller than I_{c3}, and another SFQ remains trapped at the converter. Then when I_{in} returns its state to low, J_1 is broken and the left SFQ is also transmitted to reset JTL, and the converter returns to the initial state.

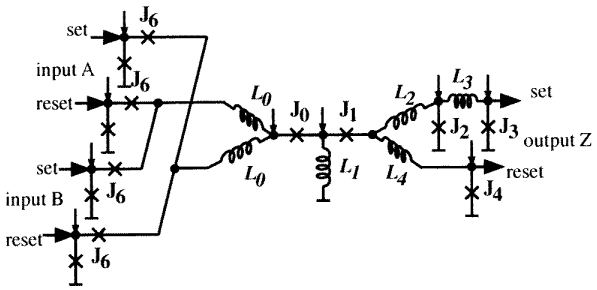

Figure 3. XOR gate.

2.2. AND, OR gates

AND and OR gates (figure 2) have the same circuit structure and only parameters of the elements are different. Each gate is divided into two parts: pulse-to-level converting part (left side from J_0 in figure 2) and level-to-pulse converting part. When input current is set to high, that is, the set pulse comes to a gate, the phase level of L_1 increases because the SFQ is trapped the loop which contains J_0 and L_1. Then the level-to-pulse converting part generates a pair of SFQs. If both of the inputs are set to high, the phase of L_1 increases twofold. The phase threshold of L_1, which the set pulse is transmitted on, is set to 2 steps at the AND gate and 1 step at the OR gate. Adjusting inductance and biases sets these thresholds. Trapped SFQ is coupled with another SFQ which was transmitted from the reset JTL and disappears.

2.3. Inverter

The BSFQ circuit is a dual-rail logic. An inverter with a dual-rail logic can be generally obtained only by crossing lines, but fundamental gates with the present BSFQ logic use the same inductance L_0 to both set and reset input terminals, so that it is not able to distinguish set and reset lines. Therefore an inverter with BSFQ logic can be obtained by putting an SFQ in the relevant reset input terminal at the initial state.

2.4. XOR gate

It is well known that an XOR gate can be made from a combination of the above-mentioned gates, but the number of junctions is several times larger than for other gates. So we propose another type of XOR gate (figure 3). This uses a level-to-pulse converter and an RSFQ confluence buffer. If either input becomes high, an SFQ is trapped the loop which contains J_0 and L_1, and a set pulse is output. Then when the input becomes low or another input becomes high, the trapped SFQ is coupled with the subsequent SFQ and disappears.

3. Design and experimentation

We designed AND with input-invert terminal, OR (figure 4) and XOR circuits. Each circuit has two level-to-pulse converters and a pulse-to-level converter because all of these circuits are two-input one-output circuits.

The chip was fabricated by NEC Corporation using their standard $Nb/AlO_x/Nb$ process [5].

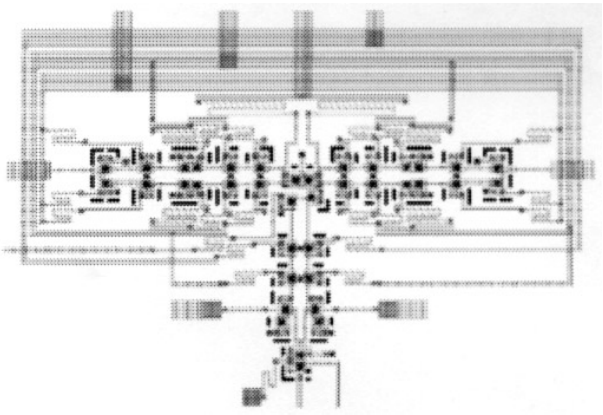

Figure 4. Layout of an OR circuit.

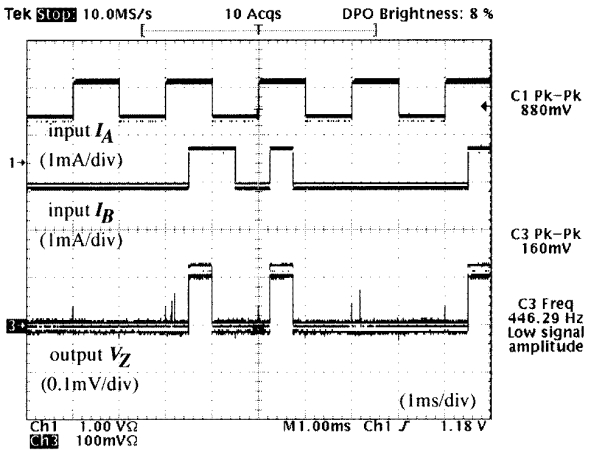

Figure 5. AND gate without input-inverting biases.

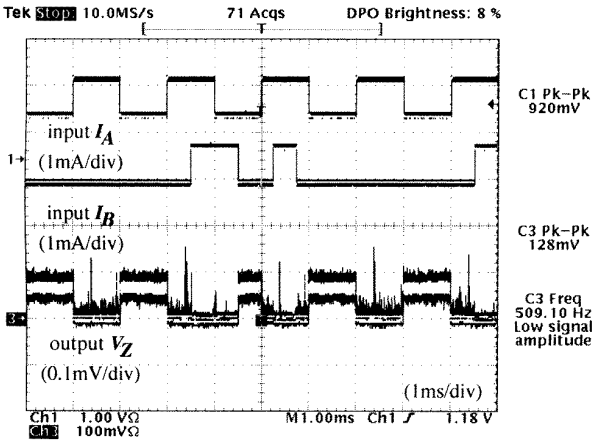

Figure 6. AND gate with input-inverting biases (equivalental to NOR gate).

4. Results

Figures 5 and 6 are as the results of the same AND circuit. The input-inverting terminals are connected to the confluence buffers with RSFQ dc-to-SFQ converters. If a terminal is set to high at the initial state, the input whose reset JTL has

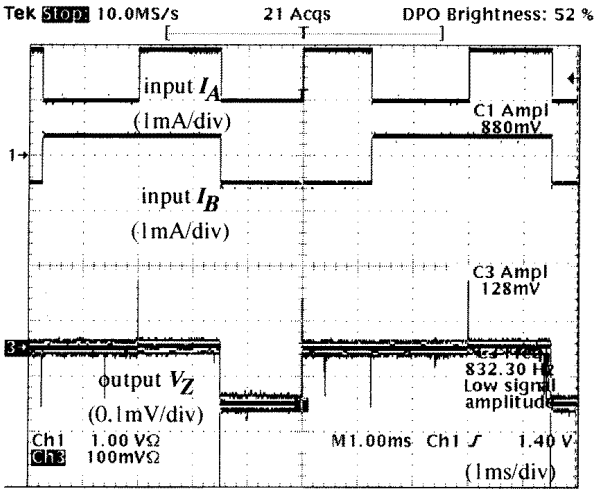

Figure 7. OR gate.

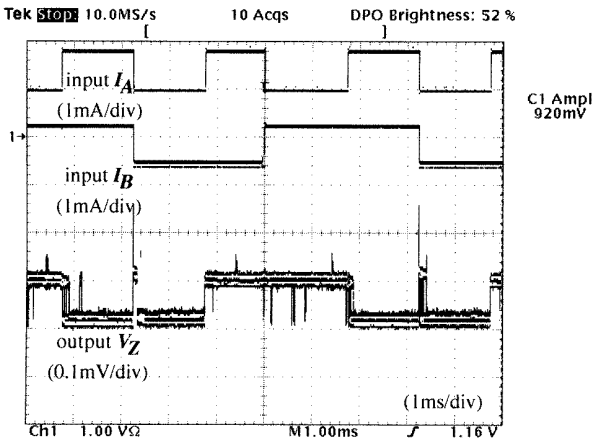

Figure 8. XOR gate.

the connection to the confluence buffer is inverted. Both of the input-invert terminals were set to high at the initial state in figure 6. Therefore, both of inputs were inverted and this circuit operated as (NOT A) AND (NOT B), that is, A NOR B.

Figures 7 and 8 show the results of OR and XOR gates, respectively. Output voltage changes to high for a short time when both of the inputs change from high to lows (figure 7). The reason for this is probably that either of the input signals is delayed in the measurement system, and the gate seems to operate correctly.

5. Discussion

Fundamental logic gates with BSFQ operated correctly. However, if an error occurs somewhere from unexpected flux trapping in the circuits, these gates are not able to recover themselves with present logic, and we must make the circuit temperature higher than the critical temperature or use some forcible measures. So it is very difficult to correct the operation of a complicated circuit when even an error occurs. We have designed and tested some combination circuits such as full adder and decoder, but have not obtained the results with proper outputs yet.

We are now designing improved BSFQ logic gates to solve this problem. The improved gates are able to correct the operation themselves, and an inverter can be obtained simply by crossing lines like other dual-rail logics.

6. Conclusion

We have designed and obtained experimental results with correct operation of fundamental BSFQ logic gates, that is, AND, OR, inverter and XOR. So we will make further studies for designing the improved BSFQ logic gate, many input/output combination circuits and sequential circuits.

Acknowledgments

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