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ASP-DAC 2003 Best Paper Award Candidates

- 1D-1 **SAT-based Sequential Depth Computation**
M. Mneimneh, K. Sakallah – University of Michigan, USA
- 2B-1 **Approximate Formulae Approach for Efficient Inductance Extraction**
A. Kurokawa – Semiconductor Technology Academic Research Center, Japan, T. Sato – Hitachi Ltd., Japan, H. Masuda – Semiconductor Technology Academic Research Center, Japan
- 3A-2 **Towards On-Chip Fault-Tolerant Communication**
T. Dumitras, S. Kerner, R. Marculescu – Carnegie Mellon University, USA
- 3C-1 **Statistical Delay Computation Considering Spatial Correlations**
A. B. Agarwal, D. Blaauw – University of Michigan, USA, S. Sundareswaran, V. Zolotov, M. Zhao, K. Gala, R. Panda – Motorola, USA
- 4C-1 **Efficient LUT-Based FPGA Technology Mapping for Power Minimization**
H. Li, W.-K. Mak, S. Katkoori – University of South Florida, USA
- 5A-1 **Fast Buffer Planning and Congestion Optimization in Interconnect-driven Floorplanning**
K. W. C. Wong, E. F.Y. Young – The Chinese University of Hong Kong, Hong Kong
- 5D-2 **Design of a Scalable RSA and ECC Crypto-Processor**
M.-C. Sun, C.-P. Su, C.-T. Huang, C.-W. Wu – National Tsing Hua University, Taiwan
- 7A-1 **Run-Time Energy Estimation in System-On-a-Chip Designs**
J. Haid, G. Kaefer, C. Steger, R. Weiss – Graz University of Technology, Austria
- 7D-2 **A comparison of the RTU hardware RTOS with a Hardware/Software RTOS**
J. Lee, V. J. Mooney III – Georgia Institute of Technology, USA, A. Daleby, Karl Ingstrom – Malardalens University, Sweden, T. Klevin, Lennart Lindh – Malardalens University / RealFast, Sweden
- 8B-1 **Congestion Driven Incremental Placement Algorithm for Standard Cell Layout**
Z. Li, W. Wu, X. Hong – Tsinghua University, China
- 8C-1 **Experience in Critical Path Selection For Deep Sub-Micron Delay Test and Timing Validation**
J.-J. Liu, L.-C. Wang, A. Krstic, K.-T. Cheng – UC-Santa Barbara, USA
- 8D-1 **Using Red-Black Interval Trees in Device-Level Analog Placement with Symmetry Constraints**
F. Balasa, S. C. Maruvada, K. Krishnamoorthy – University of Illinois at Chicago, USA

ASP-DAC 2003 Table of Contents

ASP-DAC 2003 General Chair's Message	iii
Technical Program Co-Chairs' Message	iv
University LSI Design Contest	v
Keynote Addresses	vi
ASP-DAC 2002/VLSI 2002 Best Papers	x
ASP-DAC 2003 Best Paper Award Candidates	xi
ASP-DAC 2003 Organizing Committee	xii
ASP-DAC 2003 Steering Committee	xvi
ASP-DAC 2003 Technical Program Committee	xx
University LSI Design Contest Committee	xxiii
List of Reviewers	xxiv

Session 1A
Bus Encoding and Memory Optimization

Co-Chairs: Luca Benini, Hiroshi Nakamura

1A-1	BEAM: Bus Encoding Based on Instruction-Set-Aware Memories <i>Yazdan Aghaghiri, Farzan Fallah, Massoud Pedram</i>	3
1A-2	Irredundant Address Bus Encoding Techniques Based on Adaptive Codebooks for Low Power <i>Satoshi Komatsu, Masahiro Fujita</i>	9
1A-3	Multi-Parametric Improvements for Embedded Systems Using Code-Placement and Address Bus Coding <i>Sri Parameswaran, Joerg Henkel</i>	15
1A-4	Memory Access Pattern Analysis and Stream Cache Design for Multimedia Applications <i>Junghee Lee, Chanik Park, Soonhoi Ha</i>	22

Session 1B
DSM Interconnect and Gate Issues

Co-Chairs: Masanori Hashimoto, Kaushik Roy

1B-1	A Statistical Gate Delay Model for Intra-chip and Inter-chip Variabilities <i>Kenichi Okada, Kento Yamaoka, Hidetoshi Onodera</i>	31
1B-2	A Fast and Accurate Method for Interconnect Current Calculation <i>Muzhou Shao, D. F. Wong, Youxin Gao, Huijing Cao, Li-Pen Yuan</i>	37
1B-3	Calculating the Effective Capacitance for the RC Interconnect in VDSM Technologies <i>Soroush Abbaspour, Massoud Pedram</i>	43
1B-4s	Reduction of Crosstalk Noise by Optimizing 3-D Configuration of the Routing Grid <i>Atsushi Sakai, Takashi Yamada, Yoshifumi Matsushita, Hiroto Yasuura</i>	49
1B-5s	Design Tools for 3-D Integrated Circuits <i>Shamik Das, Anantha Chandrakasan, Rafael Reif</i>	53

Session 1C
Embedded Software: Task Scheduling and Compilation

Co-Chairs: Nikil Dutt, Akira Fukuda

1C-1	An On-line Approach for Power Minimization in QoS Sensitive Systems <i>Jennifer L. Wong, Miodrag Potkonjak, Gang Qu</i>	59
1C-2	Energy Minimization of Real-time Tasks on Variable Voltage Processors with Transition Energy Overhead <i>Yumin Zhang, Xiaobo Sharon Hu, Danny Z. Chen</i>	65
1C-3	Register Aware Scheduling for Distributed Cache Clustered Architecture <i>Zhong Wang, Xiaobo Sharon Hu, Edwin H. -M. Sha</i>	71
1C-4	Data Partitioning for Maximal Scratchpad Usage <i>Manish Verma, Stefan Steinke, Peter Marwedel</i>	77

Session 1D
Combinational and Sequential Verification

Co-Chairs: Kiyoharu Hamaguchi, Yuji Kukimoto

1D-1	SAT-based Sequential Depth Computation <i>Maher Mneimneh, Karem Sakallah</i>	87
1D-2	Logic Verification Based on Diagnosis Techniques <i>Veneris Andreas, Smith Alexander, Abadir Magdy</i>	93
1D-3	Algorithms for Compacting Error Traces <i>Yirng-An Chen, Fang-Sung Chen</i>	99

1D-4s	Transaction-based Waveform Analysis for IP Selection <i>Jian Liu, Eugene Shragowitz</i>	104
1D-5s	An Automatic Interconnection Rectification Technique for SoC Design Integration <i>Chun-Yao Wang, Shing-Wu Tung, Jing-Yang Jou</i>	108

<p>Session 2A C-Based Specification and ASIP Design</p>

Co-Chairs: Nagisa Ishiura, Wolfgang Rosenstiel

2A-1	Typing Abstractions and Management in a Component Framework <i>Frederic Doucet, Sandeep Shukla, Rajesh Gupta</i>	115
2A-2	Event-Driven Observability Enhanced Coverage Analysis of C Programs for Functional Validation <i>Farzan Fallah, Indradeep Ghosh, Masahiro Fujita</i>	123
2A-3	Trace-driven Rapid Pipeline Architecture Evaluation Scheme for ASIP Design <i>Jun Kyoung Kim, Tag Gon Kim</i>	129
2A-4	A Hardware/Software Partitioning Algorithm for SIMD Processor Cores <i>Koichi Tachikake, Nozomu Togawa, Yuichiro Miyaoka, Jinku Choi, Masao Yanagisawa, Tatsuo Ohtsuki</i>	135

<p>Session 2B On-Chip Inductance</p>
--

Co-Chairs: Hidetoshi Onodera, Martin D. F. Wong

2B-1	Approximate Formulae Approach for Efficient Inductance Extraction <i>Atsushi Kurokawa, Takashi Sato, Hiroo Masuda</i>	143
2B-2	Accurate Prediction of the Impact of On-chip Inductance on Interconnect Delay Using Electrical and Physical Parameters <i>Takashi Sato, Toshiki Kanamoto, Atsushi Kurokawa, Yoshiyuki Kawakami, Hiroki Oka, Tomoyashi Kitaura, Hiroyuki Kobayashi, Masanori Hashimoto</i>	149
2B-3	A Metric for Analyzing Effective On-Chip Inductive Coupling <i>Guoan Zhong, Cheng-Kok Koh, Kaushik Roy</i>	156
2B-4	Determination of Worst-Case Crosstalk Noise for Non-Switching Victims in GHz+ Interconnects <i>Jun Chen, Lei He</i>	162

<p>Session 2C Circuit and Modeling</p>
--

Co-Chairs: Hiroaki Ueno, Zhiping Yu

2C-1	Recent Developments in ESD Protection for RF ICs <i>Albert Z. H. Wang</i>	171
------	---	-----

2C-2	Temperature-Independence-Point Properties for 0.1μm-Scale Pocket-Implant Technologies and the Impact on Circuit Design <i>Kazuya Hisamitsu, Hiroaki Ueno, Masayasu Tanaka, Daisuke Kitamaru, Mitiko Miura-Mattausch, Hans Juergen Mattausch, Shigetaka Kumashiro, Tetsuya Yamaguchi, Kyoji Yamashita, Noriaki Nakayama</i>	179
2C-3	Behavioral Modeling of EM Devices by Selective Orthogonal Matrix Least-Squares Method <i>Yuichi Tanji, Masaya Suzuki, Takayuki Watanabe, Hideki Asai</i>	184

<p>Session 2D</p> <p>Logic Optimization and Technology Mapping</p>
--

Co-Chairs: Giovanni De Micheli, Shin-Ichi Minato

2D-1	A BDD-based Fast Heuristic Algorithm for Disjoint Decomposition <i>Tomas Bengtsson, Andrés Martinelli, Elena Dubrova</i>	191
2D-2	Logic Optimization for Asynchronous Speed Independent Controllers Using Transduction Method <i>Hiroshi Saito, Hiroshi Nakamura, Masahiro Fujita, Takashi Nanya</i>	197
2D-3	Technology Mapping for Low Leakage Power and High Speed with Hot-Carrier Effect Consideration <i>Chang Woo Kang, Massoud Pedram</i>	203
2D-4s	Synthesis of High Performance Low Power PTL Circuits <i>Debasis Samanta, M. C. Dharmadeep, Ajit Pal</i>	209
2D-5s	A Technology Mapping Algorithm for Heterogeneous FPGAs <i>Chi-Chou Kao, Yen-Tai Lai</i>	213

<p>Session 3A</p> <p>SoC and NoC</p>
--

Co-Chairs: Masahiro Fujita, Rajesh Gupta

3A-1	Combining Architecture Exploration and a Path to Implementation to Build a Complete SoC Design Flow from System Specification to RTL <i>Mohamed-Anouar Dziri, Firaz Samet, Flavio Wagner, Wander Cesario, Ahmed A. Jerraya</i>	219
3A-2	Towards On-Chip Fault-Tolerant Communication <i>Tudor Dumitras, Sam Kerner, Radu Marculescu</i>	225
3A-3	Energy-Aware Mapping for Tile-based NoC Architectures under Performance Constraints <i>Jingcao Hu, Radu Marculescu</i>	233

<p>Session 3B</p> <p>Clock Synthesis and Capacitance Extraction</p>

Co-Chairs: Masato Eda, Massoud Pedram

3B-1	Adaptive Wire Adjustment for Bounded Skew Clock Distribution Network <i>Haydar Saaied, Dhamin Al-Khalili, Asim Al-Khalili, Mohamed Nekili</i>	243
3B-2	Power Minimization by Clock Root Gating <i>Qi Wang, Sumit Roy</i>	249
3B-3	BBE: Hierarchical Computation of 3-D Interconnect Capacitance with BEM Block Extraction <i>Taotao Lu, Zeyi Wang, Xianlong Hong</i>	255
3B-4	Improving Boundary Element Methods for Parasitic Extraction <i>Shu Yan, Jianguo Liu, Weiping Shi</i>	261

<p>Session 3C Analysis Methodologies for Circuits</p>

Co-Chairs: Naoyuki Shigyo, Albert Z. H. Wang

3C-1	Statistical Delay Computation Considering Spatial Correlations <i>Aseem Bijay Agarwal, David Blaauw, Savithri Sundareswaran, Vladimir Zolotov, Min Zhao, Kaushik Gala, Rajendran Panda</i>	271
3C-2	Predicting Short Circuit Power from Timing Models <i>Emrah Acar, Ravishankar Arunachalam, Sani R. Nassif</i>	277
3C-3	RCLK-VJ Network Reduction with Hurwitz Polynomial Approximation <i>Zhanhai Qin, Chung-Kuan Cheng</i>	283

<p>Session 3D Symbolic Simulation and Verification</p>
--

Co-Chairs: Yirng-An Chen, Shinji Kimura

3D-1	Gate-Level Simulation of Quantum Circuits <i>George F. Viamontes, Manoj Rajagopalan, Igor L. Markov, John P. Hayes</i>	295
3D-2	Enhanced Symbolic Simulation for Efficient Verification of Embedded Array Systems <i>Tao Feng, Li-C. Wang, Kwang-Ting (tim) Cheng, Manish Pandey, Magdy S. Abadir</i>	302
3D-3s	Hardware Verification Using ANSI-C Programs as a Reference <i>Edmund Clarke, Daniel Kroening</i>	308
3D-4s	Evaluation of Multiple-Output Logic Functions Using Decision Diagrams <i>Yukihiro Iguchi, Tsutomu Sasao, Munehiro Matsuura</i>	312

<p>Session 4A Modeling for Floorplan</p>
--

Co-Chairs: Dinesh P. Mehta, Yasuhiro Takashima

4A-1	A Simulated Annealing Approach with Sequence-Pair Encoding Using a Penalty Function for Placement Problem with Boundary Constraints <i>Satoshi Tayu</i>	319
------	---	-----

4A-2	Multi-level Placement for Large-Scale Mixed-Size IC Designs <i>Chin-Chih Chang, Jason Cong, Xin Yuan</i>	325
4A-3	Selected Sequence-Pair: An Efficient Decodable Packing Representation in Linear Time Using Sequence-Pair <i>Chikaaki Kodama, Kunihiko Fujiyoshi</i>	331
4A-4s	An Extended Representation of Q-sequence for Optimizing Channel-Adjacency and Routing-Cost <i>Changwen Zhuang, Keishi Sakanushi, Liyan Jin, Yoji Kajitani</i>	338
4A-5s	Non-slicing Floorplans with Boundary Constraints Using Generalized Polish Expression <i>De-Sheng Chen, Chang-Tzu Lin, Yi-Wen Wang</i>	342

Session 4B
(Special Session) Panel Discussion: Anatomy of Platform-Based Design: Is It the Savior of UDSM SoC Design Crisis?

Organizers: Tadahiko Nakamura, Takahide Inoue
Moderator: Takahide Inoue
Panelists: Bob Altizer, Ken Chen, Jun Iwamura, Masasuke Kishi, Grant Martin, Augusto De Oliveira

Abstract	349
-----------------------	-----

Session 4C
Reconfigurable Systems

Co-Chairs: Reiner Hartenstein, Kiyoshi Oguri

4C-1	Efficient LUT-Based FPGA Technology Mapping for Power Minimization <i>Hao Li, Wai-Kei Mak, Srinivas Katkoori</i>	353
4C-2	Optimal Reconfiguration Sequence Management <i>Soheil Ghiasi, Majid Sarrafzadeh</i>	359
4C-3s	On Improving FPGA Routability Applying Multi-level Switch Boxes <i>Jiping Liu, Hongbing Fan, Yu-Liang Wu</i>	366
4C-4s	An Image Retrieval System Using FPGAs <i>Koji Nakano, Etsuko Takamichi</i>	370
4C-5	Logic Foundry: Rapid Prototyping of FPGA-based DSP Systems <i>Gary Spivey, Shuvra Bhattacharyya, Kazuo Nakajima</i>	374

Session 4D
Design Methodologies for Leading Edge Low-Power Design

Co-Chairs: Tohru Ishihara, Radu Marculescu

4D-1	Advanced Power Management Techniques: Going Beyond Intelligent Shutdown <i>Luca Benini</i>	385
4D-2	Design Technologies for Low Power Microprocessors <i>Toshihiro Hattori</i>	390
4D-3	Design Methodology of Low-Power CMOS RF-ICs <i>Tsuneo Tsukahara</i>	394
4D-4s	Minimizing Total Power by Simultaneous Vdd/Vth Assignment <i>Ashish Srivastava, Dennis Sylvester</i>	400
4D-5s	A Low Power CMOS Circuit with Variable Source Scheme (VSCMOS) <i>Takeo Yasuda, Kohji Hosokawa</i>	404

<p>Session 5A Performance Driven Floorplan</p>
--

Co-Chairs: Yao-Weng Chang, Shin'ichi Wakabayashi

5A-1	Fast Buffer Planning and Congestion Optimization in Interconnect-driven Floorplanning <i>Keith W. C. Wong, Evangeline F. Y. Young</i>	411
5A-2	Interconnect-Driven Floorplanning by Searching Alternative Packings <i>Chiu-Wing Sham, Evangeline F. Y. Young, Hai Zhou</i>	417
5A-3s	Noise-Aware Buffer Planning for Interconnect-Driven Floorplanning <i>Shu-Min Li, Yih-Huai Cherng, Yao-Wen Chang</i>	423
5A-4s	Floorplanning with Power Supply Noise Avoidance <i>Hung-Ming Chen, Li-Da Huang, I-Min Liu, Minghorng Lai, D. F. Wong</i>	427
5A-5s	Simultaneous Floorplanning and Buffer Block Planning <i>Iris Hui-Ru Jiang, Yao-Wen Chang, Jing-Yang Jou, Kai-Yuan Chao</i>	431
5A-6s	A Buffer Planning Algorithm Based on Dead Space Redistribution <i>Song Chen, Xianlong Hong, Sheqin Dong, Yuchun Ma, Yici Cai, Chungkuan Cheng, Jun Gu</i>	435

<p>Session 5B (Special Session) Invited Talks: Virtual Core Based Reuse Methodology for SoC Design</p>
--

Co-Chairs: Masahiro Fujita, Sandeep K. Shukla

5B-1	VCore- Based Design Methodology <i>Michiaki Muraoka, Hideyuki Hamada, Hiroaki Nishi, Toshihiko Tada, Yoichi Onishi, Toshinori Hosokawa</i>	441
5B-2	Synthesis for SoC Architecture Using VCores <i>Hiroaki Nishi, Michiaki Muraoka, Rafael K. Morizawa, Hideaki Yokota, Hideyuki Hamada</i>	446
5B-3	VCore-based Platform for SoC Design <i>Yoichi Onishi, Michiaki Muraoka, Makoto Utsuki, Naoyuki Tsubaki</i>	453

5B-4	VCDS Tool Demonstration	
	<i>Rafael Kazumiti Morizawa</i>	459

Session 5C
(Special Session) Invited Talks + Panel Discussion: Adaptive Computing: What Can It Do, Where Can It Go?

Organizer: Robert Reuss
Moderators: Jose Munoz, Toshiaki Miyazaki
Panelists: Nader Bagherzadeh, Prith Banerjee, Brad Hutchings, Jose Munoz, Brian Schott

	Abstract	463
5C-1	DARPA'S Adaptive Computing Systems Program	
	<i>Jose Munoz</i>	464
5C-2	Applications of Adaptive Computing Systems for Signal Processing Challenges	
	<i>Brian Schott, Robert Parker</i>	465
5C-3	Interactive Ray Tracing on Reconfigurable SIMD MorphoSys	
	<i>H. Du, M. Sanchez-Elez, N. Tabrizi, N. Bagherzadeh, M. L. Anido, M. Fernandez</i>	471
5C-4	An Overview of a Compiler for Mapping MATLAB Programs onto FPGAs	
	<i>Prith Banerjee</i>	477
5C-5	Issues in Debugging Highly Parallel FPGA-based Applications Derived from Source Code	
	<i>Karl Scott Hemmert, Brad L. Hutchings</i>	483

Session 5D
Leading Edge Design Examples

Co-Chairs: Seongsoo Lee, Takashi Miyamori

5D-1s	Implementation of the Super-Systolic Array for Convolution	
	<i>Gi-Yong Song, Jae-Jin Lee</i>	491
5D-2s	Design of a Scalable RSA and ECC Crypto-Processor	
	<i>Ming-Cheng Sun, Chih-Pin Su, Chih-Tsun Huang, Cheng-Wen Wu</i>	495
5D-3s	A Reconfigurable, Power-Scalable Rake Receiver IP for W-CDMA	
	<i>Alessandro Bianco, Alberto Dassatti, Maurizio Martina, Andrea Molino, Fabrizio Vacca</i>	499
5D-4s	Robust High-Performance Low-Power Carry Select Adder	
	<i>Woopyo Jeong, Kaushik Roy</i>	503
5D-5s	Full-Custom vs. Standard-Cell Design Flow - An Adder Case Study	
	<i>Henrik Eriksson, Tomas Henriksson, Per Larsson-Edefors, Christer Svensson</i>	507
5D-6s	A 500-MHz Low-Power Five-Port CMOS Register File	
	<i>Jiajing Wang, Qianling Zhang</i>	511

5D-7s	An Effective SDRAM Power Mode Management Scheme for Performance and Energy Sensitive Embedded Systems <i>Ning-Yaun Ker, Chung-Ho Chen</i>	515
5D-8s	Branch Predictor Design and Performance Estimation for a High Performance Embedded Microprocessor <i>Sang-Hyuk Lee, Il-Kwan Kim, Lynn Choi</i>	519

<p>Session 6A Design Space Exploration</p>
--

Co-Chairs: Tohru Ishihara, Sri Parameswaran

6A-1	Accelerating Design Space Exploration Using Pareto-Front Arithmetics <i>Christian Haubelt, Jürgen Teich</i>	525
6A-2	Quality-Driven Design by Bitwidth Optimization for Video Applications <i>Yun Cao, Hiroto Yasuura</i>	532
6A-3	Arbitrary Long Digit Integer Sorter HW/SW Co-Design <i>Shun-Wen Cheng</i>	538

<p>Session 6B (Special Session) Panel Discussion: Roles of Funding Agencies in Technology-driven Economic Development</p>

Organizer: Kazuo Nakajima
Moderators: Kazuo Nakajima, Brian Schott
Panelists: Tokinori Kozawa, Jose Munoz, Wolfgang Rosenstiel, Sakae Takahashi, Chen-Wen Wu

Abstract	547
-----------------------	-----

<p>Session 6C (Special Session) Invited Talk: Legal Protection for Semiconductor Intellectual Property</p>
--

Chair: Masaharu Imai

6C-1	Legal Protection for Semiconductor Intellectual Property (IP) <i>Yoichi Oshima</i>	551
------	--	-----

<p>Session 6D (Special Session) Presentation and Poster Session: University LSI Design Contest</p>
--

Co-Chairs: Tomohisa Wada, Shoji Kawahito

6D-1	Design and Implementation of a Video-Oriented Network-Interface-Card System <i>Ming-Chih Chen, Shen-Fu Hsiao, Cheng-Hsien Yang</i>	559
------	--	-----

6D-2	A Highly Efficient AES Cipher Chip <i>Chih-Pin Su, Tsung-Fu Lin, Chih-Tsun Huang, Cheng-Wen Wu</i>	561
6D-3	Implementation of Fast CRC Calculation <i>Tomas Henriksson, Dake Liu</i>	563
6D-4	Design of a CMOS Test Chip for Package Models and I/O Characteristics Verification <i>Chetan Deshpande, Tom Chen</i>	565
6D-5	A Still Image Encoder Based on Adaptive Resolution Vector Quantization Employing Needless Calculation Elimination Architecture <i>Masanori Fujibayashi, Toshiyuki Nozawa, Takahiro Nakayama, Kenji Mochizuki, Koji Kotani, Shigetoshi Sugawa, Tadahiro Ohmi</i>	567
6D-6	Speech Encoding and Encryption in VLSI <i>KalyanChakravarti Kongara, Srinivas B. Mandalika</i>	569
6D-7	The Design of a i8080A Instruction Compatible Processor with Extended Memory Address <i>Chiaki Kon, Naohiko Shimizu</i>	571
6D-8	The Design of a USB Device Controller IYOYOYO <i>Tomoaki Kouyama, Hibiki Nano, Chiaki Kon, Naohiko Shimizu</i>	573
6D-9	MAPLE Chip: a Processing Element for a Static Scheduling Centric Multiprocessor <i>Kenta Yasufuku, Riku Ogawa, Keisuke Iwai, Hideharu Amano</i>	575
6D-10	Finding the Best System Design Flow for a High-Speed JPEG Encoder <i>Kazuo Sakiyama, Patrick Schaumont, Ingrid Verbauwhede</i>	577
6D-11	The Design of PCI Bus Interface <i>Haruyasu Hayasaka, Hiroaki Haramiishi, Naohiko Shimizu</i>	579
6D-12	Low-Power Digital CDMA Receiver <i>I Hsin Chen, Ja Sheng Liu, Yi Chen Tsai</i>	581
6D-13	Hardware Implementation of an EAN-13 Bar Code Decoder <i>Jeroen De Maeyer, Harald Devos, Wim Meeus, Peter Verplaetse, Dirk Stroobandt</i>	583
6D-14	Error Correction Receiver Using Difference-set Cyclic Code <i>Yukihiro Kato, Tomokazu Morita</i>	585
6D-15	Design of Digital CDMA Receiver <i>Vijay Kumar Immadi, Srinivas B. Mandalika</i>	587
6D-16	Standard Cell Libraries with Various Driving Strength Cells for 0.13, 0.18 and 0.35μm Technologies <i>Masanori Hashimoto, Kazunori Fujimori, Hidetoshi Onodera</i>	589
6D-17	A Nearest-Hamming-Distance Search Memory with Fully Parallel Mixed Digital-Analog Match Circuitry <i>Tetsushi Koide, Hans Juergen Mattausch, Yuji Yano, Takayuki Gyohten, Yoshihiro Soda</i> ..	591

Session 7A
System-Level Power Issues

Co-Chairs: Kazutoshi Kobayashi, Massoud Pedram

7A-1	Run-Time Energy Estimation in System-On-a-Chip Designs <i>Josef Haid, Gerald Kaefer, Christian Steger, Reinhold Weiss</i>	595
7A-2	SEA: Fast Power Estimation for Micro-Architectures <i>Praveen G. N. Kalla, Joerg Henkel, Xiaobo (sharon) Hu</i>	600
7A-3s	HyPE: Hybrid Power Estimation for IP-Based Programmable Systems <i>Xun Liu, Marios C. Papaefthymiou</i>	606
7A-4s	An Efficient IP-Level Power Model for Complex Digital Circuits <i>Chih-Yang Hsu, Chien-Nan Jimmy Liu, Jing-Yang Jou</i>	610
7A-5	A Hierarchical Analysis Methodology for Chip-Level Power Delivery with Realizable Model Reduction <i>Yu-Min Lee, Charlie Chung-Ping Chen</i>	614

Session 7B
(Special Session) Invited Talks: Design Methodologies for 50M Gate ASICs

Co-Chairs: Jason Cong, Satoshi Matsushita

7B-1	Optimality and Scalability Study of Existing Placement Algorithms <i>Chin-Chih Chang, Jason Cong, Min Xie</i>	621
7B-2	IBM's 50 Million Gate ASICs <i>Juergen Koehl, David E. Lackey</i>	628
7B-3	Silicon Virtual Prototyping: The New Cockpit for Nanometer Chip Design <i>Wei-Jin Dai, Dennis Huang, Chin-Chih Chang, Michel Courtoy</i>	635
7B-4	Design Flow and Methodology for 50M Gate ASIC <i>Yatin Trivedi</i>	640

Session 7C
(Special Session) Invited Talks: Mixed Signal Test

Co-Chairs: Kwang-Ting Cheng, Yasuo Sato

7C-1	Efficient Loop-back Testing of On-chip ADCs and DACs <i>Hak-Soo Yu, Jacob A. Abraham, Sungbae Hwang, Jeongjin Roh</i>	651
7C-2	A Novel LCD Driver Testing Technique Using Logic Test Channel <i>Chauchin Su, Wei-Juo Wang, Chih-Hu Wang</i>	657
7C-3	An Implementation of Memory-based On-chip Analogue Test Signal Generation <i>Salvador Mir, L. Rolíndez, C. Domingues, L. Rufer</i>	663

7C-4	Delta-sigma Modulator Based Mixed-signal BIST Architecture for SoC <i>Chee-Kian Ong, Kwang-Ting Cheng, Li Wang</i>	669
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<p>Session 7D</p> <p>Embedded Systems: Hardware/ Software Design Methodology and Optimization</p>

Co-Chairs: Naehyuck Chang, Hiroaki Takada

7D-1	Capturing and Analyzing Requirement- In Case of Software and Applying to Hardware - <i>Akira Kawaguchi</i>	677
7D-2	A Comparison of the RTU Hardware RTOS with a Hardware/Software RTOS <i>Jaehwan Lee, Vincent John Mooney III, Anders Daleby, Karl Ingstrom, Tommy Klevin, Lennart Lindh</i>	683
7D-3s	Linux Kernel Customization for Embedded Systems by Using Call Graph Approach <i>Che-Tai Lee, Zeng-Wei Hong, Jim-Min Lin</i>	689
7D-4s	Topology Selection for Energy Minimization in Embedded Networks <i>Dexin Li, Pai H. Chou, Nader Bagherzadeh</i>	693

<p>Session 8A</p> <p>Design Validation Techniques</p>

Co-Chairs: Vasily Moshnyaga, Hiroyuki Ochi

8A-1	Semi-Formal Test Generation and Resolving a Temporal Abstraction Problem in Practice: Industrial Application <i>Julia Dushina, Mike Benjamin, Daniel Geist</i>	699
8A-2	Scan-chain Based Watch-points for Efficient Run-Time Debugging and Verification of FPGA Designs <i>Anurag Tiwari, Karen A. Tomko</i>	705
8A-3s	A Novel Approach for Digital Waveform Compression <i>Edwin Naroska, Shang-Jang Ruan, Chia-Lin Ho, Said Mchaalia, Feipei Lai, Uwe Schwiegelshohn</i>	712
8A-4s	A Deep Submicron Power Estimation Methodology Adaptable to Variations between Power Characterization and Estimation <i>Daniel Eckerbert, Per Larsson-Edefors</i>	716

<p>Session 8B</p> <p>Placement</p>
--

Co-Chairs: Masaaki Yamada, Xin Yuan

8B-1	Congestion Driven Incremental Placement Algorithm for Standard Cell Layout <i>Zhuoyuan Li, Weimin Wu, Xianlong Hong</i>	723
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8B-2	Performance-Driven Multi-Level Clustering for Combinational Circuits <i>C. N. Sze, Ting-Chi Wang</i>	729
8B-3	Cross Talk Driven Placement <i>Jinan Lou, Wei Chen</i>	735
8B-4s	VLSI Module Placement with Pre-placed Modules and Considering Congestion Using Solution Space Smoothing <i>Sheqin Dong, Xianlong Hong, Xin Qi, Ruijie Wang, Song Chen, Jun Gu</i>	741
8B-5s	A Path-based Timing-driven Quadratic Placement Algorithm <i>Wenting Hou, Xianlong Hong, Weimin Wu, Yici Cai</i>	745

<p>Session 8C Test Issues for Deep Sub-Micron Design</p>
--

Co-Chairs: Tomoo Inoue, Rochit Rajsuman

8C-1	Experience in Critical Path Selection for Deep Sub-Micron Delay Test and Timing Validation <i>Jing-Jia Liu, Li-C. Wang, Angela Krstic, Kwang-Ting (tim) Cheng</i>	751
8C-2	On Effective Criterion of Path Selection for Delay Testing <i>Masayasu Fukunaga, Seiji Kajihara, Sadami Takeoka, Shinichi Yoshimura</i>	757
8C-3	DFT Timing Design Methodology for At-Speed BIST <i>Yasuo Sato, Motoyuki Sato, Koki Tsutsumida, Masatoshi Kawashima, Kazumi Hatayama, Kazuyuki Nomoto</i>	763
8C-4	An Automated Method for Test Model Generation from Switch Level Circuits <i>Tim McDougall, Atanas N Parashkevov, Simon Jolly, Juhong Zhu, Jing Zeng, Magdy Abadir, Carol Pyron</i>	769

<p>Session 8D Analog Circuits Design and Methodology</p>
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Co-Chairs: Yu-Chung Hung, Makoto Nagata

8D-1	Using Red-Black Interval Trees in Device-Level Analog Placement with Symmetry Constraints <i>Florin Balasa, Sarat C. Maruvada, Karthik Krishnamoorthy</i>	777
8D-2	Current-Driven Wire Planning for Electromigration Avoidance in Analog Circuits <i>Jens Lienig, Goeran Jerke</i>	783
8D-3	Efficient DDD-based Term Generation Algorithm for Analog Circuit Behavioral Modeling <i>Sheldon X. -D. Tan, C. -J. Richard Shi</i>	789
8D-4	5Gbps Serial Link Transmitter with Pre-emphasis <i>Chih-Hsien Lin, Chun-Hong Wang, Shyh-Jye Jou</i>	795

Session 9A
Synthesis for Power Performance Optimization

Co-Chairs: Yutaka Tamiya, Li-C. Wang

9A-1	Low Power Synthesis of Finite State Machines with Mixed D and T Flip-Flops <i>Ali Iranli, Peyman Rezvani, Massoud Pedram</i>	803
9A-2	Don't Cares in Logic Minimization of Extended Finite State Machines <i>Yunjian Jiang, Robert K. Brayton</i>	809
9A-3s	Performance Optimization of Synchronous Control Units for Datapaths with Variable Delay Arithmetic Units <i>Euiseok Kim, Hiroshi Saito, Jeong-Gun Lee, Dong-Ik Lee, Hiroshi Nakamura, Takashi Nanya</i>	816
9A-4s	Integer Linear Programming-Based Synthesis of Skewed Logic Circuits <i>Aiqun Cao, Naran Sirisantana, Cheng-Kok Koh, Kaushik Roy</i>	820

Session 9B
Routing

Co-Chairs: Xinlong Hong, Yoichi Shiraiashi

9B-1	Highly Scalable Algorithms for Rectilinear and Octilinear Steiner Trees <i>Andrew B. Kahng, Ion Mandoiu, Alexander Zelikovsky</i>	827
9B-2	UTACO: A Unified Timing and Congestion Optimizing Algorithm for Standard Cell Global Routing <i>Tong Jing, Xianlong Hong, Haiyun Bao, Yici Cai, Jingyu Xu, Chungkuan Cheng, Jun Gu</i>	834
9B-3	The Y-Architecture: Yet Another On-Chip Interconnect Solution <i>Hongyu Chen, Feng Zhou, Chung-Kuan Cheng</i>	840
9B-4s	A Novel Timing-Driven Global Routing Algorithm Considering Coupling Effects for High Performance Circuit Design <i>Jingyu Xu, Xianlong Hong, Tong Jing, Yici Cai, Jun Gu</i>	847
9B-5s	Graph Matching-Based Algorithms for Array-Based FPGA Segmentation Design and Routing <i>Jai-Ming Lin, Song-Ra Pan, Yao-Wen Chang</i>	851

Session 9C
DFT Optimizations

Co-Chairs: Alfred Crouch, Hiroshi Date

9C-1	Routing-Aware Scan Chain Ordering <i>Puneet Gupta, Stefanus Mantik, Andrew B. Kahng</i>	857
9C-2	Multiple Test Set Generation Method for LFSR-Based BIST <i>YouHua Shi, Zhe Zhang</i>	863

9C-3	A Seed Selection Procedure for LFSR-Based Random Pattern Generators <i>Kenichi Ichino, Kohichi Watanabe, Masayuki Arai, Satoshi Fukumoto, Kazuhiko Iwasaki</i>	869
9C-4s	Efficient BIST Design for Sequential Machines Using FiF-FoF Values in Machines States <i>Roy S, Maulik U, Bandyopadhyay S, Basu S, Sikdar K Biplab</i>	875
9C-5s	A New Design-for-Test Technique for Reducing SOC Test Time <i>C V Guru Rao, D Roy Chowdhury</i>	879

Session 9D
RF Circuits Design and Methodology

Co-Chairs: Wing-Hung Ki, Tsuneo Tsukahara

9D-1	Periodic Steady-State Analysis of Coupled ODE-AE-CGE Systems for MOS RF Autonomous Circuit Simulation <i>Xinyu Wu, Zaiman Chen, Jinmei Lai, Qianling Zhang, Omar Wing, Junyan Ren</i>	885
9D-2	A Frequency Separation Macromodel for System-Level Simulation of RF Circuits <i>Xin Li, Peng Li, Yang Xu, Robert Dimaggio, Lawrence Pileggi</i>	891
9D-3	Nonlinear Distortion Analysis via Linear-Centric Models <i>Peng Li, Lawrence T. Pileggi</i>	897
9D-4	Parasitic-Aware Design and Optimization of a Fully Integrated CMOS Wideband Amplifier <i>Jinho Park, David J. Allstot</i>	904
Author Index		909