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ASP-DAC 2003 Best Paper Award Candidates

1D-1 **SAT-based Sequential Depth Computation**
M. Mneimneh, K. Sakallah – *University of Michigan, USA*

2B-1 **Approximate Formulae Approach for Efficient Inductance Extraction**
A. Kurokawa – *Semiconductor Technology Academic Research Center, Japan,* ***T. Sato*** – *Hitachi Ltd., Japan,* ***H. Masuda*** – *Semiconductor Technology Academic Research Center, Japan*

3A-2 **Towards On-Chip Fault-Tolerant Communication**
T. Dumitras, S. Kerner, R. Marculescu – *Carnegie Mellon University, USA*

3C-1 **Statistical Delay Computation Considering Spatial Correlations**
A. B. Agarwal, D. Blaauw – *University of Michigan, USA,* ***S. Sundareswaran, V. Zolotov, M. Zhao, K. Gala, R. Panda*** – *Motorola,USA*

4C-1 **Efficient LUT-Based FPGA Technology Mapping for Power Minimization**
H. Li, W.-K. Mak, S. Katkoori – *University of South Florida, USA*

5A-1 **Fast Buffer Planning and Congestion Optimization in Interconnect-driven Floorplanning**
K. W. C. Wong, E. F.Y. Young – *The Chinese University of Hong Kong, Hong Kong*

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Z. Li, W. Wu, X. Hong – *Tsinghua University, China*

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