A New Design Approach for RSFQ Logic Circuits Based on the Binary Decision Diagram

Nobuyuki Yoshikawa, Hiroshi Tago and Kaoru Yoneyama
Faculty of Engineering, Yokohama National University, 79-5 Tokiwadai, Hodogaya, Yokohama 240, Japan

Abstract—We will propose a new design approach for single-flux-quantum (SFQ) logic circuits based on a binary decision diagram (BDD). The BDD is a way to represent a logical function by using a directed graph, which is composed of nodes having one input (root) and two outputs (branches). The node has binary states internally which can be controlled from outside, and it switches a messenger entering from the root into one of two branches depending on the internal state. It has been proven that any combinational logic can be represented by this basic element. We will show that the BDD is effectively implemented by an SFQ circuit, where the node is replaced with an SFQ D_2 flip-flop. Important features of the BDD SFQ logic circuit are simplicity of circuit structure, self-timed nature and high modularity. We have designed a BDD SFQ adder and showed that the junction count and latency are smaller than that of the conventional RSFQ adder.

I. Introduction

Representation of logical functions using a binary decision diagram (BDD) has been developed actively in the field of VLSI design and computer algorithm, because it reduces the computational cost in terms of speed and memory size when the logical functions are processed on a computer [1], [2]. The idea of implementing digital circuits by replacing the BDD directly with real devices has been proposed by Asahi et al. [3], [4], and has mainly been investigated for application to single electron devices.

Rapid single flux quantum (RSFQ) logic circuits [5], where logical "1" and "0" are represented by the existence or absence of a single flux quantum (SFQ), have been developed extensively in the world because of their potentially high performance with clock frequency beyond hundreds of gigahertz and extremely low power consumption. However, because RSFQ logic circuits inherently need SFQ clock signals to all gates to reset them, precise timing is very hard when the operating frequency exceeds tens of gigahertz. In addition, the RSFQ logic circuits use Josephson transmission lines (JTL) for distributing the clock signals and for wiring gates, complicating the design of the logic circuits.

In this paper, we will show that the circuit structure can be simplified if we use the BDD representation to design RSFQ logic circuits. This design approach eliminates the need for a synchronous clock, and also brings about high modularity of the circuits, resulting in high efficiency of the circuit design.

Manuscript received September 15, 1998.

II. Representation of Logic Functions by Binary Decision Diagram

It is an important subject in designing VLSI circuits to investigate how to represent the logical functions and process them efficiently on a computer. Usually the Boolean equation and the truth table have been used to represent digital functions; the BDD is another approach. The logical function can be accomplished by the BDD with small memory size and small calculation steps compared with the usual method.

The binary decision diagram is a way to represent the logical functions by using a directed graph as shown in Fig. 1. The basic element of the BDD is a node having one input terminal (root) and two output terminals (branch0 and branch1). Each node has internal states "0" or "1" and points to one of the branches depending on the internal state, say branch0 for the "0" state and branch1 for the "1" state. For example, when one traces from the top of the graph in Fig.1, if the state of the node x_1 is "1" one will move to node "x_2", and if "0" one will move to node "x_3". Continuing this procedure, one reaches the end of the graph which is labeled by "0" and "1". This value corresponds to the solution of the logic operation. Figure 1 is an example of the representation of the logic operation $f = x_1 \cdot x_2 + \bar{x}_3$ by the BDD. It is known that any logic function can be represented by the BDD.

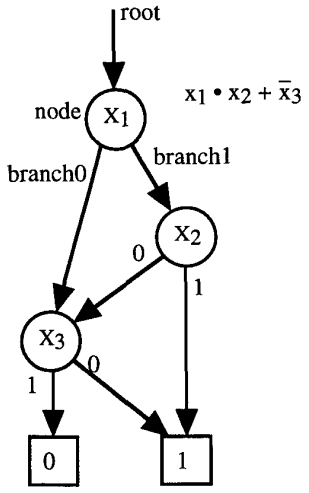

Fig. 1 The binary decision diagram (BDD). The figure shows an example of the logical function $x_1 \cdot x_2 + \bar{x}_3$.

III. Design of RSFQ Logic Circuits by the Binary Decision Diagram

In order to design digital circuits based on the BDD representation, we must find the basic element which operates as the node in the BDD. This element has to switch the messenger, the particle representing the state of the system, from the root into one of the branches depending on its internal state [3]. Because the SFQ pulse can be used as the messenger, the BDD basic element can be effectively implemented by superconducting circuits.

One way is to use a D_2 flip-flop [6] as shown in Fig. 2. In this case, the root and the two branches in the BDD element correspond to the "Clock" and the complementary outputs, "Out" and "$\overline{\text{Out}}$" in the D_2 flip-flop, respectively. The internal state of the basic element can be changed by an input of an SFQ pulse into the complementary input, "Data" and "$\overline{\text{Data}}$". The input of an SFQ pulse into "Data" ("$\overline{\text{Data}}$") changes the state of the flip-flop into the "1" ("0") state, regardless of the previous state. When an SFQ pulse is applied to the "Clock", an SFQ is outputted at "Out" ("$\overline{\text{Out}}$") if the state of the flip-flop is "1" ("0"). After the output of the SFQ pulse the state is reset to "0". Note that the BDD basic element can also be implemented by using B flop-flops [7].

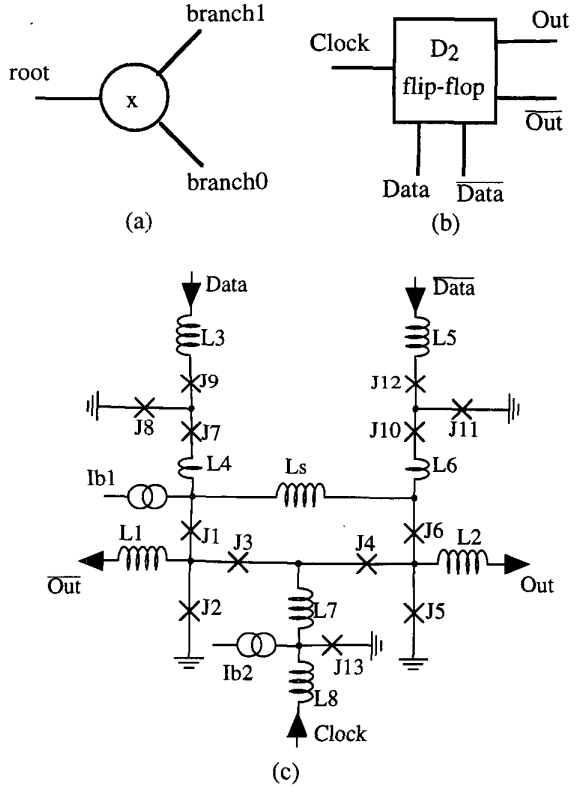

Fig. 2 Implementation of a BDD basic element by a D_2 flip-flop. (a) The basic element of the BDD. (b) Its implementation using the D_2 flip-flop. (c) A circuit diagram of the D_2 flip-flop. Designed junction critical current are: J_1 = 150 μA, J_2, J_{11} = 180 μA, J_3, J_6, J_{13} = 310 μA, J_4 = 250 μA, J_5 = 370 μA, J_7, J_8 = 190 μA, J_9 = 220 μA, J_{10} = 140 μA, J_{12} = 240 μA. Designed inductances are: L_s, L_2 = 3.5 pH, L_1 = 4.1 pH, L_3, L_6 = 3.4 pH, L_4, L_8 = 2.8 pH, L_5 = 3.7 pH, L_7 = 1.0 pH. Designed bias currents are: I_1 = 248 μA, I_2 = 275 μA.

Figure 3 shows an example of the implementation of the logic gates (AND, OR, XOR) by the BDD representation. These BDD gates have the following advantages over the conventional RSFQ logic gates.

(i) Any combinational logic function can be performed by a series of identical basic elements, such as the D_2 flip-flop.

(ii) The gates are dual rail, and they are data-driven self-timed [8], [9]. Distribution of clock signals to the gate is not necessary in this case.

(iii) The internal state is determined by the propagation of the messenger. The only requirement for the timing is that the messenger had to arrive to each gate after the transition caused by input data.

(iv) Since complex logic circuits can be implemented by regular arrays of BDD basic elements, the modularity of the circuits is very large, which simplifies layout design.

It should be noted here that if the complementary inputs ("x_0", "$\bar{x}_0$") to the first stage of the D_2 flip-flop are directly applied to the root of the next stage, the flip-flop at the first stage is eliminated as shown in Fig. 4.

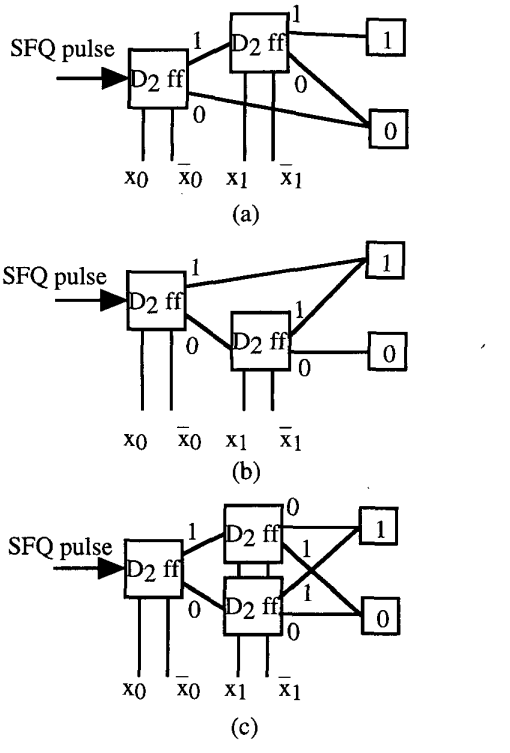

Fig. 3 The implementation the logic gates using the BDD representations. (a) AND, (b) OR, (c) XOR.

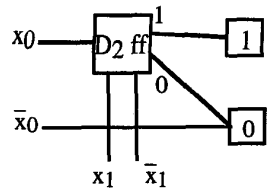

Fig. 4 The simplified version of the BDD SFQ AND gate.

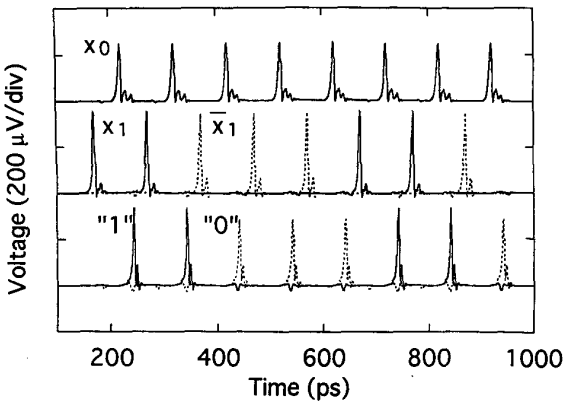

Fig. 5 Simulation results of the BDD SFQ AND gate for the input data patterns of x_0 = (1111 1111) and x_1 = (1100 0110).

Figure 5 shows simulation results for the BDD SFQ AND gate shown in Fig. 4 assuming the Nb Josephson process with critical current density of 1 kA/cm^2. An output data pattern of (1100 0110) is obtained for the input of x_0 = (1111 1111) and x_1 = (1100 0110), where the throughput of the input data is more than 10 Gb/s and the latency is about 23 ps. The simulated dc global bias margin is ±30%.

The BDD SFQ AND gate was fabricated using the standard HYPRES Nb Josephson technology. Figure 6 shows the test results of the BDD SFQ AND gate at low frequency (1 kHz) with input data patterns x_0 = (1111 1111) and x_1 = (1100 0110). One can see that correct operation is observed with output data patterns of (1100 0110) in Output "1" and (0011 1001) in Output "0". The measured dc bias margin of this circuit is ±9.5%. The discrepancy between the simulated margin and the test margin is thought to arise from local circuit parameter variations as well as uncertainty of the values of parasitic inductance in our layout design.

IV. Design of a BDD SFQ Adder

In order to investigate the validity of this design approach, we have designed a BDD SFQ adder and compared its performance with that of the conventional RSFQ adder.

Figure 7 shows a 1-bit half adder and 1-bit full adder

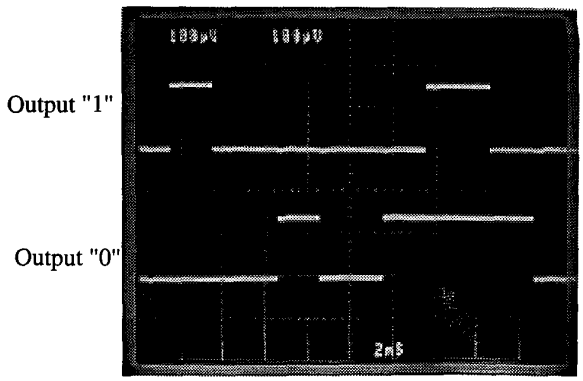

Fig. 6 Test results of the BDD SFQ AND gate at low frequency (1 kHz) with input data patterns x_0 = (1111 1111) and x_1 = (1100 0110). Each transition corresponds to an output of one SFQ.

design based on the BDD representation, where (a, $\bar{a}$) and (b, $\bar{b}$) are the adder input, (c_i, $\bar{c}_i$) is the carry input, (c_o, $\bar{c}_o$) is the carry output, and (s, $\bar{s}$) is the sum output. In these design, further simplification was carried out by common use of partial BDD graphs, where two BDD graphs to derive the sum and the carry are combined together to reduce the node number, or the number of the D_2 flip-flop.

Figure 8 shows simulation results for the 1-bit BDD SFQ full adder with input data patterns a = (1111), b = (0101) and c = (0011). From the simulation, the propagation delay of the carry is estimated to be 120 ps and the dc-bias margin is -20% ~ +30% at 10 Gb/s. In TABLE I, we compare the performance of the BDD SFQ adder with the conventional RSFQ adder [10], [11], assuming the standard 1 kA/cm^2 Nb process. The BDD SFQ adder has a lower junction count and a smaller latency than the conventional RSFQ adder. In the table we should compare the performance of the BDD SFQ adder with that of DDST RSFQ adder for impartial comparison, since they are both dual-rail circuits. Note that the conventional RSFQ adder in TABLE I is designed in straightforward way using RSFQ AND and XOR gates. A novel RSFQ adder having a lower junction count has been implemented based on an efficient circuit design at the gate level [12].

The main problem with the BDD design approach is that through put of the system will be low if system become large, since pipelining is difficult in this design approach.

V. Conclusion

We have proposed a new design approach for RSFQ circuits based on the binary decision diagram and investigated its validity. Comparison of the BDD SFQ adder with the conventional RSFQ adder indicates that the BDD SFQ adder has a lower junction count and a smaller latency.

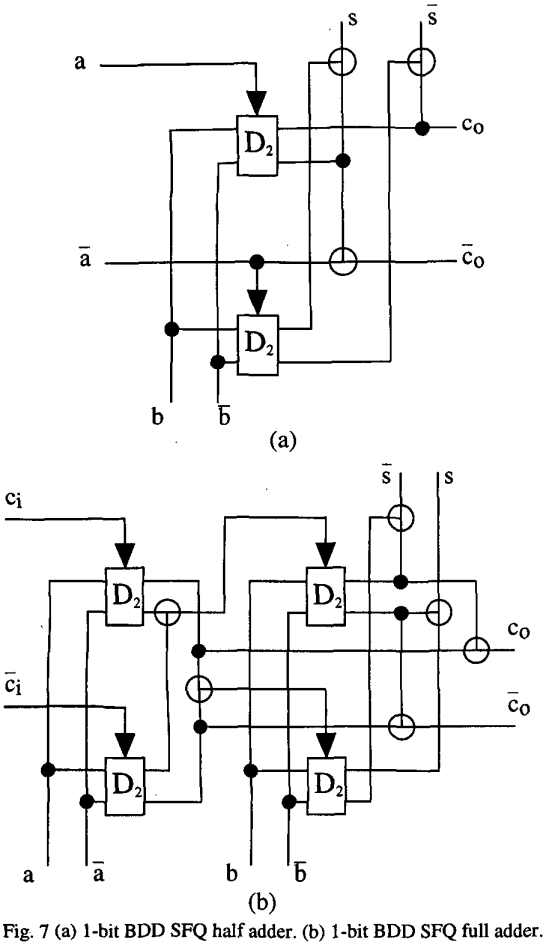

Fig. 7 (a) 1-bit BDD SFQ half adder. (b) 1-bit BDD SFQ full adder.

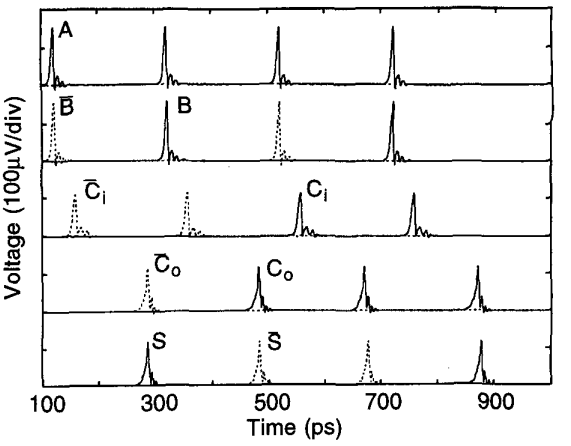

Fig. 8 Simulation results of the 1-bit BDD SFQ full adder.

TABLE I
COMPARISON OF PERFORMANCE OF THE BDD SFQ ADDER AND THE CONVENTIONAL RSFQ ADDER, ASSUMING THE 1 kA/cm^2 Nb PROCESS.

	Number of Junction	Latency of Carry Bit	DC Bias Margin
1-bit BDD SFQ Full Adder	116	120 ps	- 20~30%
1-bit Conventional RSFQ Full Adder [11]	122	165 ps	- 20~30%
1-bit DDST RSFQ Full Adder [11]	168	250 ps	- 20~30%

ACKNOWLEDGEMENT

The authors would like to thank Prof. T. Van Duzer for helpful discussion.

REFERENCES

[1] S. B. Akers, "Binary decision diagrams", IEEE Trans. Comput., vol. C-27, pp. 509-516, 1978.
[2] R. E. Bryant "Graph-based algorithms for Boolean function manipulation," IEEE Trans. Comput., vol. C-35, pp. 677-691, 1986.
[3] N. Asahi, M. Akazawa and Y. Amemiya, "Binary-decision-diagram device", IEEE Trans. Electron Devices, vol 42, pp.1999-2003, November, 1995.
[4] N. Asahi, M. Akazawa and Y. Amemiya, "Single-electron logic device based on the binary-decision-diagram", IEEE Trans. Electron Devices, vol 44, pp.1109-1116, July, 1997.
[5] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz-clock frequency digital systems," IEEE Trans. Appl. Superconductivity, vol. 1, pp. 1-28, March, 1991.
[6] N. Yoshikawa, Z. J. Deng, S. R. Whiteley and T. Van Duzer, "Design and testing of data-driven self-timed RSFQ demultiplexer", Extended Abstract of ISEC'97, Berlin, Germany, June, pp. 353-355, 1997.
[7] S. V. Polonsky, V. K. Semenov and A. F. Kirichenko, "Single flux quantum B flip-flop and its possible applications", IEEE Trans. Appl. Superconductivity, vol. 4, pp. 9-18, March, 1994.
[8] Z. J. Deng, N. Yoshikawa, S. R. Whiteley and T. Van Duzer, "Data-driven self-timed RSFQ digital integrated circuit and system," IEEE Trans. on Applied Superconductivity, Vol. 7, pp.3634-3637, June, 1997.
[9] M. Maezawa, I. Kurosawa, M. Aoyagi, H. Nakagawa, Y. Kameda and T. Nanya, "Rapid single-flux-quantum dual-rail logic for asynchronous circuits," IEEE Trans. Appl. Superconductivity, vol. 7, pp. 3634-3637, June, 1997.
[10] C. A. Hamilton and K. C. Gilbert, "Margin and yield in single flux quantum logic", IEEE Trans. Appl. Superconductivity, vol. 1, pp.157-163, December, 1991.
[11] N. Yoshikawa, H. Tago and K. Yoneyama, "Design considerations of data-driven self-timed RSFQ adder circuits", to be published in IEICE Trans. Electron., vol. E81-C, pp. 1618 - 1626, October, 1998.
[12] A. F. Kirichenko and O. A. Mukhanov, "Implementation of novel "push-forward" RSFQ carry-save adders", IEEE Trans. Appl. Superconductivity, vol. 5, pp.3010-3013, June, 1995.