FPGA-based applications for software radio

Software radio technology offers the ability to develop radio architectures with programmable intermediate frequency, bandwidth, modulation and coding schemes. Field-programmable gate array is important in multimission software radio applications like electronic warfare, radar, communications and RF testing.

By Angsuman Rudra

Software radio technology has gained momentum as engineers everywhere are developing radio architectures that include minimal hardwired analog components. The ability to program intermediate frequency (IF), bandwidth, modulation, coding schemes and other radio functions is the appeal for such widespread interest. Besides providing all these flexibilities, software radio must improve on performance in terms of sensitivity, dynamic range and adjacent-channel rejection. Software radio is still a radio and must perform better than the conventional radio it is replacing.

Current advances in field-programmable gate array (FPGA) technology have enabled high-speed processing in a compact footprint, while retaining the flexibility and programmability of software radio technology. FPGAs are popular for high-speed, compute-intensive, reconfigurable applications (fast Fourier transform (FFT), finite impulse response (FIR) and other multiply-accumulate operations). Reconfigurable cores are available from FPGA and board vendors and enable implementation of modulator, demodulator and CODEC functionality in the FPGA. System designers are increasingly looking for front-end acquisition/converter products with integrated FPGA to offload the baseband processing and reduce data transfer rates.

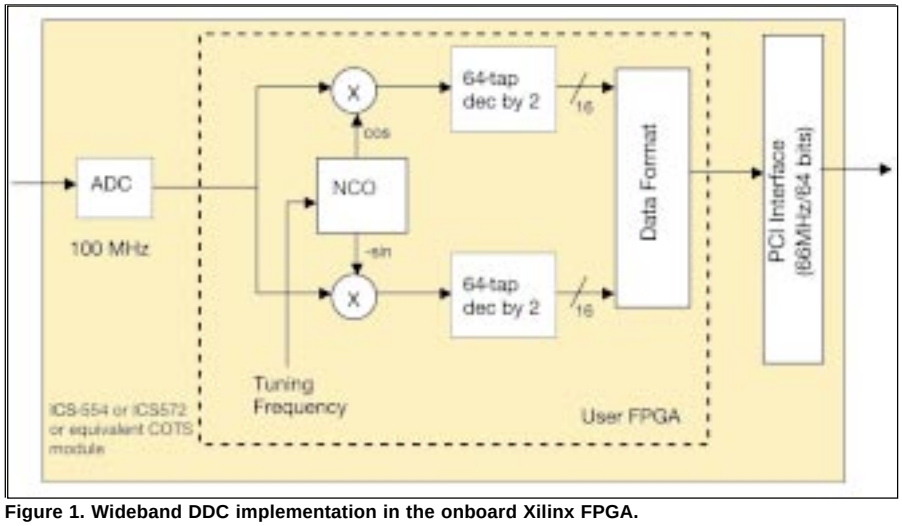

Figure 1. Wideband DDC implementation in the onboard Xilinx FPGA.

Although there has been a huge improvement of the application development tools, FPGA design should be considered as hardware (albeit flexible) development, and it requires a different skill set than software development.

This aspect of FPGA design implies that implementing a predesigned core on a commercial off-the-shelf (COTS) front-end data acquisition/converter module is not a simple software development exercise. This needs to be considered during project planning stage to reduce delays down the road.

FPGA is important in multimission software radio applications like electronic warfare (EW), radar, communications and RF testing.

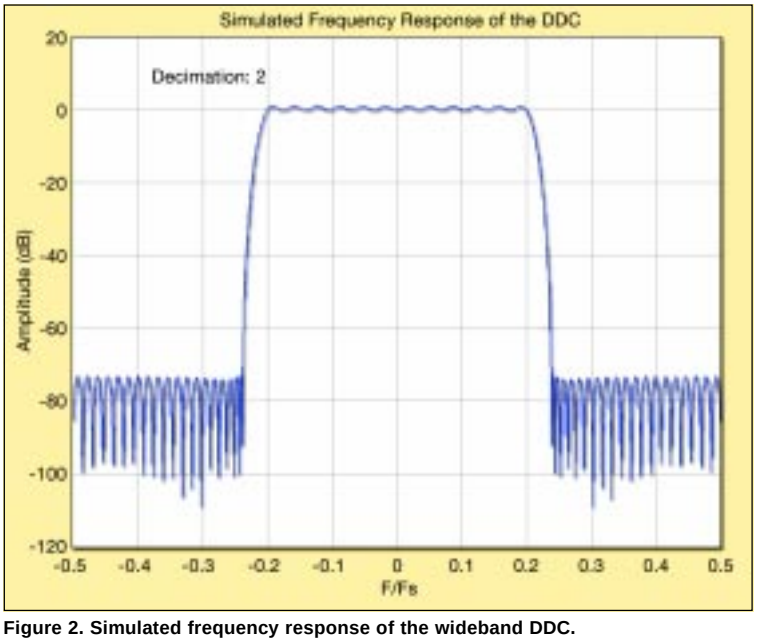

Figure 2. Simulated frequency response of the wideband DDC.

FPGA or DSP?

FPGAs have evolved from being flexible logic design platforms to signal processing engines. They are now an essential component of software radio due to their flexibility and real-time processing capabilities. Increasingly, system designers are porting more and more signal processing functionalities in FPGAs. The flexibility of having the ability to integrate logic design with signal processing is pushing designers to replace traditional digital signal processors (DSPs) with FPGAs.

FPGAs are inherently suited for high-speed parallel multiply and accumulate functions. Current generation FPGAs can perform 18 x 18 multiplication operation at speeds in excess of 200 MHz. This makes FPGAs an ideal platform for operations such as FFT, FIR, digital downconverters (DDC), digital upconverters (DUC), correlators and pulse compression (for radar processing).

It does not imply, however, that all DSP functionalities may be implemented in FPGAs. Floating point operations are difficult to implement in FPGAs due to the large amount of real estate needed in the device. Also, processing involving matrix inversion (or division) is also more suited to a DSP/GPP platform. FPGAs and DSP will thus coexist for a long time, and a flexible platform will include a mix of both.

FPGA design

FPGA design is inherently a hardware design effort and not simply a DSP coding exercise. Progress in the field of electronic design automation (EDA) tools has ensured that better and more accurate design and simulation software is on the market. The FPGA vendors (Xilinx and Altera being the two largest) have also been instrumental in driving the tool development, thereby improving the ease of FPGA design.

The hardware nature of FPGA design sometimes leads to unplanned project delays as the right engineering resources are not budgeted for the task. Starting from a prepackaged FPGA IP core to a functional hardware with the integrated functionality is a step that needs to be planned carefully.

FPGA IP cores

With the popularity of FPGAs, there has been an increase of intellectual property (IP) cores available from the FPGA vendors and other third-party core developers. These cores offer a variety of DSP functionalities. However, these need to be integrated in actual hardware. As noted earlier, integrating these cores in COTS modules requires time and hardware design expertise. ICS provides FPGA cores that are fully tested and integrated with high-performance data acquisition and converter COTS modules. The modules provide smart front-end products, thereby reducing system design and integration risks.

Wideband digital downconverter

Digital downconverter (DDC) is an essential component of any software radio-based system. DDCs have fundamentally altered conventional radio design. For a discussion on conventional radio design and software radio-based implementation please see the July 2003 issue of *RF Design*. DDCs enable simplification of RF front-end design, including LO and mixer design, as the downconversion process is performed in digital domain. Digital filters following the digital mixers provide a much sharper filtering than traditional analog filtering. These filters are usually decimating in nature, thereby reducing the output data rate.

A variety of dedicated DDCs are available, TI-Graychip and Intersil being the two most popular ones. These DDCs offer programmable bandwidth (or decimation) and tuning frequency. However, they are usually targeted for narrower band applications.

There is increasing demand for higher bandwidth, and system designers are trying to design wideband systems with bandwidths up to 40 MHz. These include radar, GPS, telemetry, and wideband communications, etc. For larger bandwidths, the DDCs need to be implemented in a FPGA following the analog-to-digital converter (ADC). A typical decimate by 2 DDC implemented by ICS is shown in Figure 1. This decimate by 2 DDC offers a maximum flat-top bandwidth of -0.2*Fs to +0.2*Fs when sampled with a 100

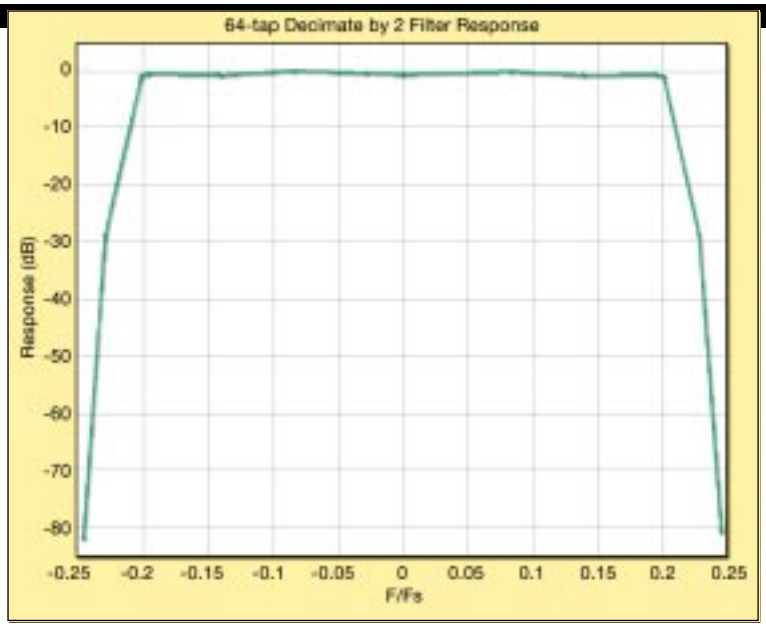

Figure 3. In-system performance of the ICS 64-tap decimate by 2 DDC implemented in the ICS-554.

MHz ADC (about 80 percent of the complex output rate). With a 100 MHz sampling clock, this translates to a flat-top bandwidth of 40 MHz and 200 MBps per channel data rate. The DDC offers stop-band rejection in excess of 70 dB (Figure 2). The filter may be configured for narrower bandwidths providing a 2x or 4x oversampling factor if desired.

The programmability of the filter is an important aspect of software radio implementation. This allows for on-the-fly bandwidth selection, a major advantage over conventional analog only systems.

ICS designers have implemented a decimate by 4 DDC with flat-top bandwidth of –0.1*Fs to +0.1*Fs. With a sampling rate of 100 MHz, this offers a flat-top bandwidth of 20 MHz.

Figure 3 shows the frequency characteristics of the decimate by 2 wideband DDC implemented on the ICS-554. This is actual measured data as opposed to simulation plots.

Figure 4 shows the spectrum of the downconverted signal at band edge.

A single 64-tap decimate by 2 DDC is supported on a 1 million gate Virtex II FPGA and thus is easily integrated in the ICS-554B with this FPGA. ICS has also delivered complex systems with multiple wideband DDCs on the ICS-554C with 3 m gate user FPGA.

When integrating these high-speed DDCs, sufficient care has to be taken to ensure that data transfer is not interrupted. For multichannel systems, this implies that dedicated data buses need to be used. The industry-standard PMC module offers the ability of moving high-speed data directly over the Pn4 user I/O connector bypassing the PCI bus (See High-speed data transfer over Pn4 PMC User I/O below).

The same concepts discussed here hold equally well for the transmit direction. For the transmitter, the digital down-converters are replaced with digital upconverters (DUC). The DUCs use digital interpolating filters and provide the same advantages.

Real-time spectrum monitoring and detection

Real-time spectrum monitoring and detection is another area where FPGAs and software radio-based technology can be conveniently used.

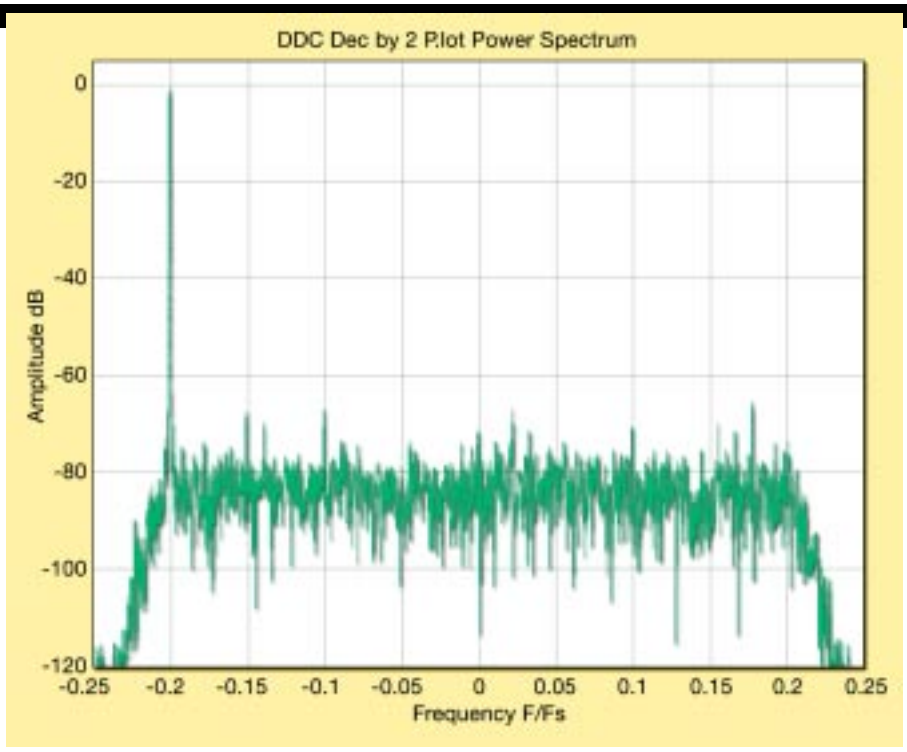

Figure 4. Power spectrum of the downconverted signal at band edge.

Other than the obvious use in signal intelligence (SIGINT) and EW scenarios, this functionality has widespread use in RF testing and spectrum analysis applications.

A COTS module like the ICS-554 with high-speed ADC and large user FPGA is an ideal platform for a real time spectrum monitoring and detection system. The large-user FPGA is ideally suited for implementing a real-time power spectral estimator (FFT, magnitude computation and spectral averaging). After thresholding and detection, the onboard narrowband digital tuners may be used as drop-down receivers to tune to the channels of interest. The integrated IP cores integrated ensure that such a complex system is available on a single industry-standard PMC card.

ICS has integrated an 8 K real-time FFT engine with power detection and spectral averaging as shown in Figure 5.

Figure 6 shows the in-system performance of the FFT-based power spectral estimator.

Figure 7 shows the in-system response with averaging turned on. As expected, spectral averaging reduces uncorrelated noise and improves dynamic range. Spectral averaging also has the advantage of reducing the data throughput rate, enabling multiple boards to share the same system bus.

The 8 K FFT engine with power detection and programmable averaging can be easily supported on a 3 m gate Virtex II FPGA.

Smart antenna for C/I improvement and phased array radar beamformer

Phased array radars with a large number of elements and smart antenna for C/I improvement are becoming common for next-

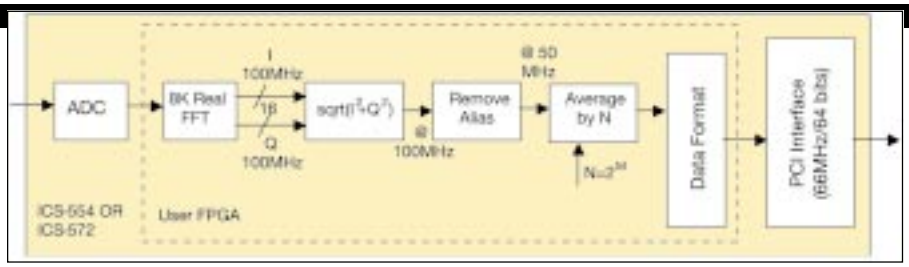

Figure 5. Real-time (Fs=100 MHz) power spectra computation implemented in the onboard Xilinx FPGA.

generation radar and commercial wireless systems. Both these application share a common principle. These systems can handle a large bandwidth and thus pass a large amount of data back and forth. The challenge here is to build a synchronized system with synchronization between multiple DDCs and high-speed data transfer between modules.

ICS has successfully developed and delivered a prototype system that implements a 2 x 2 beamformer at 40 and 20 MHz bandwidths as shown in Figure 8.

For the implementation, two ICS-554s (refer to ICS Tech Note #45) are used to acquire four analog channels. For the 20 MHz bandwidth case, each ICS-554 generates four partial beams, of which two are sent to the other data acquisition card. Each card generates two full beams by combining two partial beams generated internally with two partial beams received from the other ICS-554. The data transfer between boards is 200 MBps each direction for a total of 400 MBps over low-voltage transistor to transistor logic (LVTTL). It is expected that implementing a low-voltage differential signalling (LVDS) interface will dramatically increase data transfer leading to increased bandwidth.

High-speed data transfer over Pn4 PMC user I/O

In some applications, it is more convenient for system integrators to move high-speed data over user-defined protocols from COTS PMC modules, leaving the system bus free for other functionalities. One such protocol that is commonly used is the front-panel data port (FPDP) protocol, which is an American National Standard Institute/VMEbus Industry Trade Association (ANSI/VITA) standard. To ensure high-speed data movement, ICS has implemented transmit and receive cores in the user FPGA to support FPDP over the Pn4 user I/O connector of the PMC module. Thus, system integrators will have a seamless way of moving data in and out of ICS PMC modules over FPDP. Other standard and proprietary data transfer protocols may also be implemented in the user FPGA.

Using LVDS signalling over the Pn4 user I/O connector allows high-speed data transfer between PMC modules or from PMC modules to motherboards. This is useful as larger bandwidth and channel counts put an increasing demand on the data transfer capability. It is undesirable for system engineers to be limited by data transfer bottlenecks, preventing them from using the full feature set of a board.

Conclusion

FPGAs are becoming an integral part of radio design. Increasingly, more functionality is being ported to the FPGA. However, FPGAs and traditional DSPs and GPPs are going to coexist, and a flexible platform will include a mix of both.

FPGA design should be treated like a hardware design exercise and not just a software design problem. This needs to be factored in during project planning stage. RFD

References

ICS has a number of publications containing information on software-defined radio.

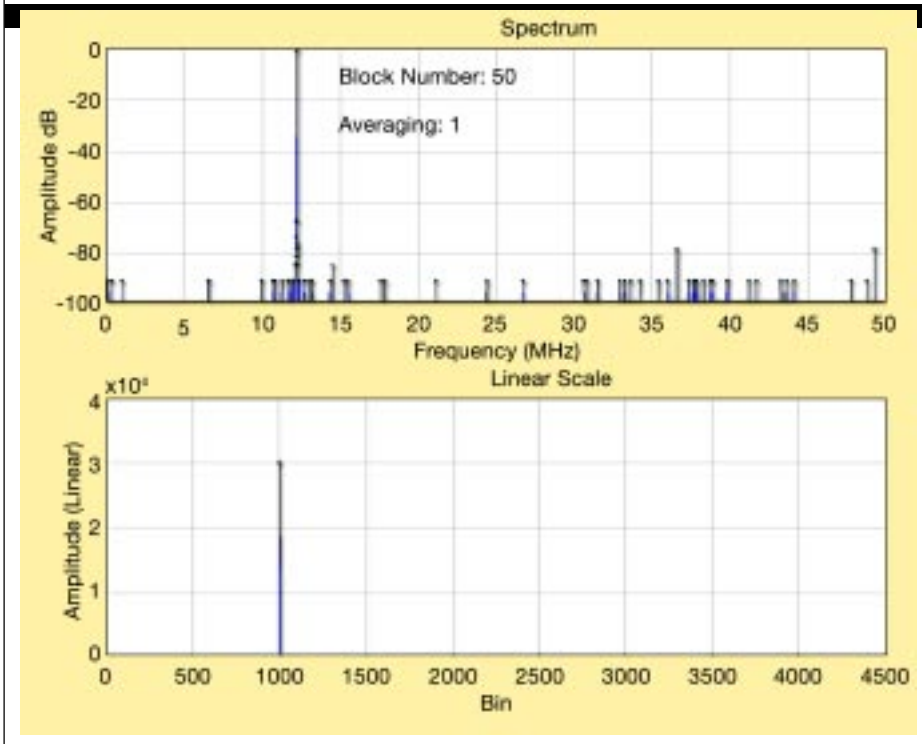

Figure 6. In-system response of the 8K FFT engine with a 12.2 MHz signal.

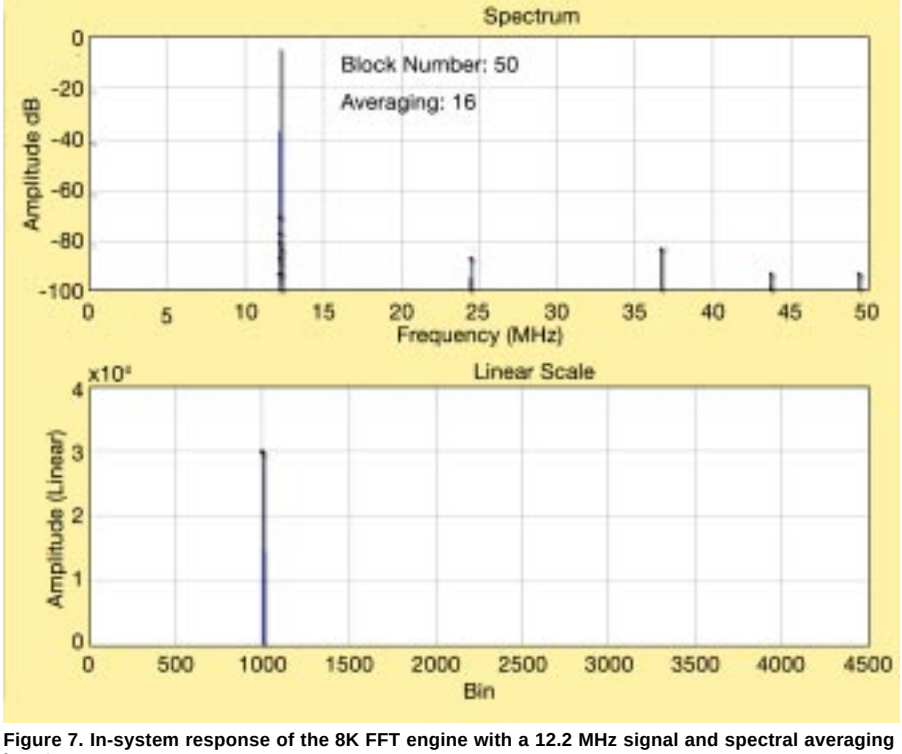

Figure 7. In-system response of the 8K FFT engine with a 12.2 MHz signal and spectral averaging by 16.

These are available from the ICS website www.ics-ltd.com.

1. Graychip DDC & DUC: www.ti.com/graychip

2. Intersil DDC & DUC: www.intersil.com.

3. *RF Design*, July 2003, "Multichannel Multiband VHF Software Radio Based Receiver Eliminates RF Downconversion."

4. ICS Tech Note No. 45: "ICS-554: 4-Channel, 14-Bit, 105 MHz PMC ADC Board with Down-Converters and Xilinx FPGA."

5. ICS Tech Note No. 46: "The ICS-564 4-Channel, 14-Bit, 200 MHz DAC PMC Module With Integrated Digital Upconverter and PCI 64/66 Interface."

6. ICS Tech Note No. 48: "The ICS-572 a 2-Channel ADC, 2-Channel DAC, With Xilinx FPGA, SDRAM, QDR SRAM and PCI 64/

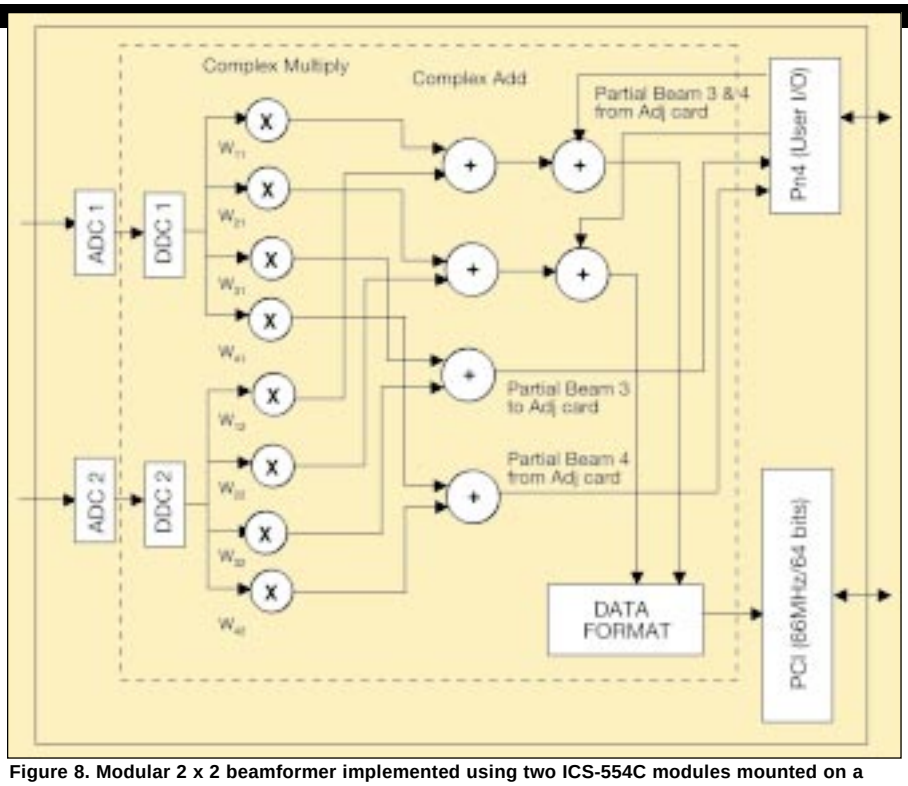

Figure 8. Modular 2 x 2 beamformer implemented using two ICS-554C modules mounted on a single PCI carrier.

66 Interface."

7. ICS Application Note (AN-SR-7): "The Next Generation Software Radio Modules."

8. ICS Application Note (AN-SR-13): "Acquisition and FPGA based processing of Wideband Radio Signals in one PCI bus slot."

9. ICS Application Note (AN-SR-15): "Building a Versatile Low Latency Cognitive Radio for Multimission Applications with the ICS-572."

10. ICS Application Note (AN-SR-15): "Building a Fast Frequency Hopped Radio with Zero Latency."

11. FPDP: www.fpdp.com

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