A 2048 complex point FFT processor for acceleration in Digital Holographic Imaging

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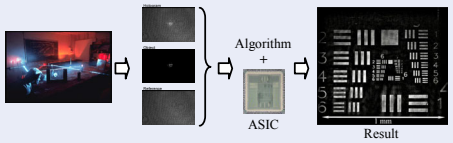
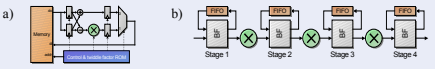
Digital Holographic Imaging

"A key component in a digital holographic imaging system is the holographic video camera. The purpose of the camera is to record the hologram on a solid-state sensor and digitally construct the image. The image construction is very computational expensive involving large 2-dimensional FFT calculations. A major task of designing the camera system will thus be to design the ASIC, which will perform the image reconstruction."



FFT Implementation

In *Digital Holographic Imaging*, a high throughput FFT is required. 2D FFT transforms of up to 2048x2048 complex points should be calculated in real-time. There are many different ways to implement an FFT processor. The computations can be done in a number of iterations by time multiplexing a single memory and arithmetic unit (a), or by using a pipelined architecture (b).



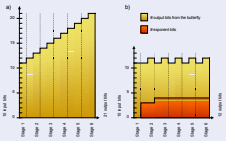
+ Compact design
+ Flexible
- Low throughput

+ High throughput
- Large design

The achieve a high throughput, a pipelined architecture is selected. The implementation is based on the Radix-2^2 decimation-in-frequency algorithm with a single path delay feedback.

Data scaling in pipelined architectures

The problem with a fixed point FFT is to maintain the accuracy and preserve the dynamic range at the same time. One way to achieve a high signal-to-noise ratio is to increase the internal word length for every stage in the pipelined FFT (variable datapath), i.e. the word length will be wider at the output than at the input (a).

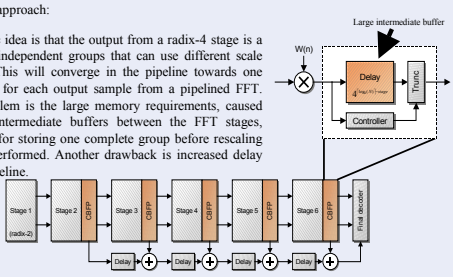


Another way to improve the signal-to-noise ratio without increasing the internal word length is to use data scaling (b). One example of data scaling is *block floating point* that uses exponents, or scaling factors, for internal representation to improve the SNR. The exponents are usually shared between the real and imaginary part of a complex value, or even shared among a set of complex values, unlike normal floating point representation.

Data scaling - Convergent block floating point

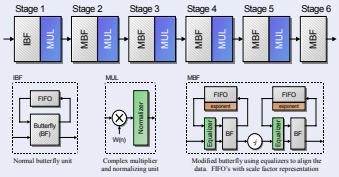
Existing approach:

The basic idea is that the output from a radix-4 stage is a set of 4 independent groups that can use different scale factors. This will converge in the pipeline towards one exponent for each output sample from a pipelined FFT. The problem is the large memory requirements, caused by the intermediate buffers between the FFT stages, required for storing one complete group before rescaling can be performed. Another drawback is increased delay in the pipeline.



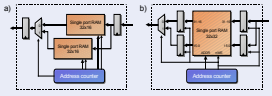
Data scaling - Hybrid floating point

Presented approach:

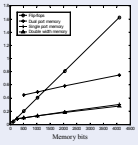


The proposed solution is to rescale data on the fly and minimize the memory requirements. No changes are required of the complex adders/multipliers due to the simple scaling logic using normalizers and equalizing units. The scaling logic uses only one scale factor for representing both the real and imaginary part of a complex value.

Delay feedback implementation



Area comparison

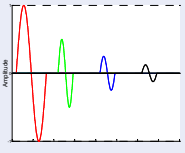


Different approaches:

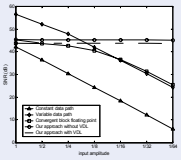
1. Dual port memory connected to an address generator. This allows simultaneous reads and writes to any memory location. Requires larger area than single port memories.
2. Two single port memories, alternating between reading and writing every clock cycle (a). The drawback is duplication of the address logic when using two memories instead of one.
3. Only one single port memory but with double word length (b). This is possible, due to the consecutive addressing scheme used in the delay feedback. In addition to removing the duplicated address logic, the total number of memories for placement will be reduced.

Precision

The proposed FFT processor generates a constant Signal-to-Noise ratio for all kinds of input signals due to the scaling logic in each pipeline stage. An FFT processor using variable datapath produces a higher SNR if the input signal utilizes the full dynamic range, but for arbitrary input signals, scaling can be used to improve the Signal-to-Noise ratio. One of the reasons that CBFP is not capable of keeping a constant SNR is that there is usually no CBFP logic in the first radix-2 stage due to the high memory requirements.



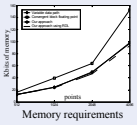
Arbitrary input signals with different amplitudes



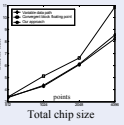
SNR for different amplitudes

Memory and area requirements

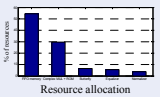
For a 2048 complex point FFT processor, the memory occupies approximately 55% of the chip area. Reducing the memory requirement will therefore significantly affect the total size of the design. Our approach is both memory efficient and accurate.



Memory requirements



Total chip size



Resource allocation

Conclusion

An FFT processor using a novel data scaling approach that can operate on a wide range of input signals, keeping the SNR at a constant level, has been presented. Compared to block scaling approaches, such as CBFP, the proposed design requires significantly smaller chip area due to the reduced memory requirements. At the same time it is capable of producing a higher SNR since scaling is applied in all pipeline stages.