JEDEC STANDARD

High Temperature Storage Life

JESD22-A103C

(Revision of JESD22-A103-B)

NOVEMBER 2004

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A103C

HIGH TEMPERATURE STORAGE LIFE

(From JEDEC Board Ballot JCB-04-96, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices.

High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any).

2 Apparatus

2.1 High temperature storage chambers

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature over the entire sample population under test.

2.2 Electrical test equipment

Electrical equipment capable of performing the appropriate measurements for the devices being tested, including write and verify the required data retention pattern(s) for nonvolatile memories.

3 Procedure

3.1 High temperature storage conditions

The Devices under test shall be subjected to continuous storage at one of the Temperature Conditions of Table 1.

Table 1 — High Temperature storage conditions

Condition A: +125 (-0/+10) °C
Condition B: +150 (-0/+10) °C
Condition C: +175 (-0/+10) °C
Condition D: +200 (-0/+10) °C
Condition E: +250 (-0/+10) °C
Condition F: +300 (-0/+10) °C
Condition G: +85 (-0/+10) °C

NOTE CAUTION should be exercised when selecting an accelerated test condition since the accelerated temperature used may exceed the capabilities of the device and materials, thereby inducing failures (overstress) failures that would not occur under normal use conditions.

As a minimum the following items should be taken into consideration:

1) Melting point of metals present, especially solder. Degradation of metals includes metallurgical interfaces.

2) Package degradation. For example Glass Transition Temperature and thermal stability (in air) of any polymeric materials.

3) Moisture rating of package (per J-STD-020).

4) Temperature limitations of silicon devices. For example: Charge loss in Nonvolatile memories.

The Qualification and Reliability monitoring test conditions have typically duration of 1000 hours per condition B of Table 1 (JESD 47). Other conditions and durations may be used as appropriate.

The devices may be returned to room ambient conditions for interim electrical measurements.

3 Procedure (cont'd)

3.2 Measurements

Unless otherwise specified, interim and final electrical test measurements shall be completed within 96 hours after removal of the devices from the specified test conditions. Intermediate measurements are optional unless otherwise specified.

The electrical test measurements shall consist of parametric and functional tests specified in the applicable procurement document. For nonvolatile memories, the data specified data retention pattern must be written initially, and then subsequently verified without re-writing.

3.3 Failure criteria

A device will be considered a High Temperature Storage failure if parametric limits are exceeded, or if functionality cannot be demonstrated under nominal and worst-case conditions, as specified in the applicable procurement document. For nonvolatile memories, the specified data retention pattern shall be verified before and after storage. A margin test may be used to detect data retention degradation.

Mechanical damage, such as cracking, chipping, or breaking of the package, (as defined in test method B101 "External visual") will be considered a failure, provided that such damage was not induced by fixtures or handling and it is critical to the package performance in the specific application.

Cosmetic package defects and degradation of lead finish, or solderability are not considered valid failure criteria for this stress.

4 Summary

The following details shall be specified in the applicable procurement document.

a) Electrical test measurements.

b) Sample size and number of failures (specify zero if none observed).

c) Time and conditions, if other than 1000 hours per condition B.

d) Intermediate electrical test measurements, if required.

e) Nonvolatile memory data retention pattern (for appropriate devices)

Annex A (informative) Difference between JESD22-A103C and JESD22-A103-B

This table briefly describes most of the changes made to entries that appear in this standard, JESD22-A103C, compared to its predecessor, JESD22-A103-B (August 2001). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description of change
2	Add Test Condition G + 85°C to Table 1- High Temperature storage conditions

Standard Improvement Form **JEDEC JESD22-A103C**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

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